MS-7345

ATX Version: 1.2

CPU: **Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.**

System Chipset:

Intel Bearlake - Q/G/P (G33, P35, Q35/33North Bridge)
Intel ICH9 (South Bridge)

On Board Device:

CLOCK Gen -- ICS 9LPRS906
LPC Super I/O -- Fintek F71882F
LAN -- Realtek 8111 (PCIE)
HD Audio Codec -- RTL888/888T
1394 Controller -- VT6308 (2-port)
PCIE to PATA/SATA Bridge -- Marvel 88SE6111

Main Memory:

Dual-channel DDR-II * 4

Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X4 SLOT — **Alternative**
PCI EXPRESS X1 SLOT * 2 — **Alternative**
PCI SLOT * 2

PWM: **Intersil ISL6322 (4 Phases) w/ ISL6612 driver**

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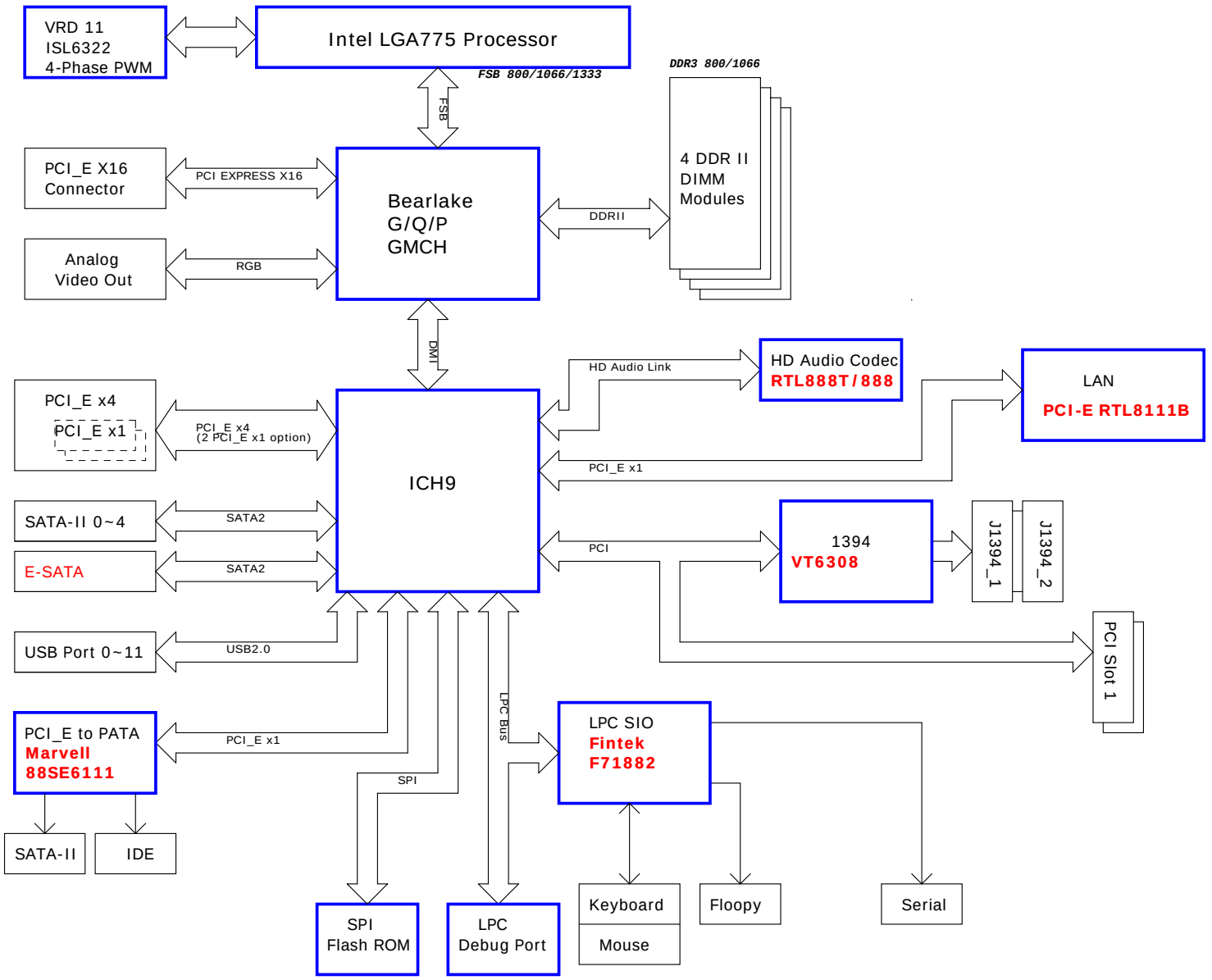
MS-7345

Size: Custom | Document Description: COVER SHEET | Rev: 1.2

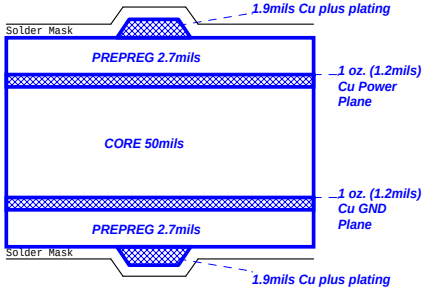
Date: Friday, May 18, 2007 | Sheet 1 of 35

Block Diagram



Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
LAN - 100ohm : 15/4/8/4/15
PCIE - 95ohm : 15/4/8/4/15
IEEE1394 - 110ohm : 15/4/9/4/15
IDE : 15/4/8/4/15

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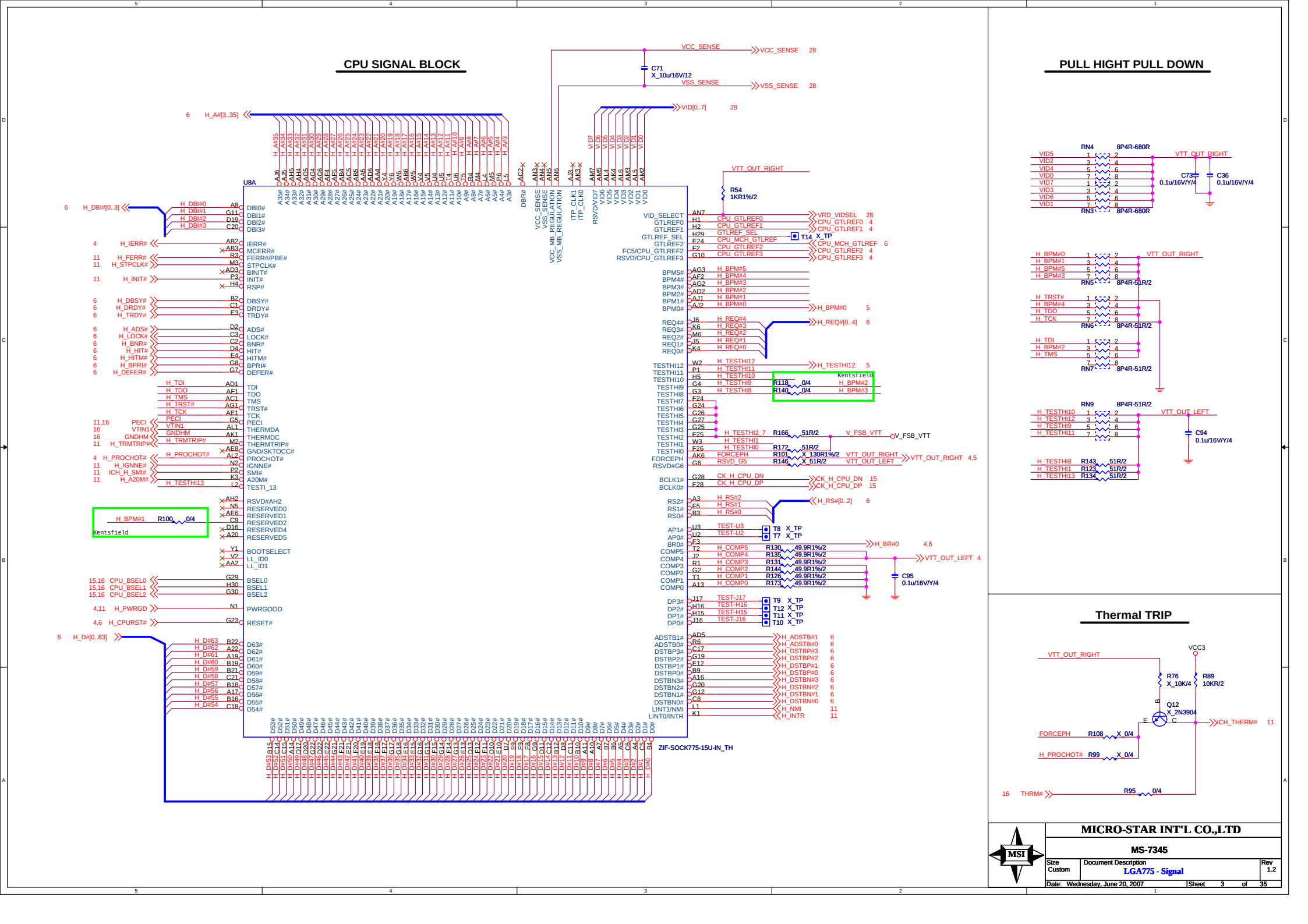
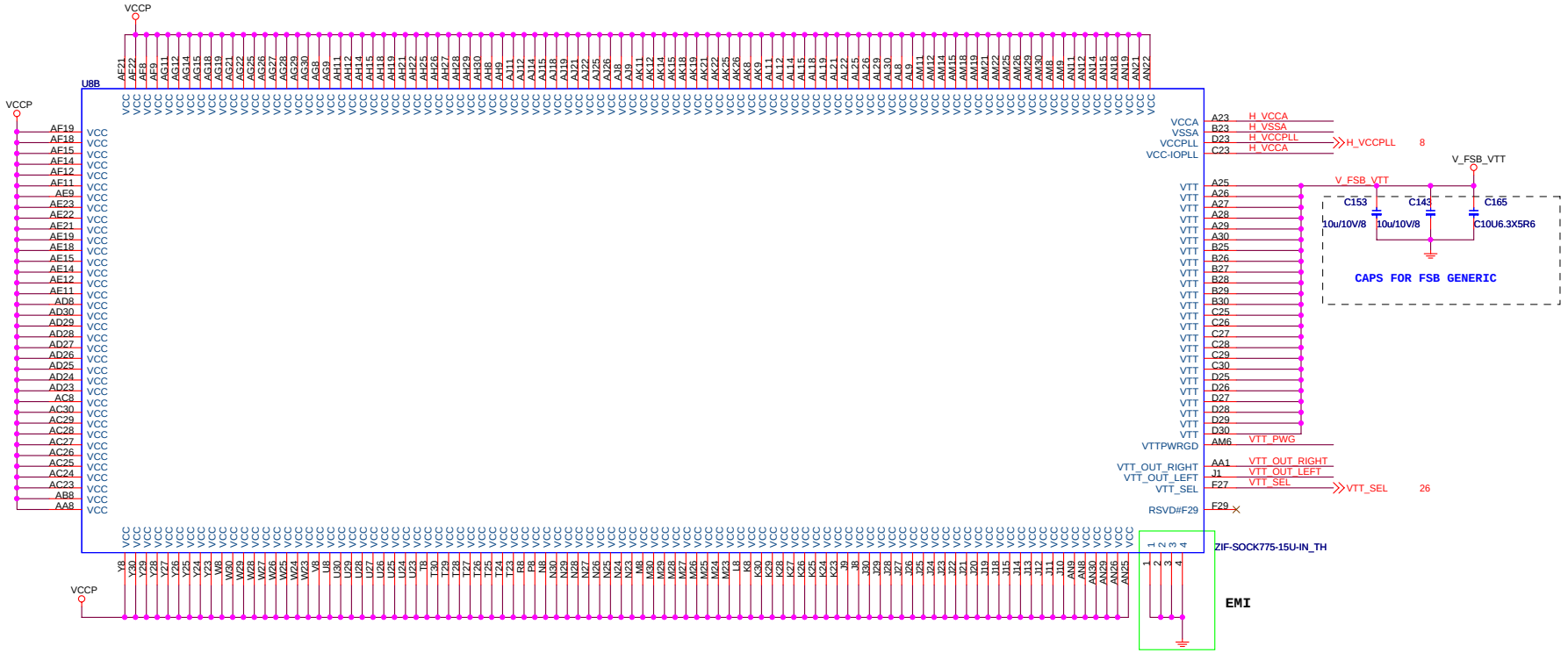
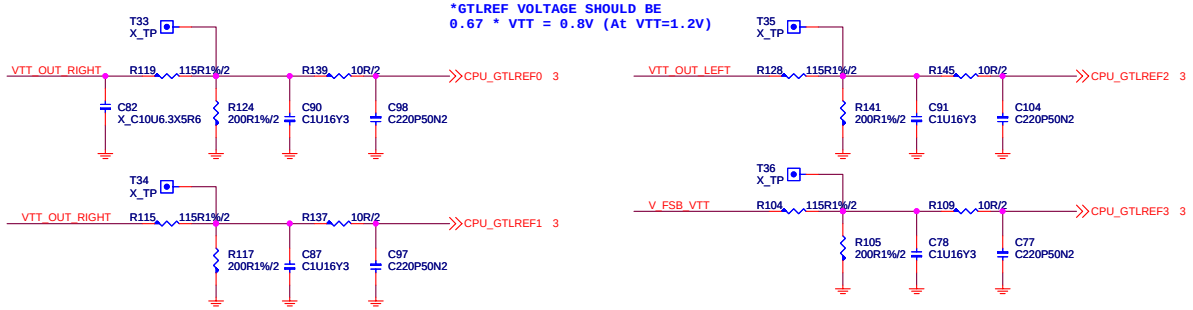
MS-7345		
Size: Custom	Document Description: BLOCK DIAGRAM	Rev: 1.2
Date: Friday, May 18, 2007	Sheet 2 of 35	

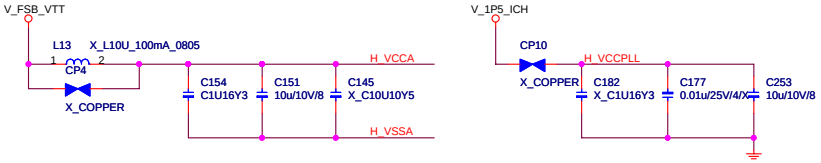

CPU SIGNAL BLOCK
PULL HIGHT PULL DOWN
Thermal TRIP
U8A
ZIF-SOCK775-15U-IN_TH
MICRO-STAR INT'L CO.,LTD
MS-7345
LGA775 - Signal
Size Custom
Rev 1.2
Date: Wednesday, June 20, 2007
Sheet 3 of 35



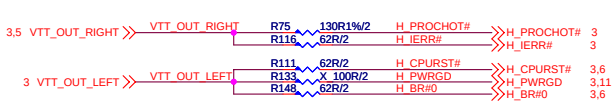
*GTLREF VOLTAGE SHOULD BE
0.67 * VTT = 0.8V (At VTT=1.2V)



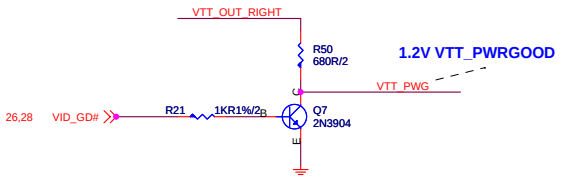
*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS



PLACE AT CPU END OF ROUTE



VTT_PWRGOOD



VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns

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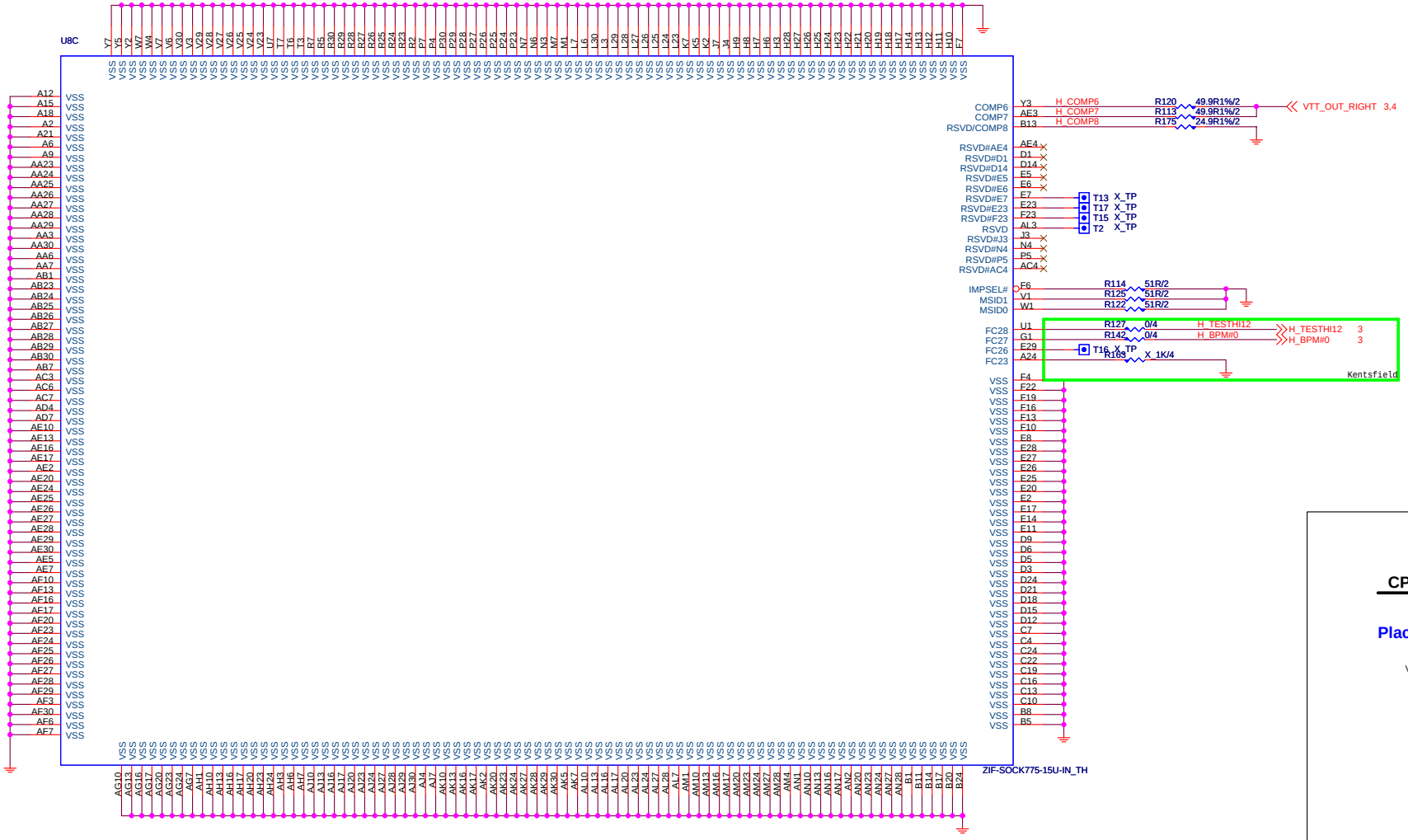
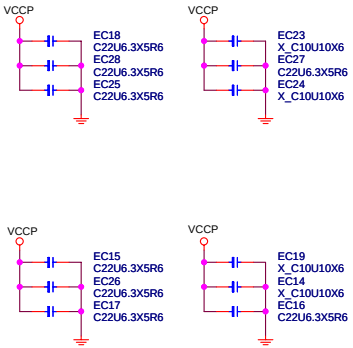
MS-7345		
Size: Custom	Document Description: LGA775 - Power	Rev: 1.2
Date: Friday, May 18, 2007	Sheet 4 of 35	



CPU DECOUPLING CAPACITORS

Place these caps within socket cavity



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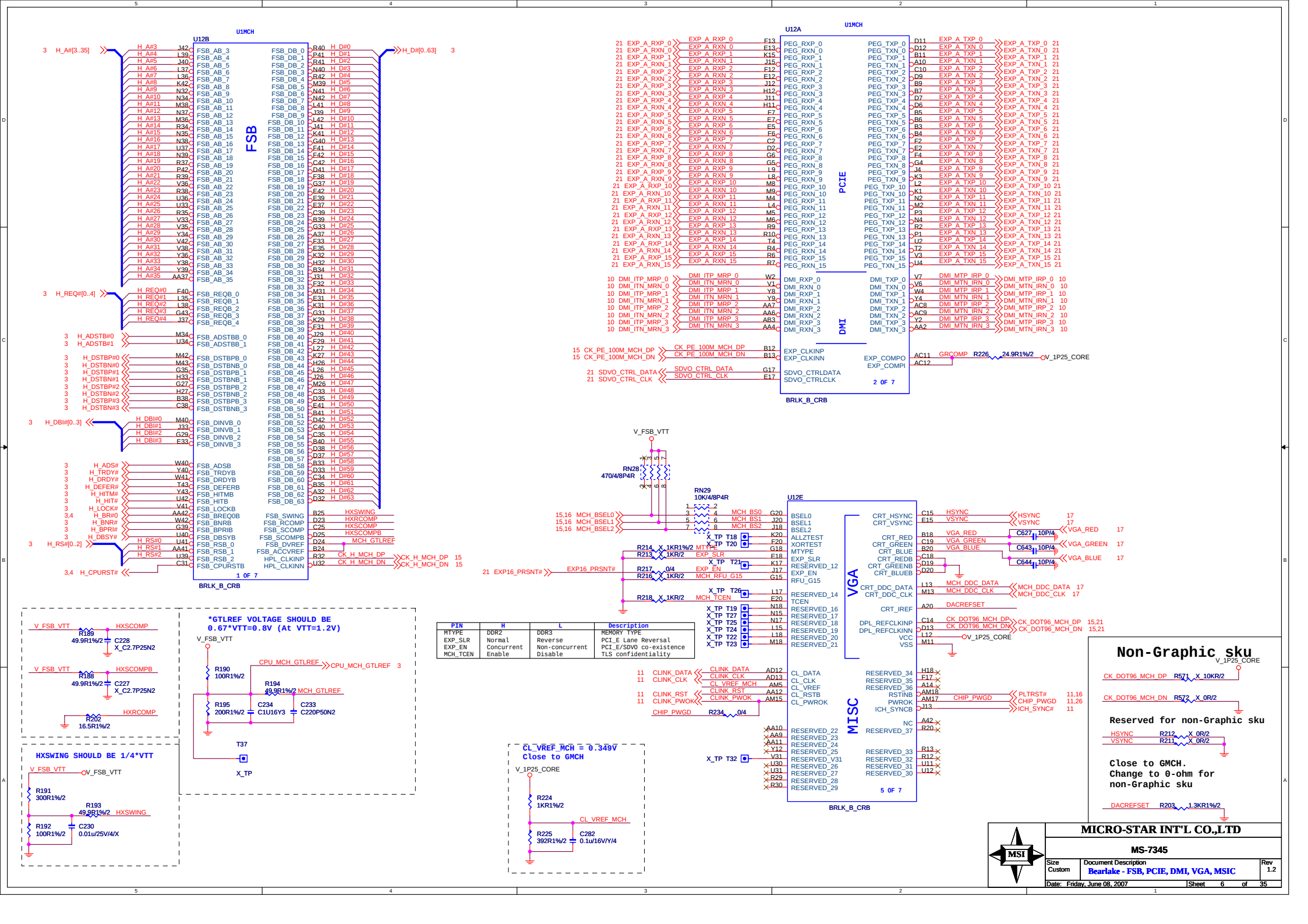
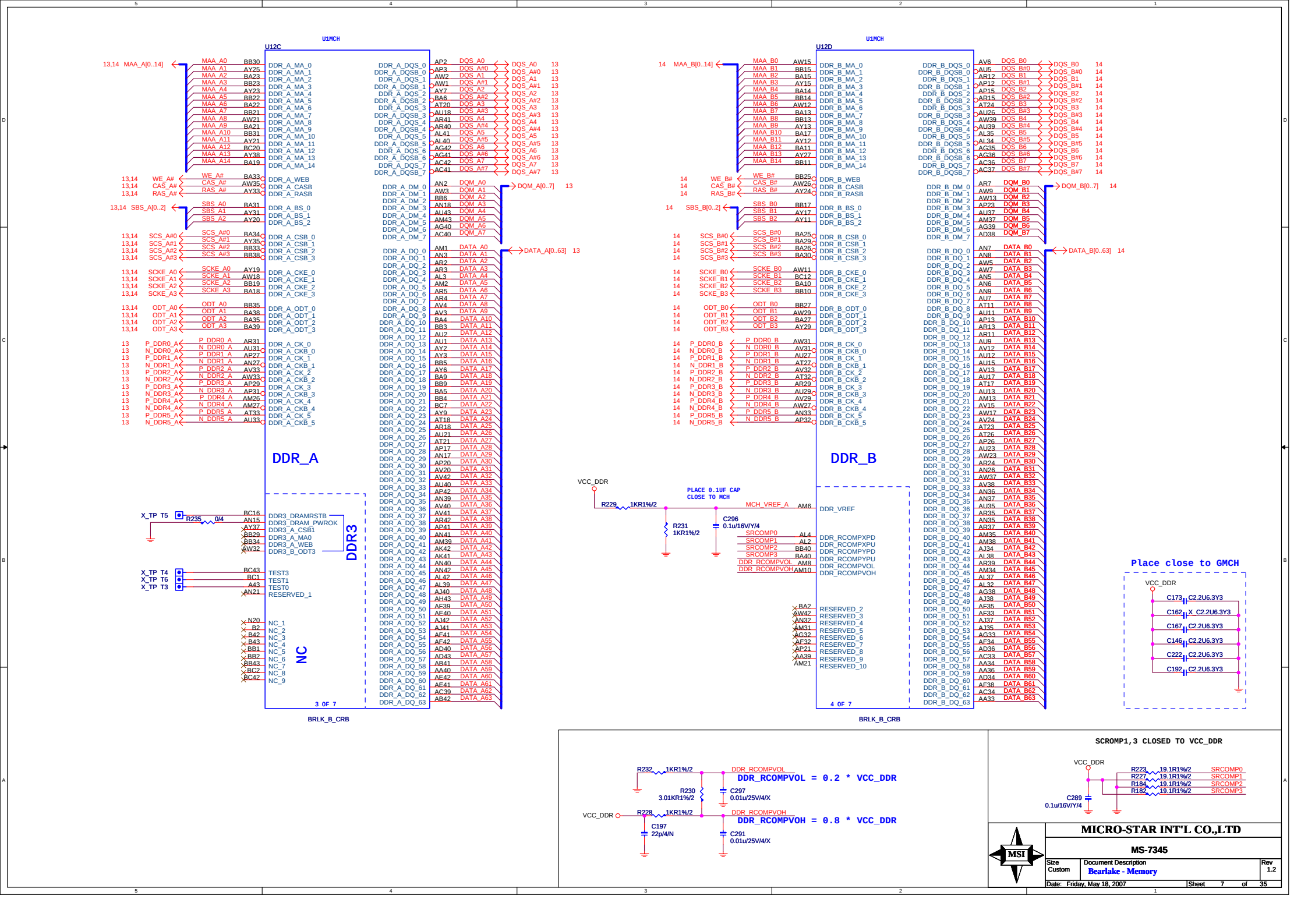
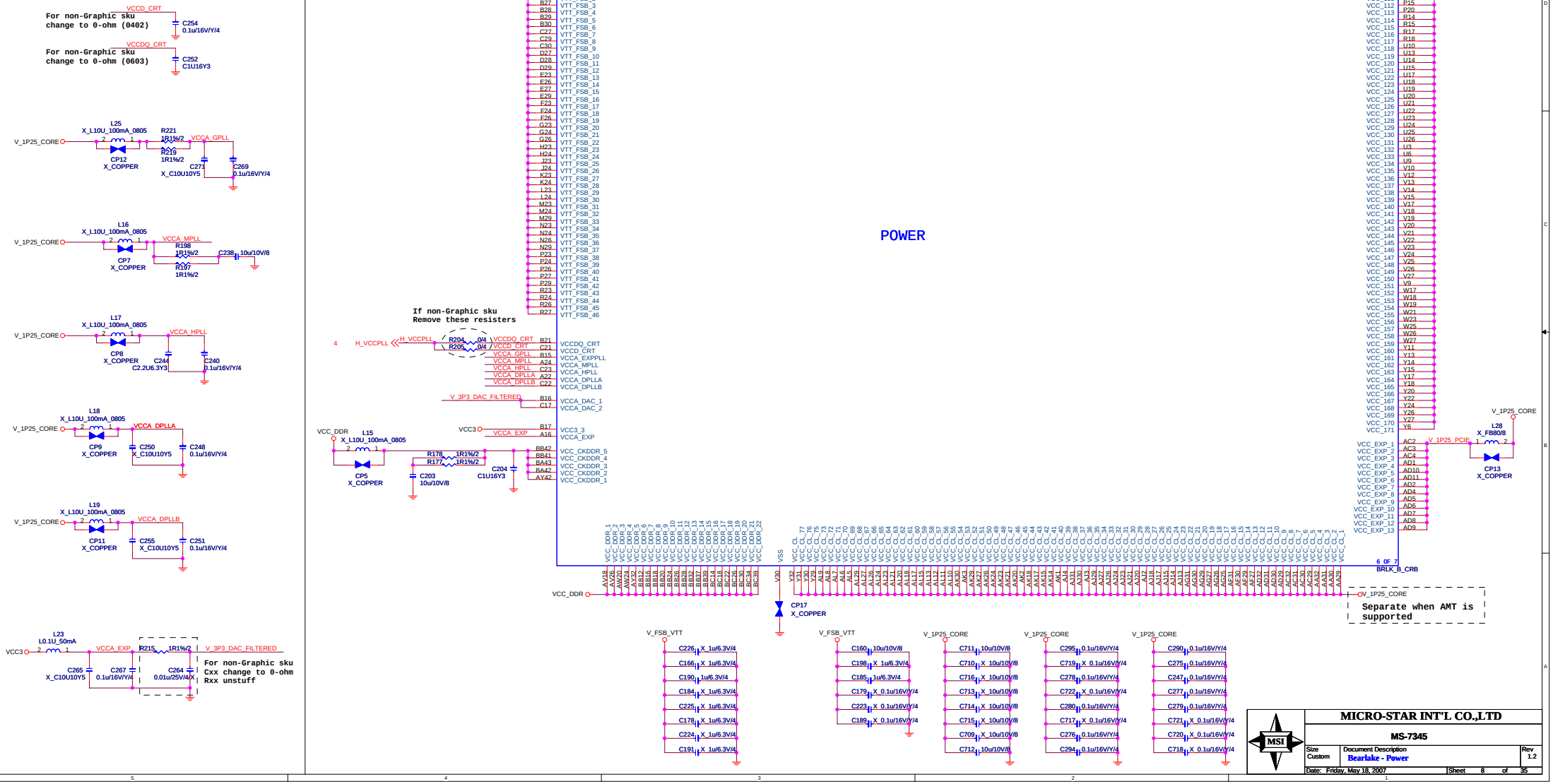
MS-7345		
Size: Custom	Document Description: LGA775 - GND	Rev: 1.2
Date: Thursday, May 31, 2007	Sheet 5 of 35	

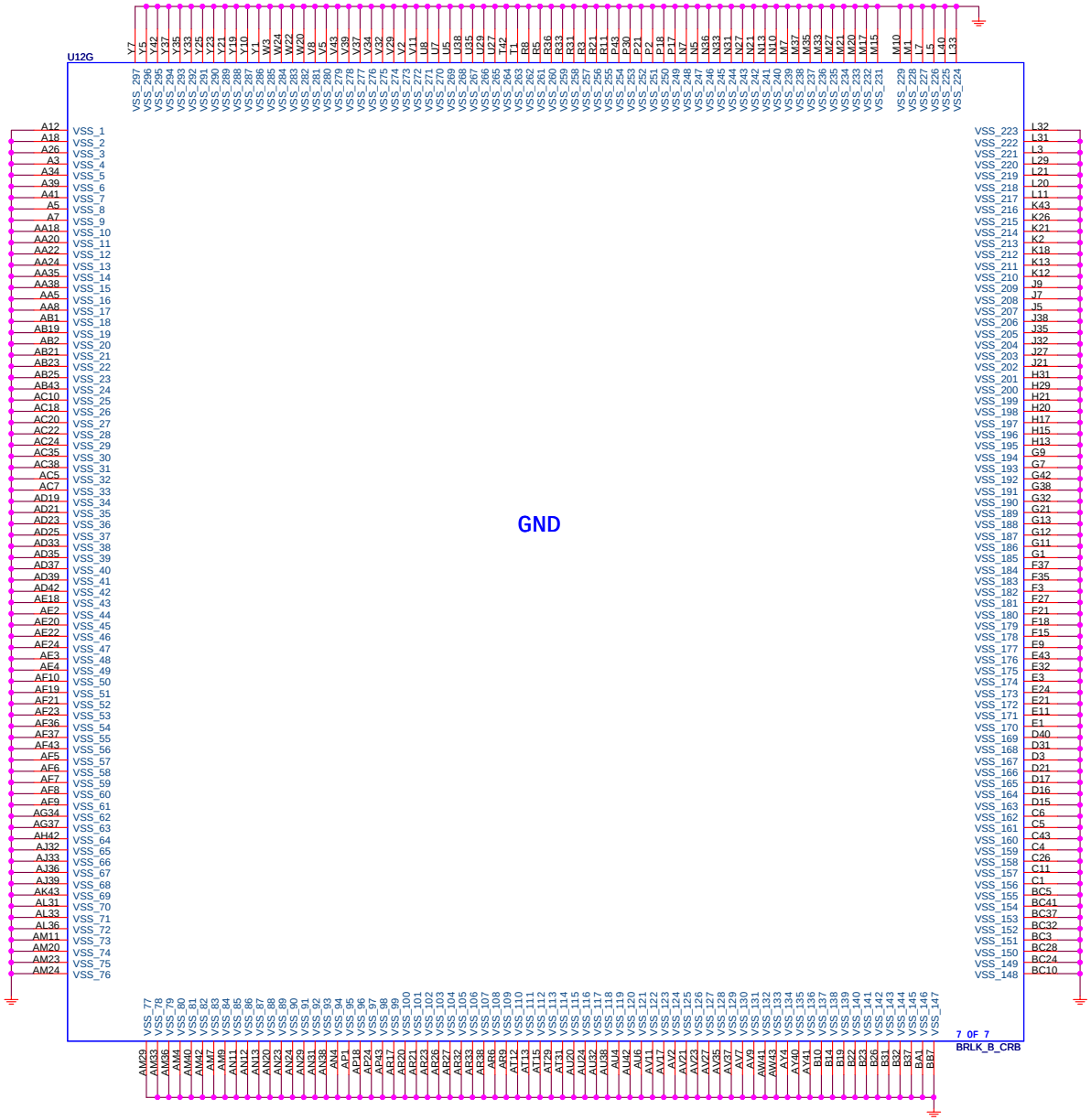


PIN	H	L	Description
MTYPE	DDR2	DDR3	MEMORY TYPE
EXP_SLR	Normal	Reverse	PCI_E Lane Reversal
EXP_EN	Concurrent	Non-concurrent	PCI_E/SDVO co-existence
MCH_TCEN	Enable	Disable	TLS confidentiality

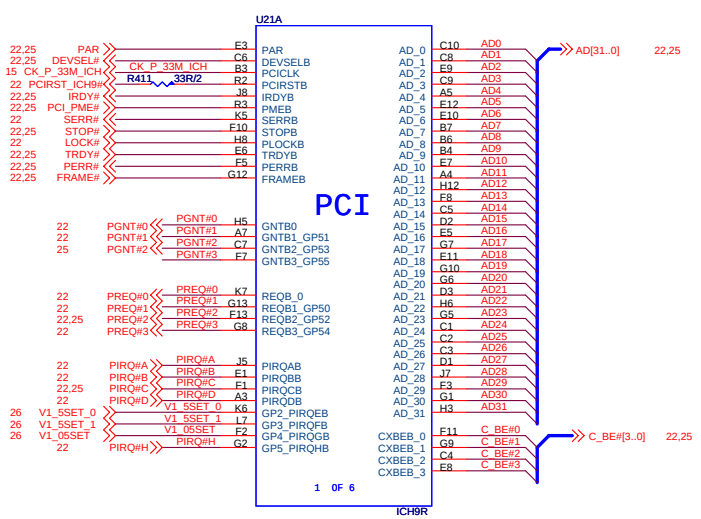

U1MCH
U12C
DDR_A
DDR3
NC
3 OF 7
BRLK_B_CRB
U1MCH
U12D
DDR_B
DDR_VREF
4 OF 7
BRLK_B_CRB
PLACE 0.1UF CAP
CLOSE TO MCH
VCC_DDR
R229 1KR1%/2
R231 1KR1%/2
C296 0.1u/16V/Y/4
MCH_VREF_A
SRCOMP0
SRCOMP1
SRCOMP2
SRCOMP3
DDR_RCOMPVOL
DDR_RCOMPVOH
Place close to GMCH
C173 C2.2U6.3Y3
C162 C2.2U6.3Y3
C167 C2.2U6.3Y3
C146 C2.2U6.3Y3
C222 C2.2U6.3Y3
C192 C2.2U6.3Y3
R232 1KR1%/2
R230 3.01KR1%/2
R228 1KR1%/2
C297 0.01u/25V/4/X
C197 22p/4/N
C291 0.01u/25V/4/X
DDR_RCOMPVOL = 0.2 * VCC_DDR
DDR_RCOMPVOH = 0.8 * VCC_DDR
SCROMP1,3 CLOSED TO VCC_DDR
R223 19.1R1%/2
R227 19.1R1%/2
R184 19.1R1%/2
R182 19.1R1%/2
C289 0.1u/16V/Y/4
MICRO-STAR INT'L CO.,LTD
MS-7345
Size Custom
Document Description
Bearlake - Memory
Rev 1.2
Date: Friday, May 18, 2007
Sheet 7 of 35

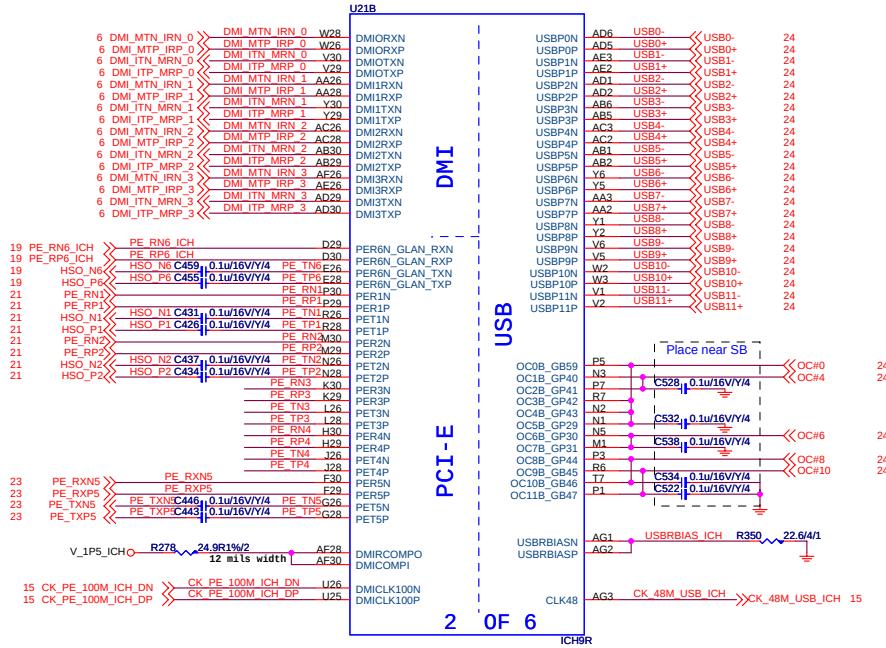
NB POWER


POWER
U12F
For non-Graphic sku
change to 0-ohm (0402)
For non-Graphic sku
change to 0-ohm (0603)
If non-Graphic sku
Remove these resisters
For non-Graphic sku
Cxx change to 0-ohm
Rxx unstuff
Separate when AMT is supported
6 OF 7
BRLK_B_CRB
CP17
X_COPPER
MICRO-STAR INT'L CO.,LTD
MS-7345
Bearlake - Power
Size Custom
Rev 1.2
Date: Friday, May 18, 2007
Sheet 8 of 35

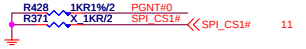


MICRO-STAR INT'L CO.,LTD	
MS-7345	
Size: Custom	Document Description: Bearlake - GND
Rev: 1.2	
Date: Friday, May 18, 2007	Sheet 9 of 35

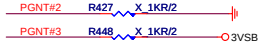




SB STRAPPING RESISTOR

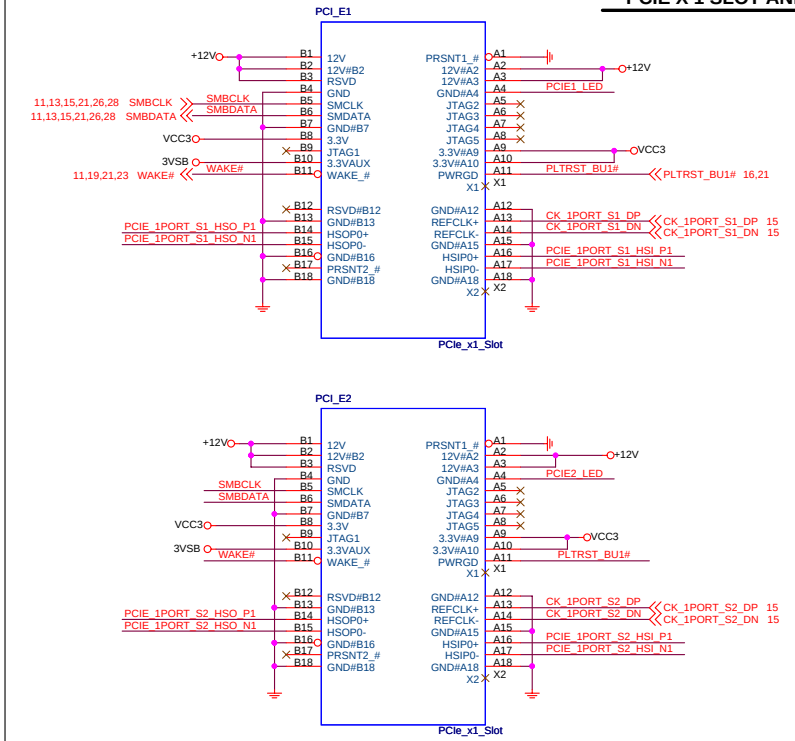


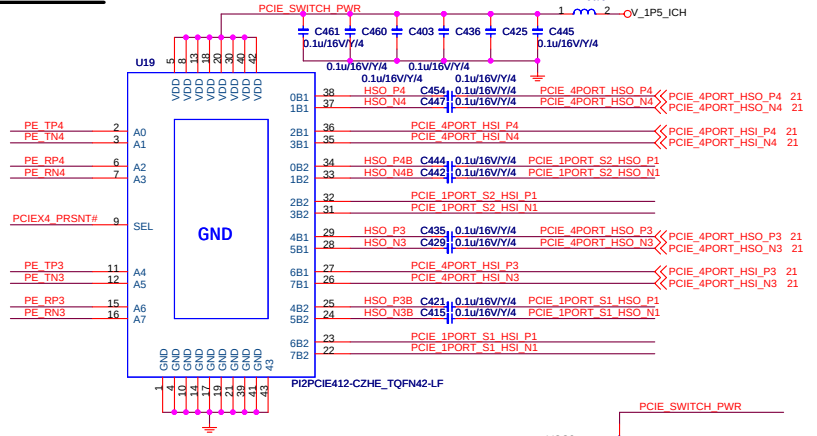
BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
FWH	1	1
SPI	0	X
PCI	1	0

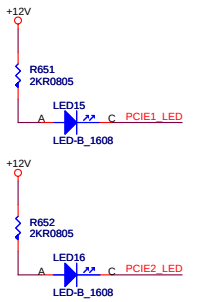


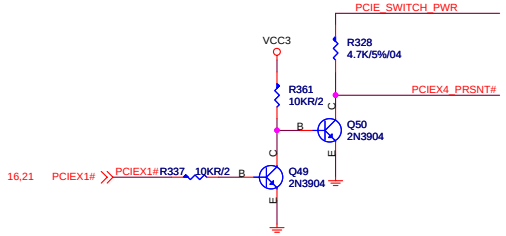
SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

PCIE X 1 SLOT AND SWITCH









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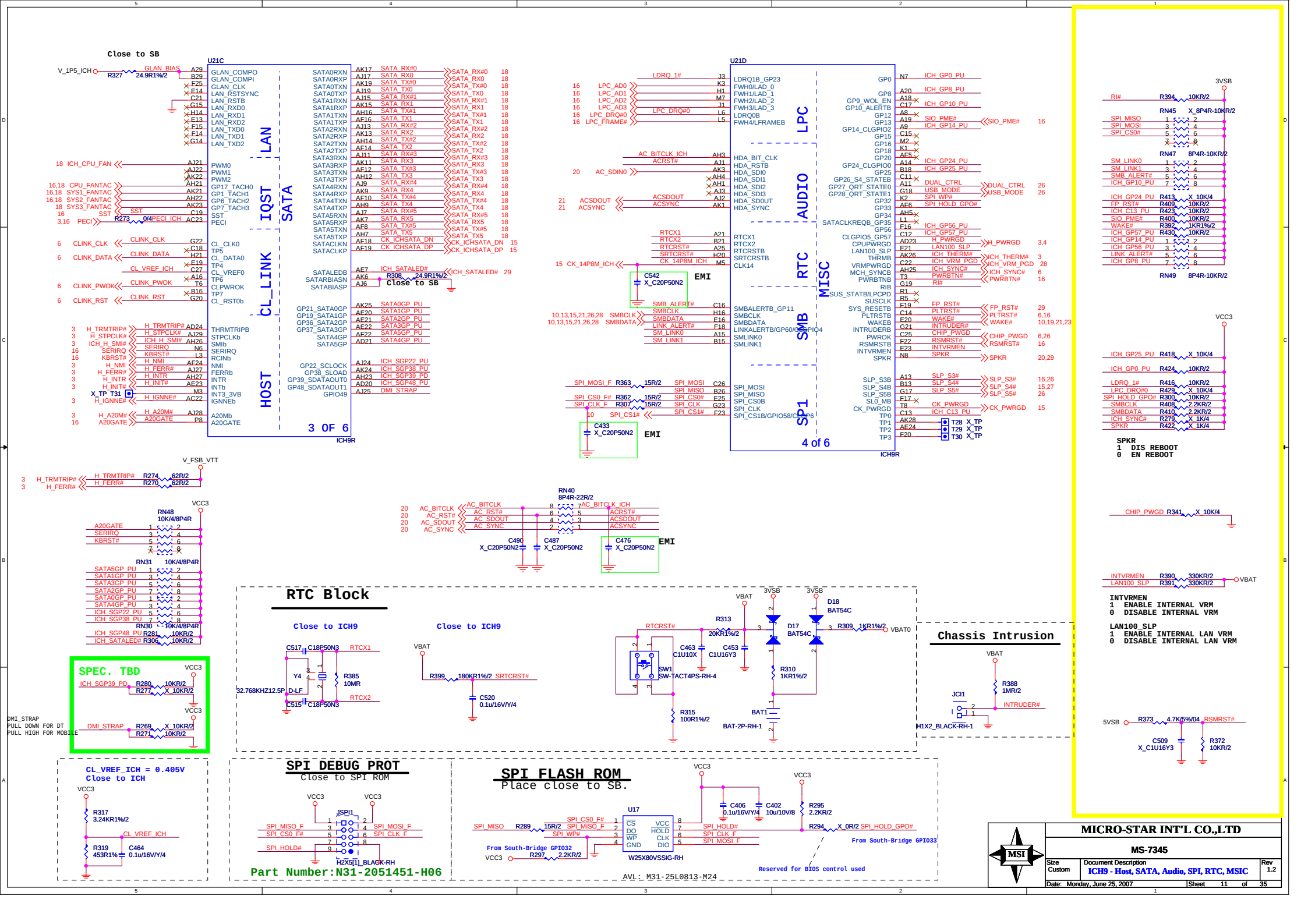
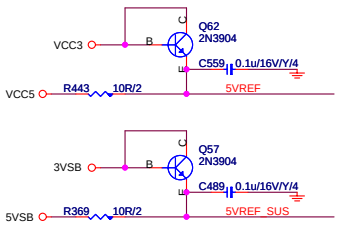
MS-7345

Size	Document Description	Rev
Custom	ICH9 - PCI, DMI, USB, PCIE & Slots	1.2

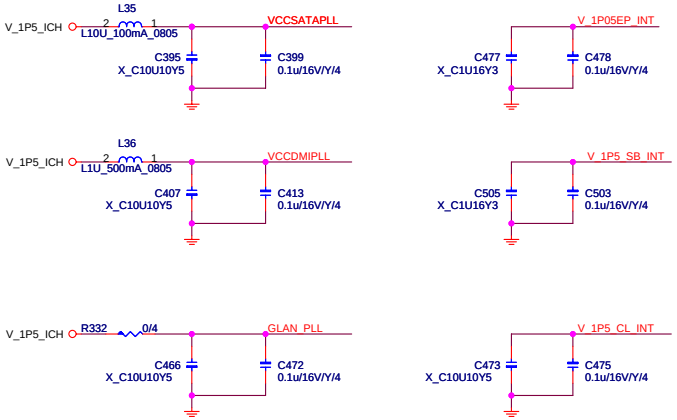
Date: Friday, May 18, 2007 Sheet 10 of 35

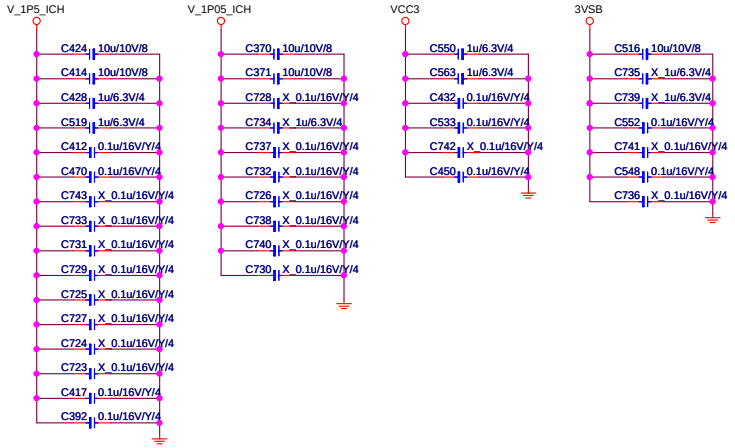

Close to SB
U21C
LAN
IQST
SATA
CL_LINK
HOST
3 OF 6
ICH9R
U21D
LPC
AUDIO
RTC
MISC
SMB
SPI
4 of 6
ICH9R
EMI
EMI
EMI
RTC Block
Close to ICH9
Close to ICH9
SPEC. TBD
Chassis Intrusion
CL_VREF_ICH = 0.405V
Close to ICH
SPI DEBUG PROT
Close to SPI ROM
SPI FLASH ROM
Place close to SB.
Part Number:N31-2051451-H06
AVL: M31-25L0813-M24
SPKR
1 DIS REBOOT
0 EN REBOOT
INTVRMEN
1 ENABLE INTERNAL VRM
0 DISABLE INTERNAL VRM
LAN100_SLP
1 ENABLE INTERNAL LAN VRM
0 DISABLE INTERNAL LAN VRM
MICRO-STAR INT'L CO.,LTD
MS-7345
ICH9 - Host, SATA, Audio, SPI, RTC, MSIC
Monday, June 25, 2007

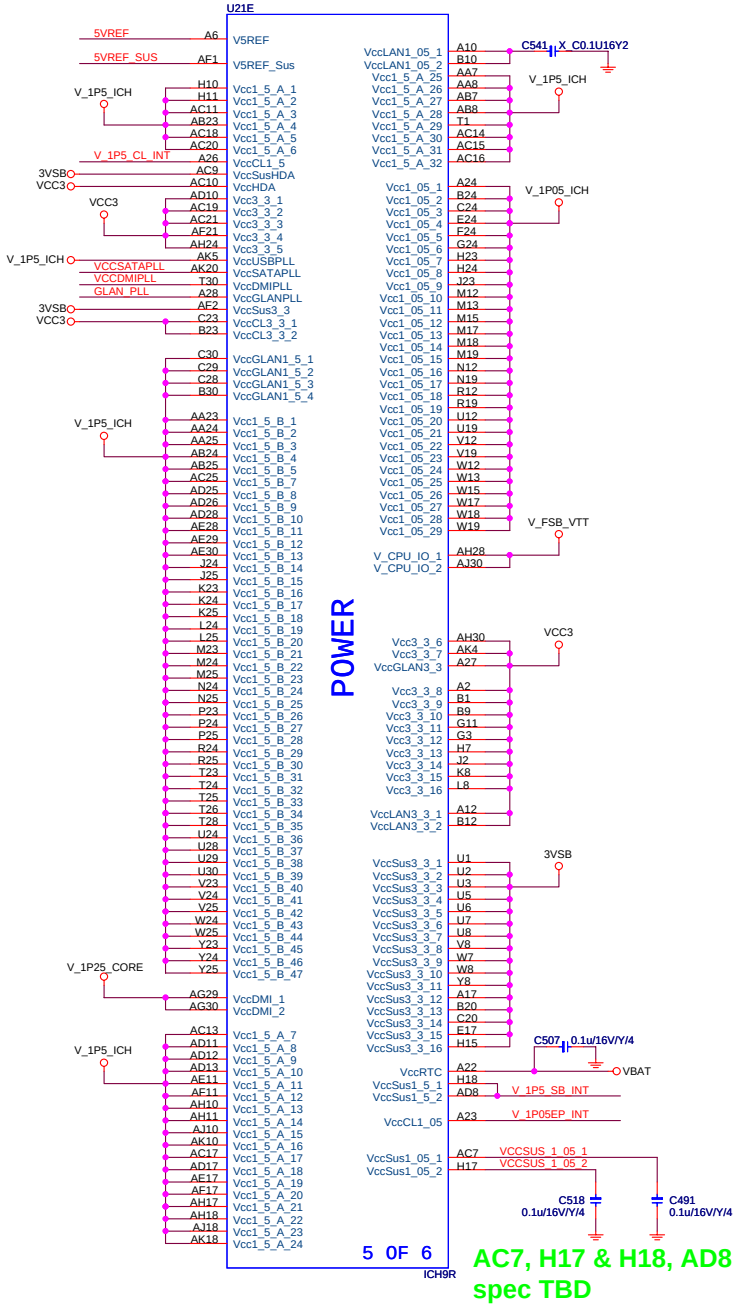
5VREF & 5VREF_SUS Sequencing Circuit

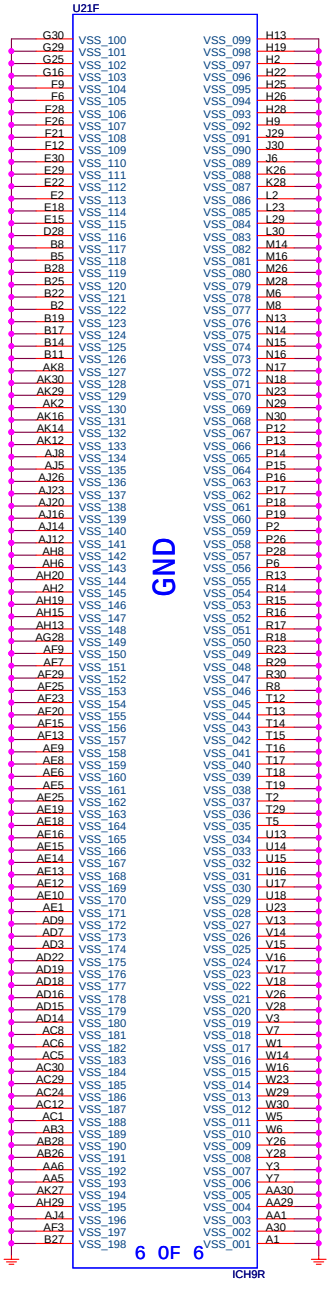


SB POWER









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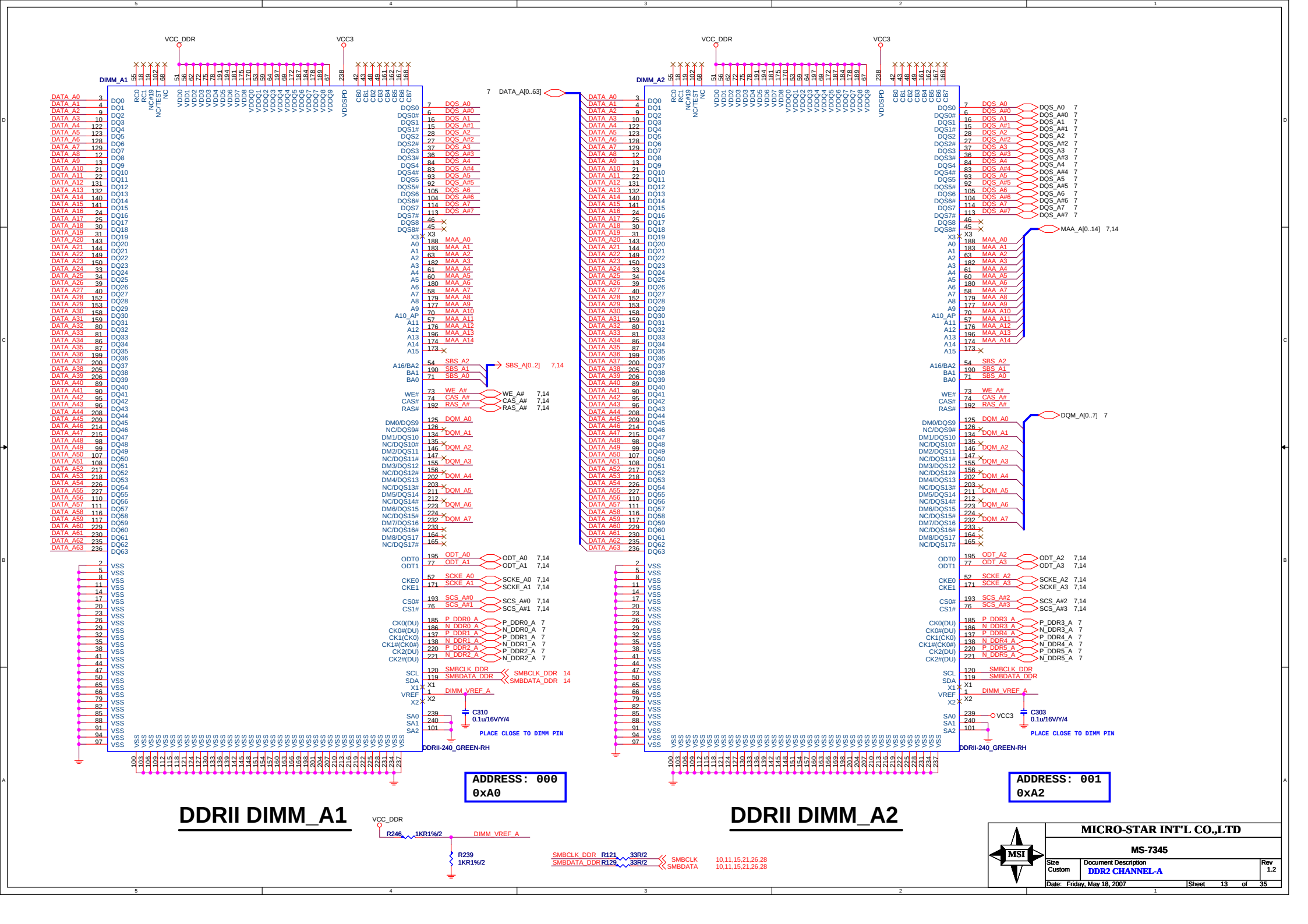
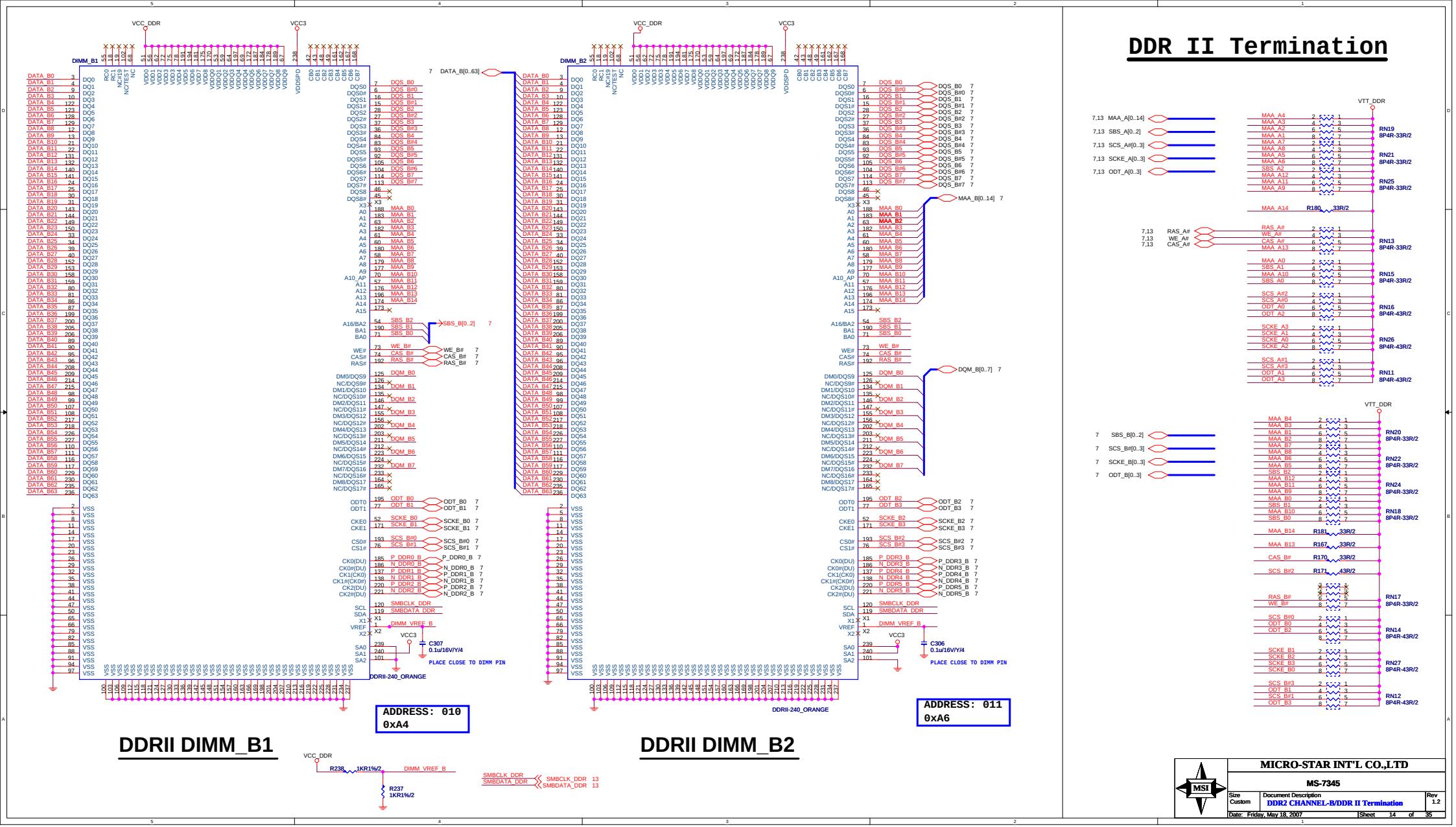
MS-7345

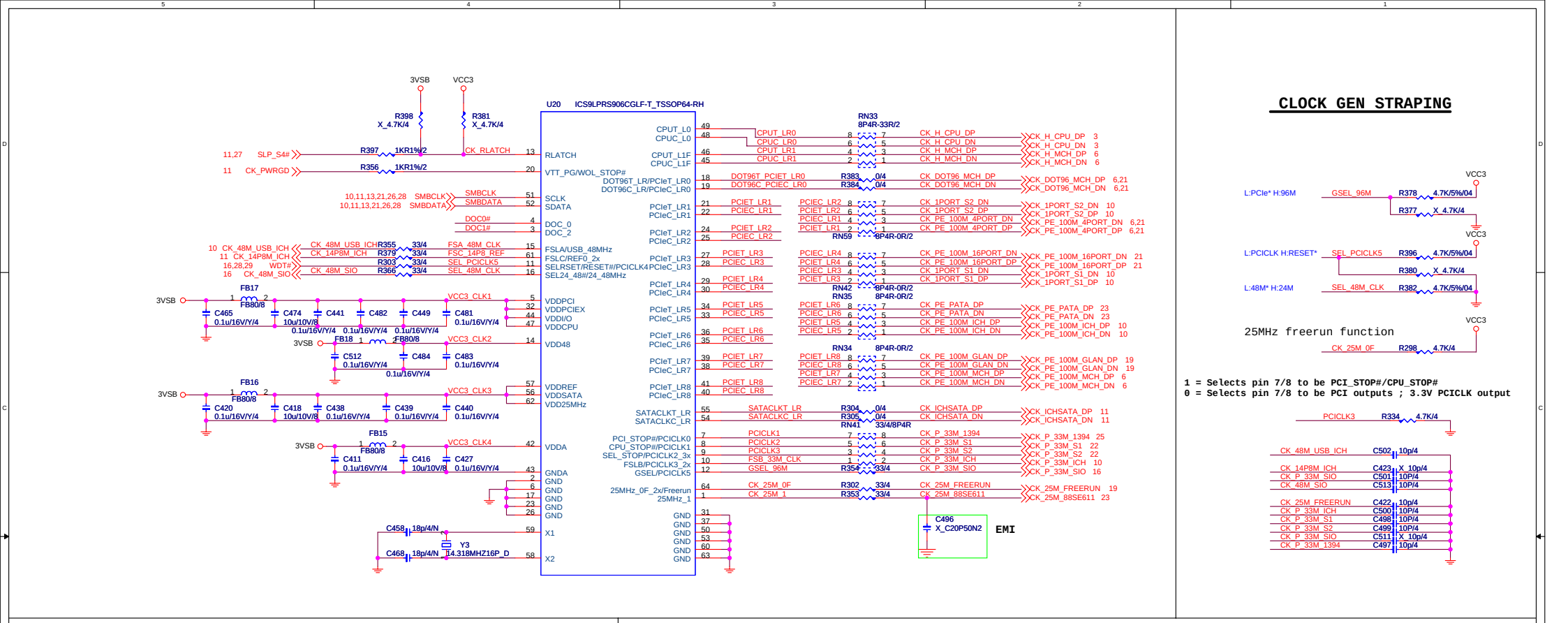
Size	Document Description	Rev
Custom	ICH9 - Power, GND	1.2

Date: Friday, May 18, 2007 | Sheet 12 of 35



MICRO-STAR INT'L CO.,LTD	
MS-7345	
Size: Custom	Document Description: DDR2 CHANNEL-A
Rev: 1.2	
Date: Friday, May 18, 2007	Sheet 13 of 35

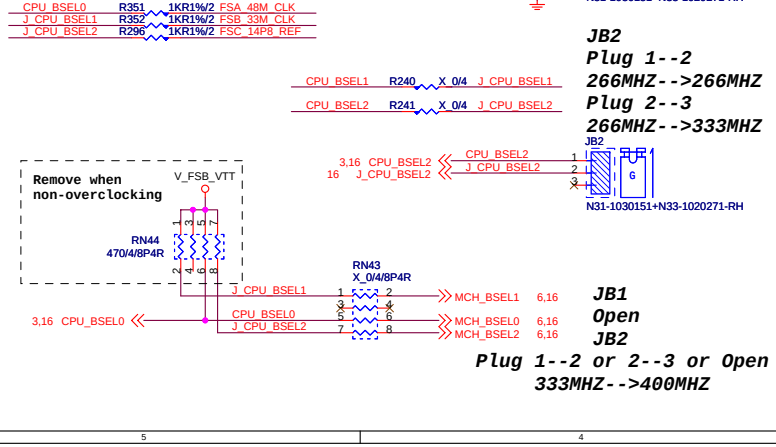

DDR II Termination
DDRII DIMM_B1
DDRII DIMM_B2
DIMM_B1
DIMM_B2
VCC_DDR
VCC3
VTT_DDR
DDRII-240_ORANGE
ADDRESS: 010
0xA4
ADDRESS: 011
0xA6
C307
0.1u/16V/Y/4
C306
0.1u/16V/Y/4
PLACE CLOSE TO DIMM PIN
R238 1KR1%/2
R237 1KR1%/2
DIMM_VREF_B
SMBCLK_DDR
SMBDATA_DDR
MICRO-STAR INT'L CO.,LTD
MS-7345
Size Custom
Document Description
DDR2 CHANNEL-B/DDR II Termination
Rev 1.2
Date: Friday, May 18, 2007
Sheet 14 of 35

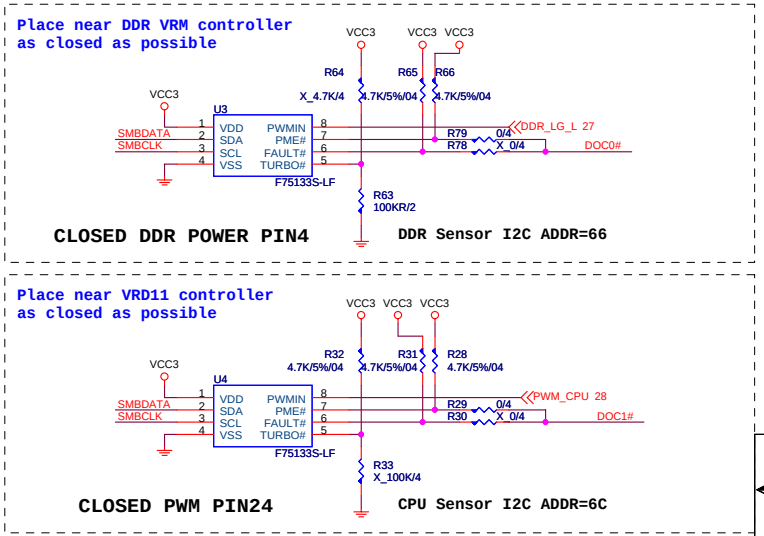


CLOCK GEN STRAPING

1 = Selects pin 7/8 to be PCI_STOP#/CPU_STOP#
0 = Selects pin 7/8 to be PCI outputs ; 3.3V PCICLK output

BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	266 MHz (1066)
1	0	0	333 MHZ (1333)
0	1	0	200 MHZ (800)
1	1	0	400 MHZ (1600)





EASY DOT FUNCTION

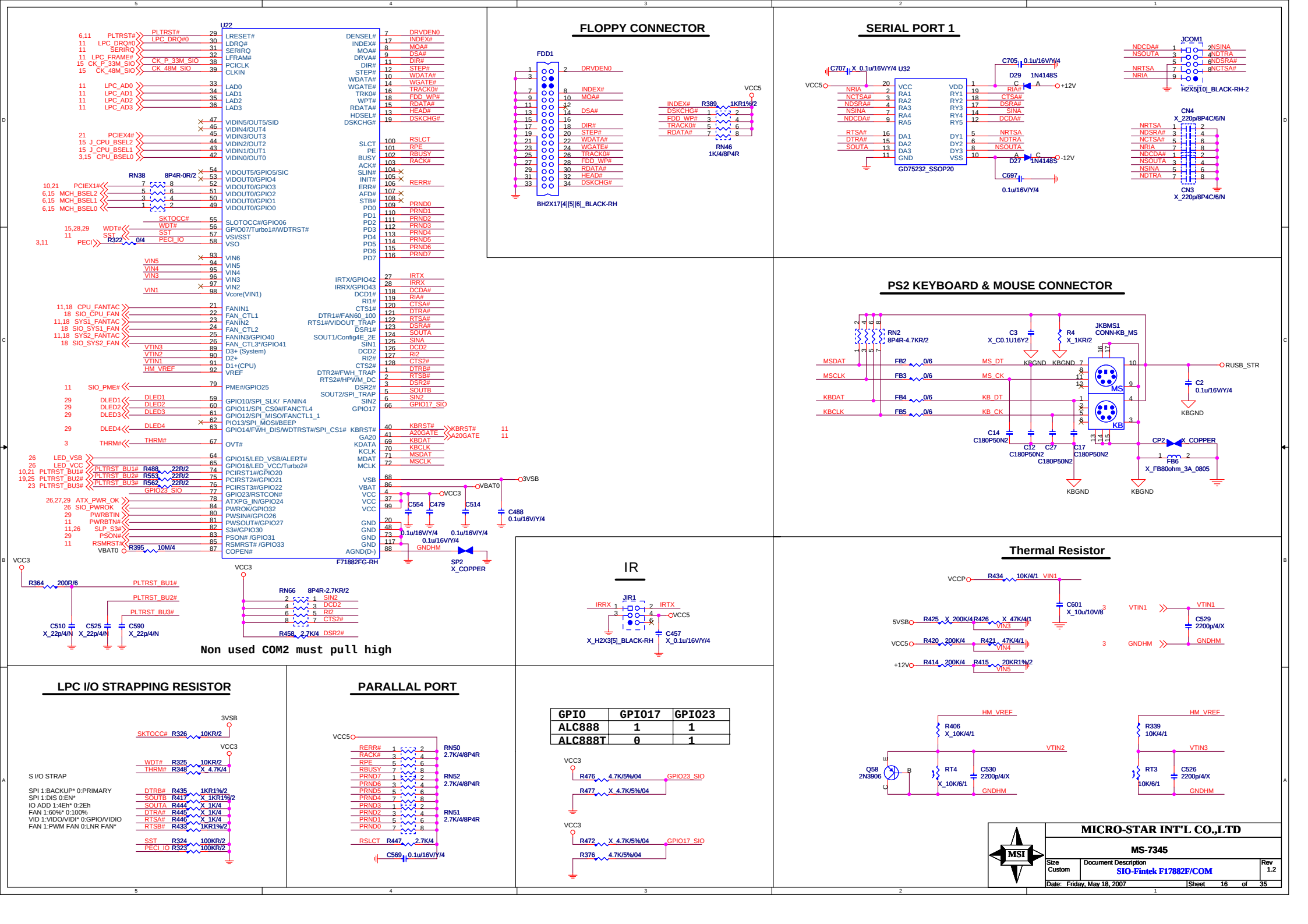
DOC#0	DOC#1	Over-clk
1	1	15%
0	1	10%
1	0	5%
0	0	Normal

MICRO-STAR INT'L CO.,LTD

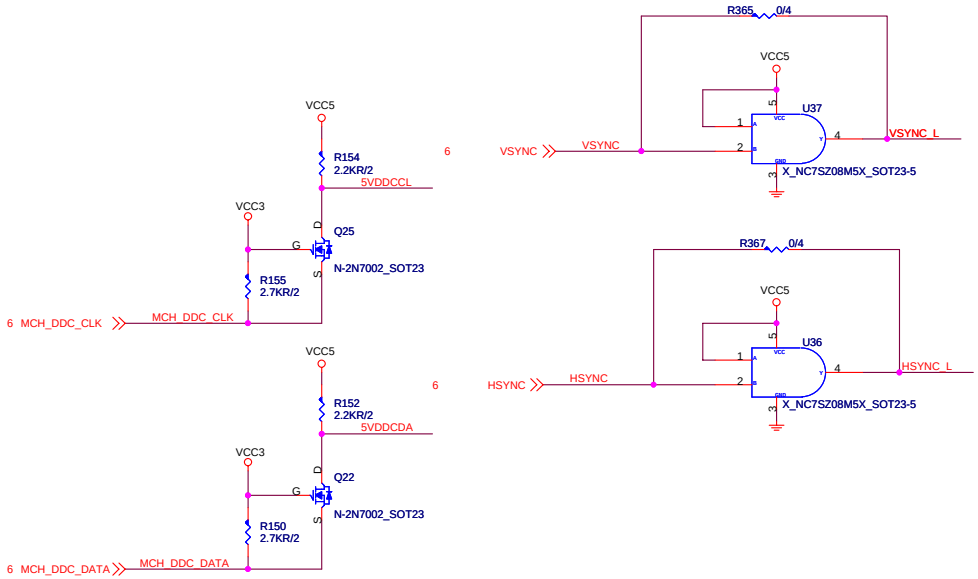
MS-7345

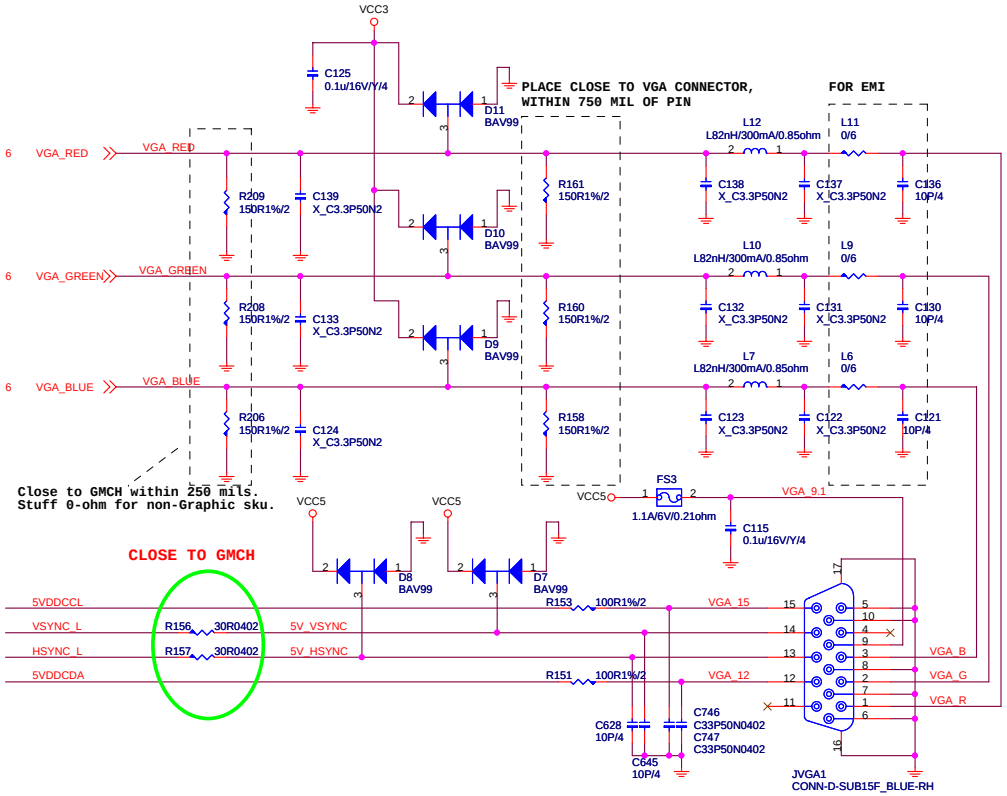
Size	Document Description	Rev
Custom	Clock Gen ICS9LPRS906	1.2

Date: Friday, May 18, 2007 Sheet 15 of 35

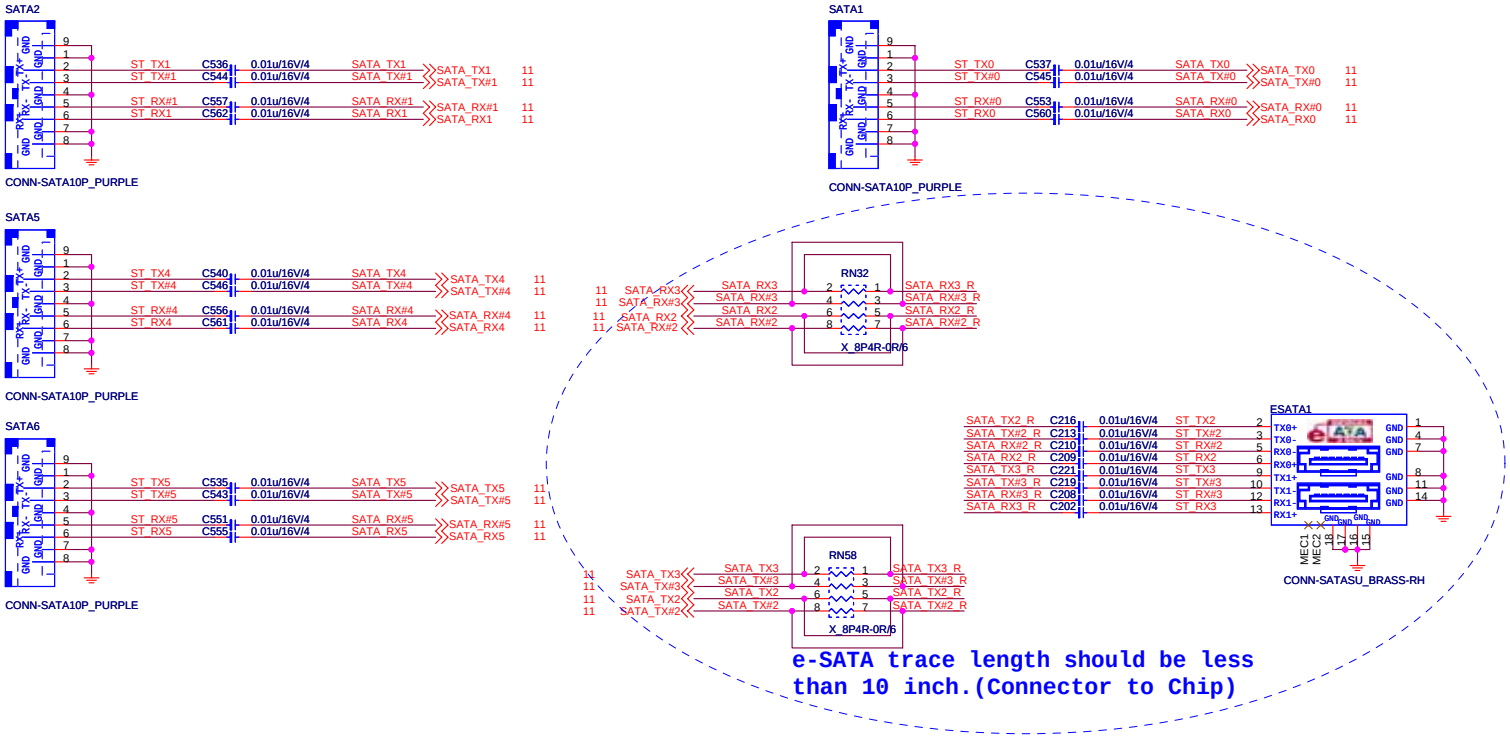

FLOPPY CONNECTOR
SERIAL PORT 1
PS2 KEYBOARD & MOUSE CONNECTOR
Thermal Resistor
IR
LPC I/O STRAPPING RESISTOR
PARALLAL PORT
Non used COM2 must pull high
S I/O STRAP
SPI 1:BACKUP* 0:PRIMARY
SPI 1:DIS 0:EN*
IO ADD 1:4Eh* 0:2Eh
FAN 1:60%* 0:100%
VID 1:VIDO/VIDI* 0:GPIO/VIDIO
FAN 1:PWM FAN 0:LNR FAN*
GPIO | GPIO17 | GPIO23
ALC888 | 1 | 1
ALC888T | 0 | 1
MICRO-STAR INT'L CO.,LTD
MS-7345
SIO-Fintek F17882F/COM
Rev 1.2
Date: Friday, May 18, 2007
Sheet 16 of 35

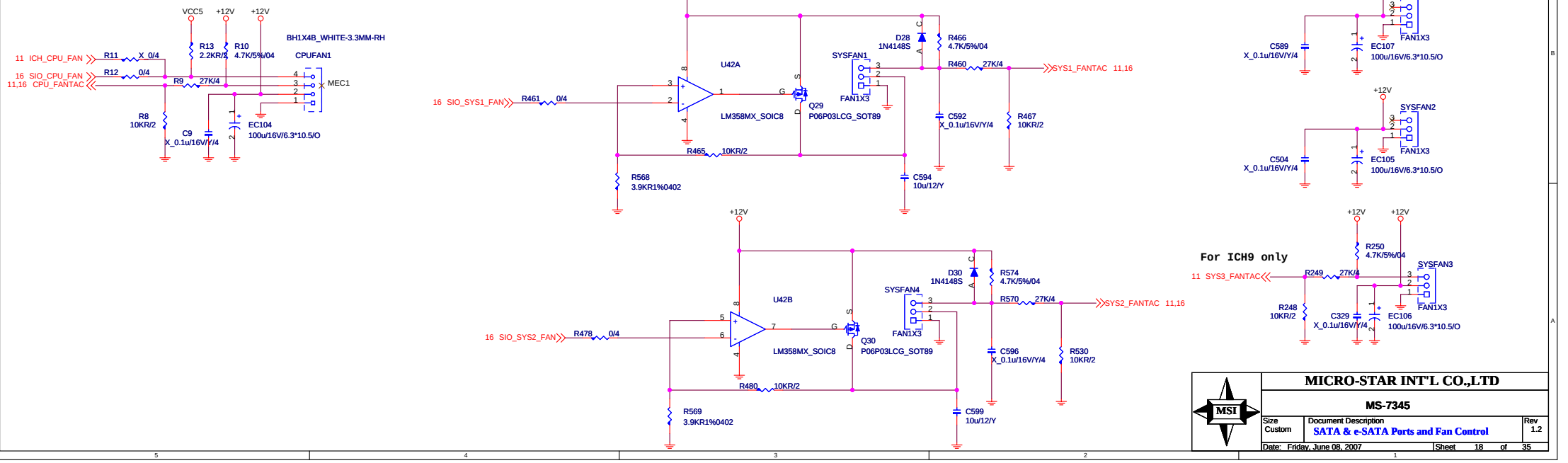
Video Connector



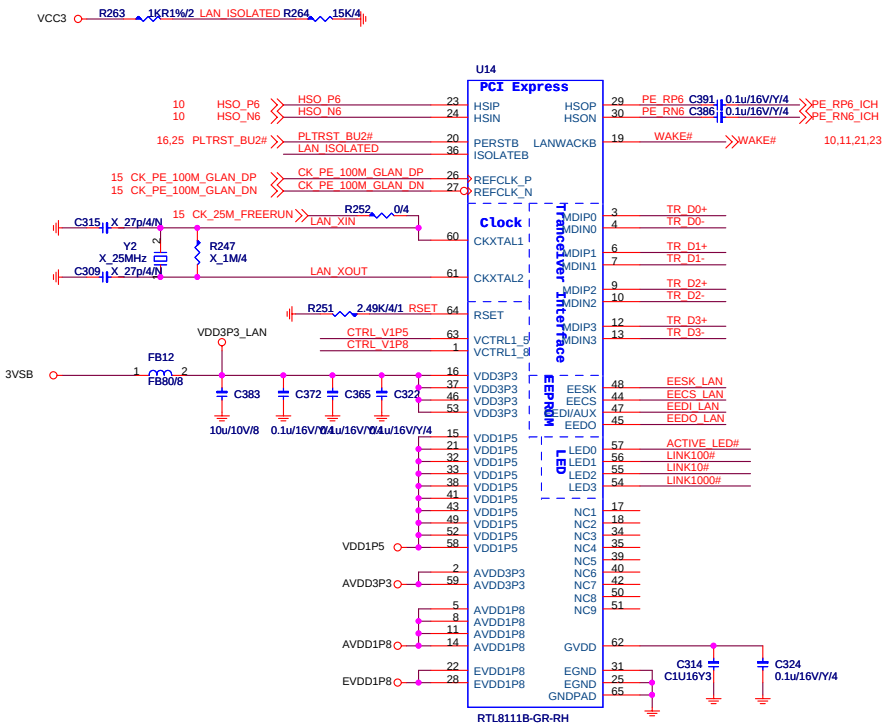


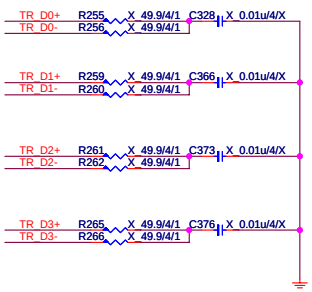
MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7345	
Size: Custom	Document Description: VGA	Rev: 1.2
Date: Friday, May 18, 2007	Sheet 17 of 35	

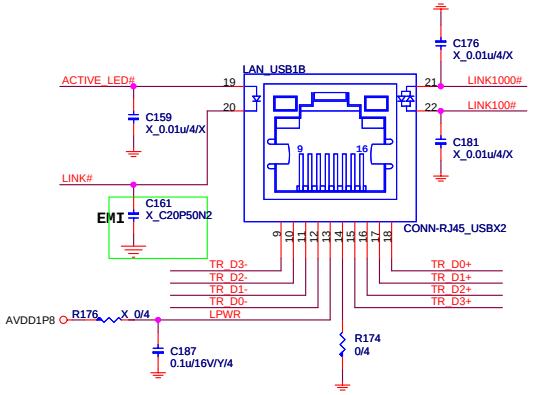


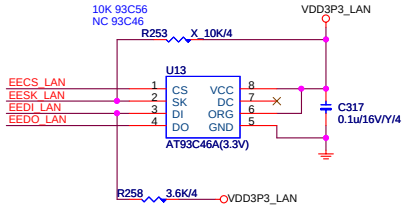


MICRO-STAR INT'L CO.,LTD	
MS-7345	
Size: Custom	Document Description: SATA & e-SATA Ports and Fan Control
Rev: 1.2	
Date: Friday, June 08, 2007	Sheet 18 of 35

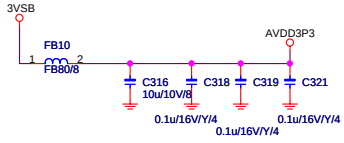


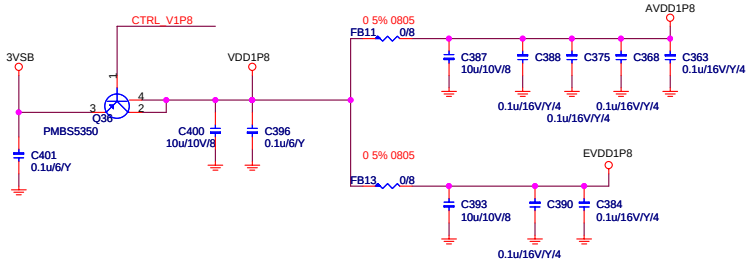


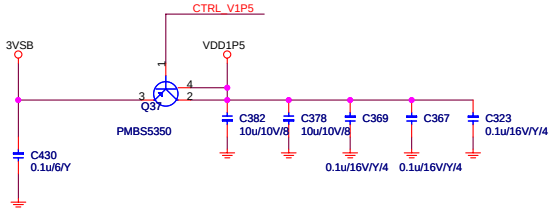




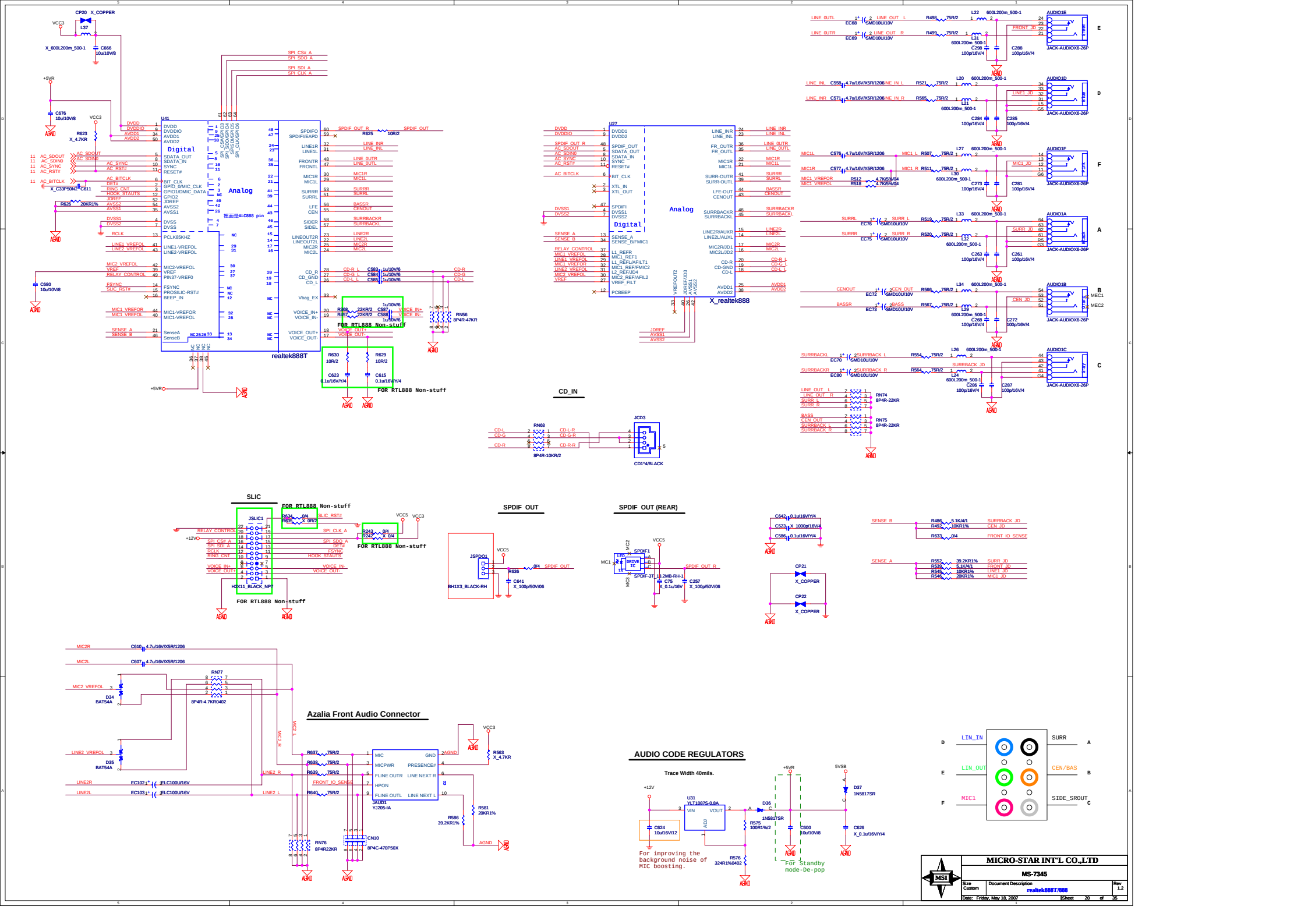
PCIE LAN(RTL8111B) POWER





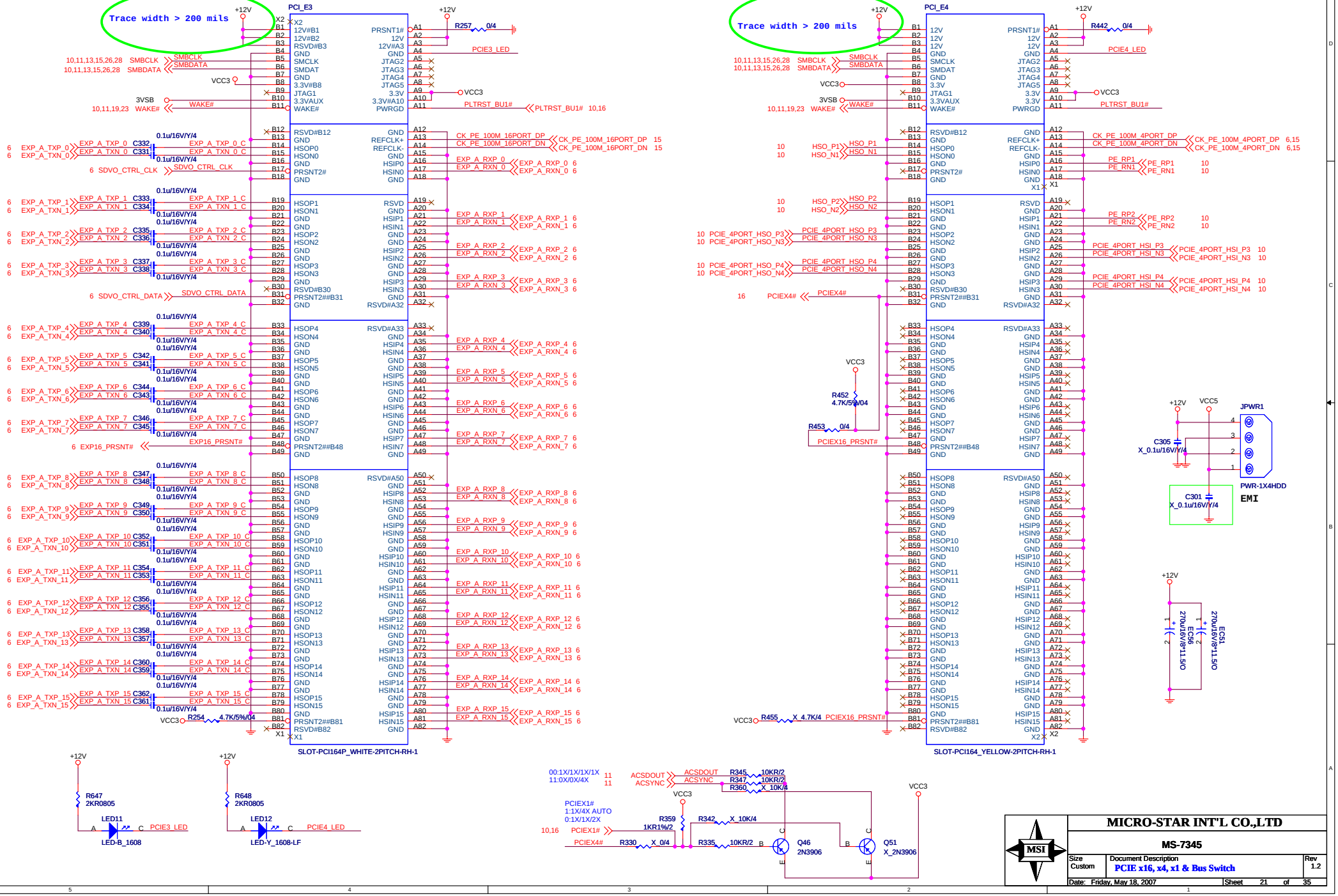


MICRO-STAR INT'L CO.,LTD		
MS-7345		
Size: Custom	Document Description: PCIE_LAN_RTL8111B	Rev: 1.2
Date: Friday, June 08, 2007	Sheet 19 of 35	


realtek888T
Analog
Digital
FOR RTL888 Non-stuff
X_realtek888
CD_IN
SLIC
SPDIF_OUT
SPDIF_OUT (REAR)
Azalia Front Audio Connector
AUDIO CODE REGULATORS
Trace Width 40mils.
For improving the background noise of MIC boosting.
For Standby mode-De-pop
MICRO-STAR INT'L CO.,LTD
MS-7345
realtek888T/888

PCI_Express X16 Slot

PCI_Express X4 Slot
(Share with PCI_E x1 Slots)



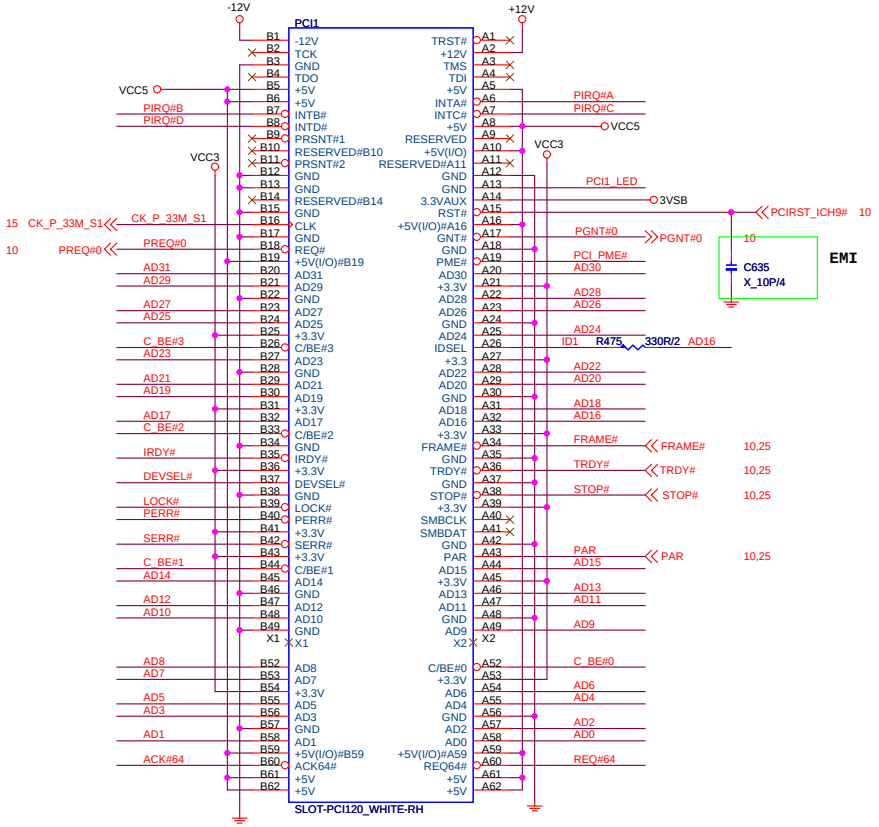
MICRO-STAR INT'L CO.,LTD

MS-7345

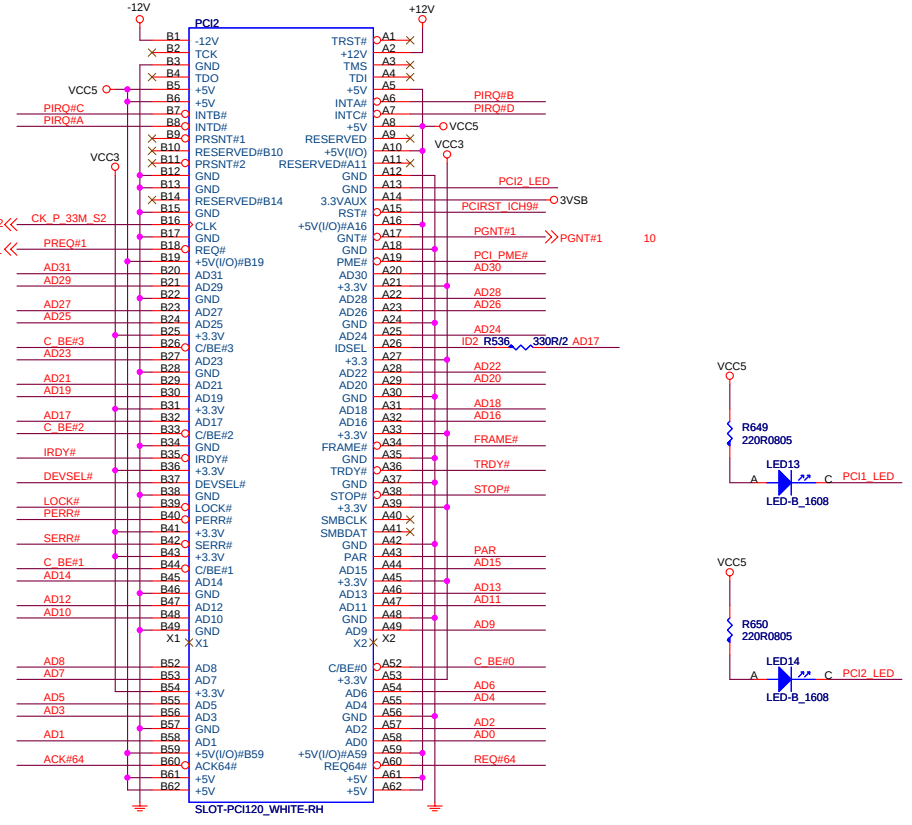
Size: Custom | Document Description: PCIE x16, x4, x1 & Bus Switch | Rev: 1.2

Date: Friday, May 18, 2007 | Sheet 21 of 35

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



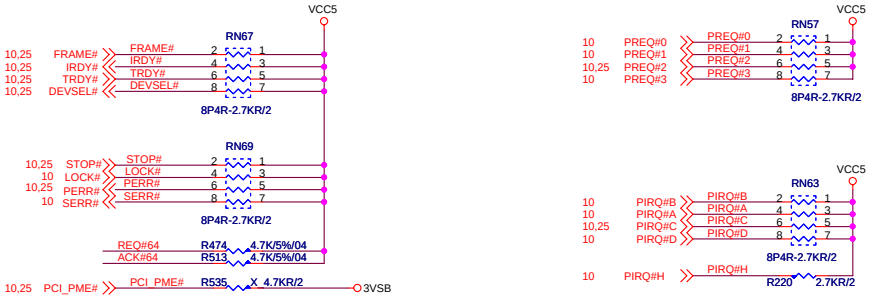
PCI SLOT 2 (PCI VER: 2.2 COMPLY)



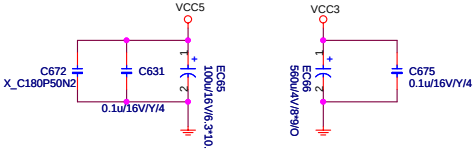
10,25 AD[31..0] AD[31..0]

10,25 C_BE#[3..0] C_BE#[3..0]

PCI PULL-UP / DOWN RESISTORS

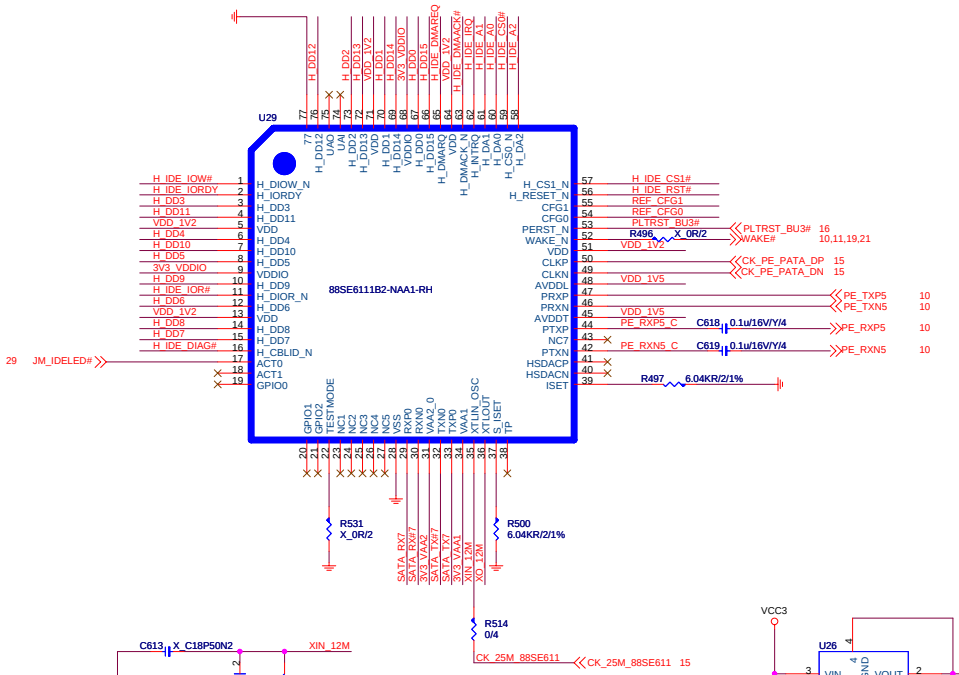


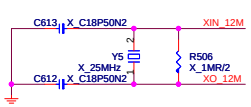
PCI SLOT DECOUPLING CAPACITORS



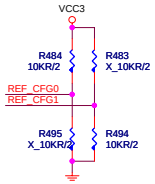
MICRO-STAR INT'L CO.,LTD		
MS-7345		
Size: Custom	Document Description: PCI Slot 1 & 2	Rev: 1.2
Date: Friday, May 18, 2007	Sheet 22 of 35	

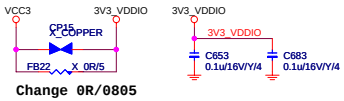
Hi-Speed PCIE to SATA/PATA Bridge





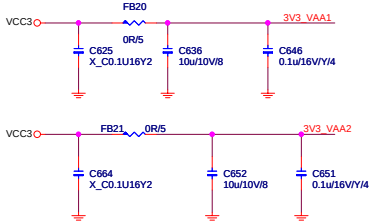
REF_CFG[1:0] =
00:20MHz
01:25MHz

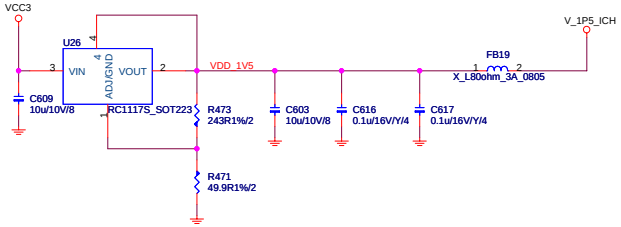


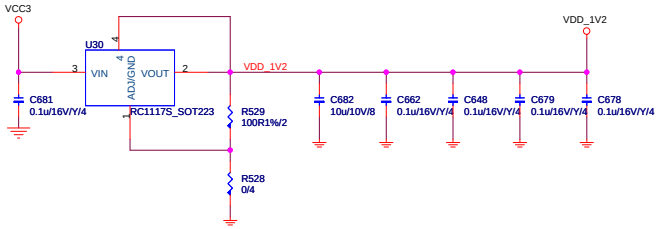


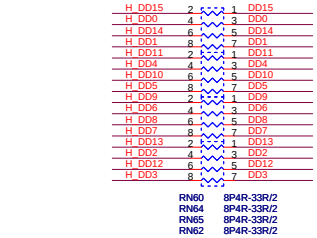
Change 0R/0805

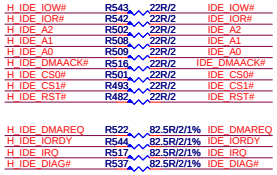
L02-8008074-J07 FOR BEAD

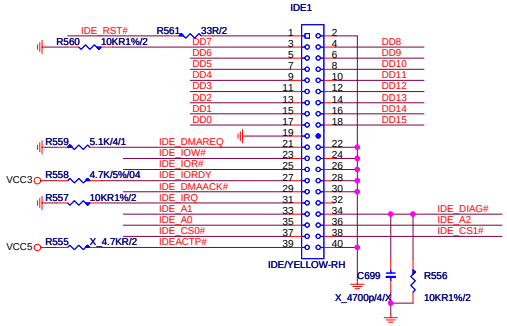


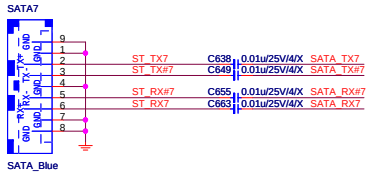










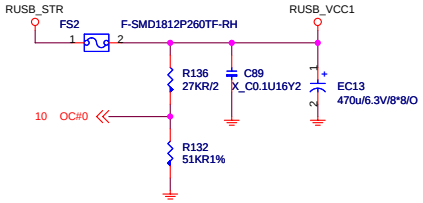


MICRO-STAR INT'L CO.,LTD	
MS-7345	
Size: Custom	Document Description: Marvell 88SE6111 PCIE to PATA/SATA
Rev: 1.2	
Date: Friday, May 18, 2007	Sheet 23 of 35

Rear USB Connector

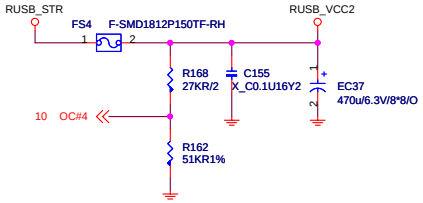
USB POWER FOR PORT 0,3,4,5

NEAR CONNECTOR

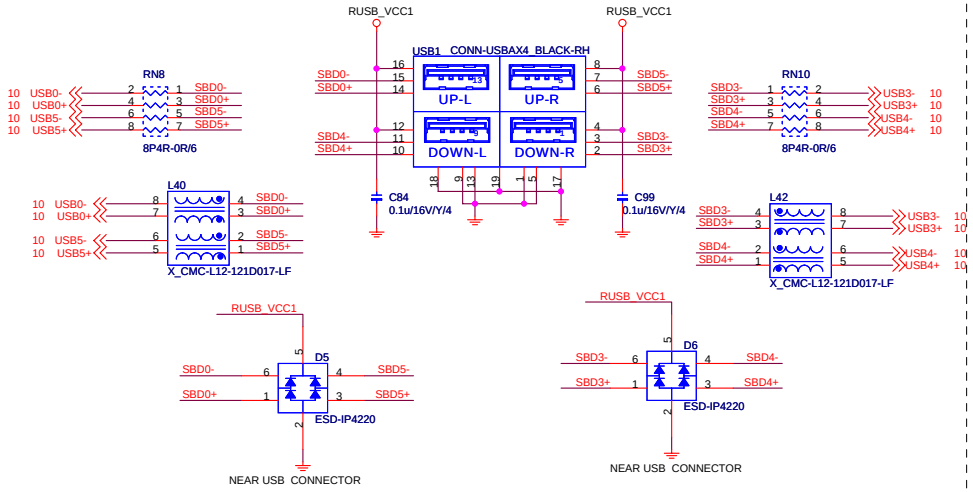


USB POWER FOR PORT 1,2

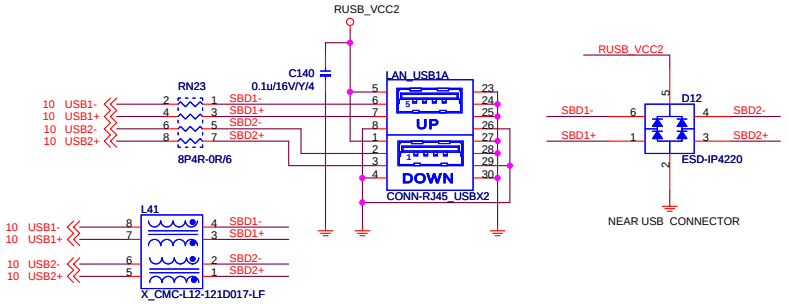
NEAR CONNECTOR



REAR USB PORT 0,3,4,5 (2x2)



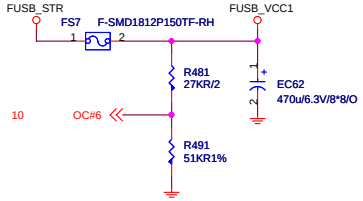
REAR USB PORT 1,2 (With LAN)



Front USB Connector

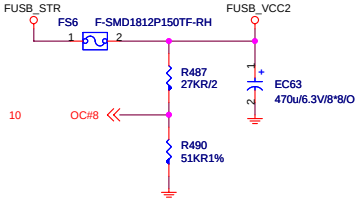
USB POWER FOR PORT 6,7

NEAR CONNECTOR



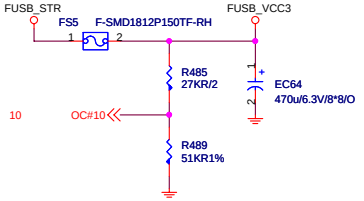
USB POWER FOR PORT 6,7

NEAR CONNECTOR

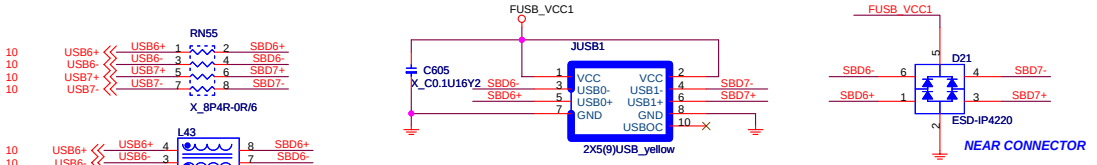


USB POWER FOR PORT 6,7

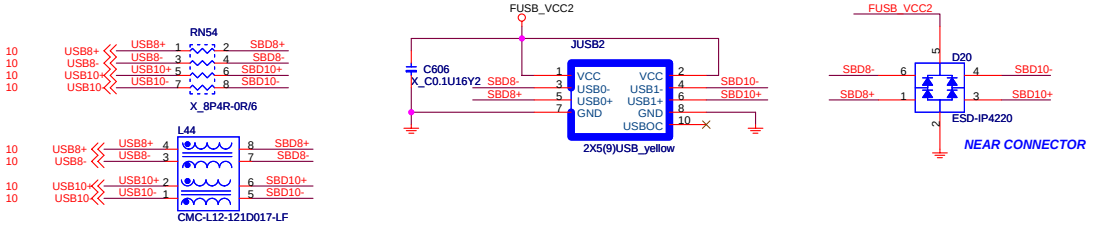
NEAR CONNECTOR



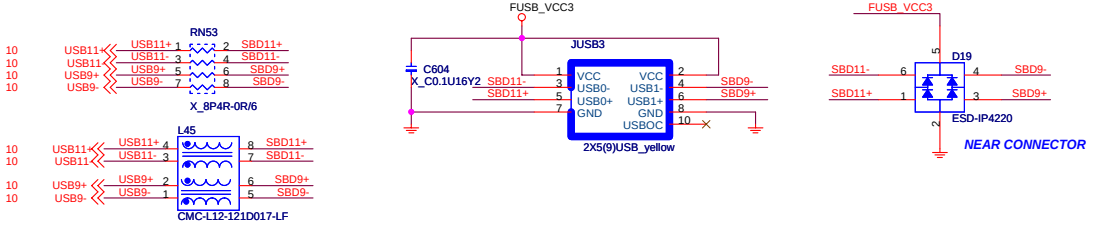
FRONT USB PORT 6,7



FRONT USB PORT 8,9

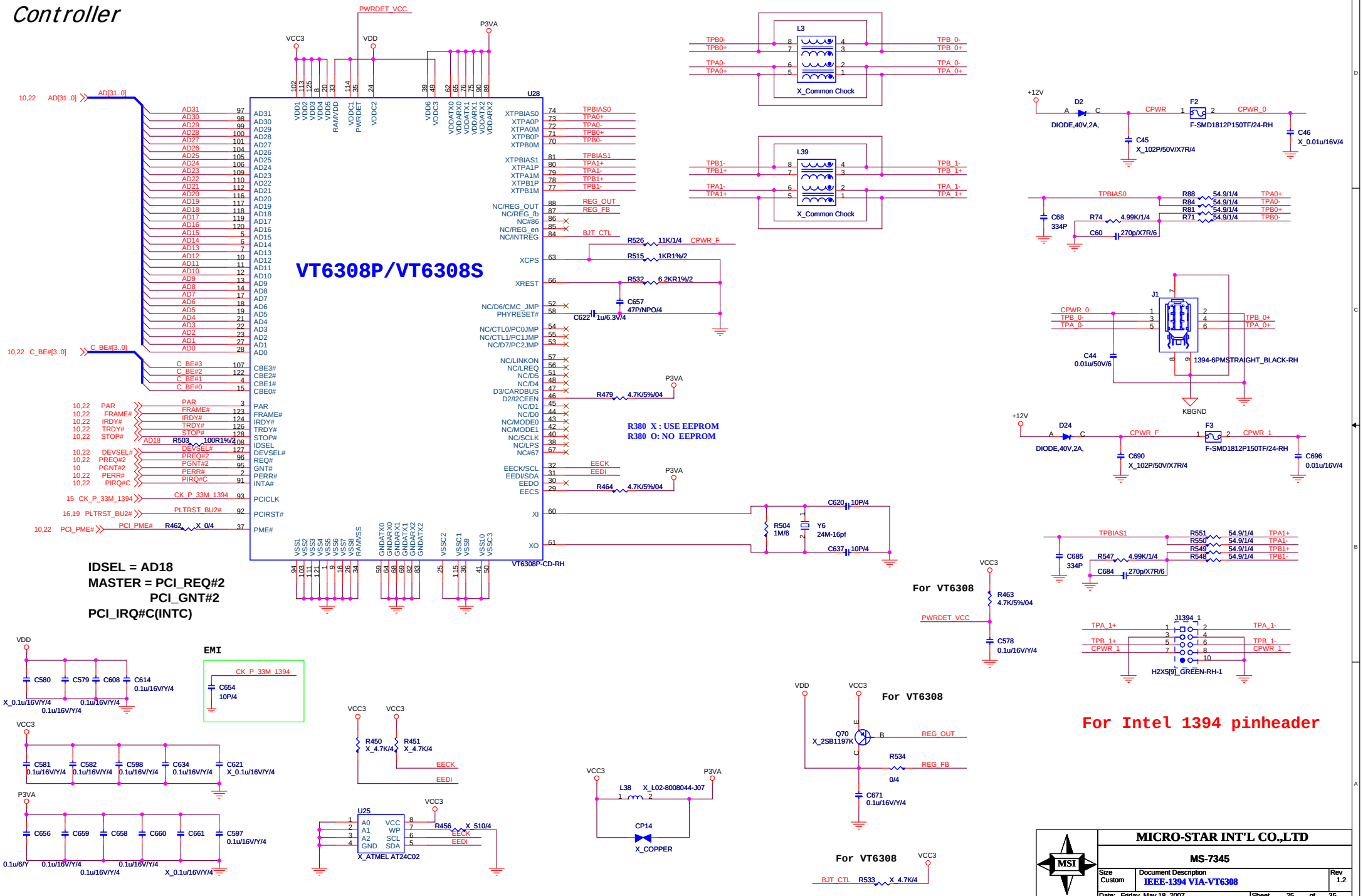


FRONT USB PORT 10,11

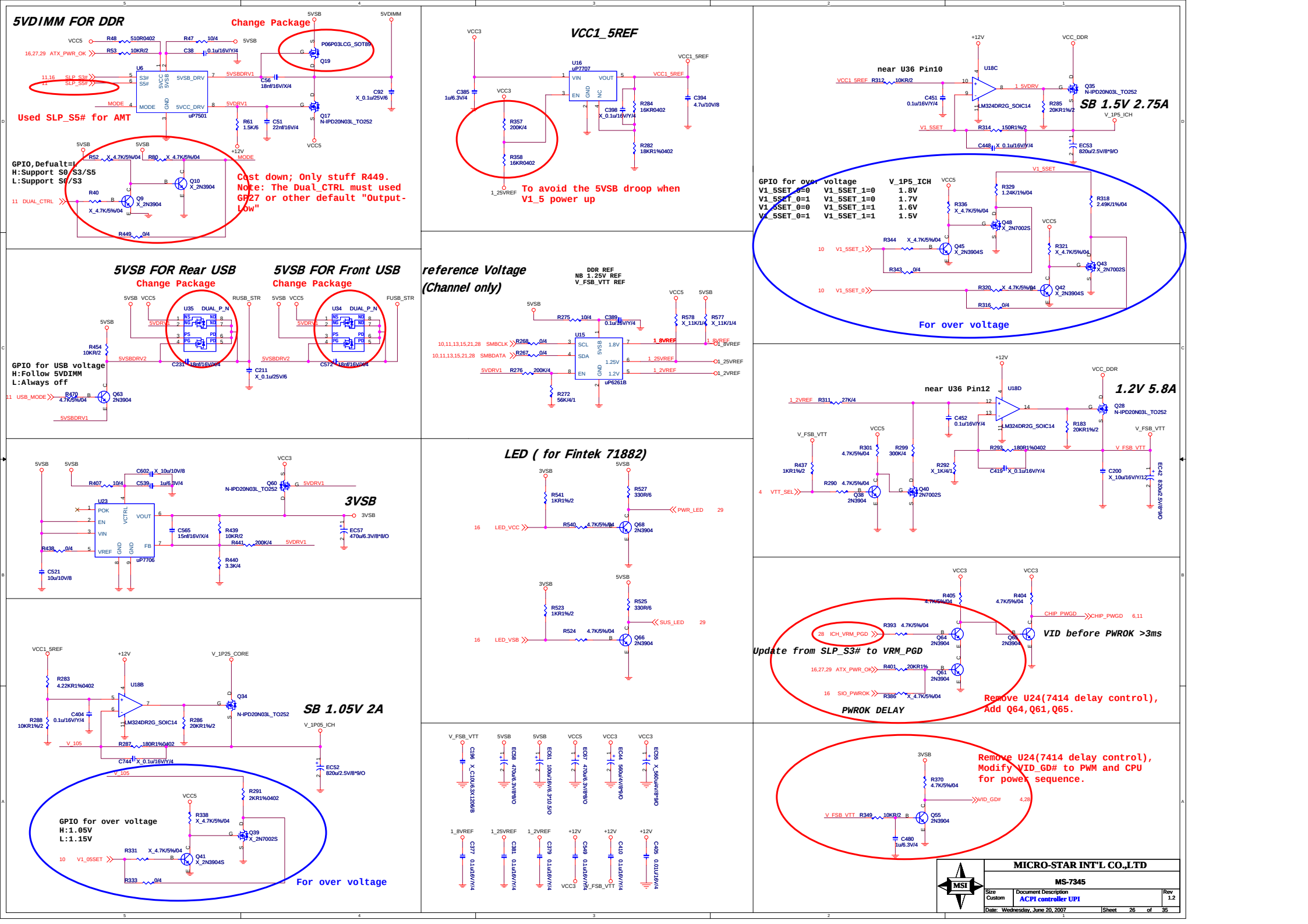


MICRO-STAR INT'L CO.,LTD		
MS-7345		
Size: Custom	Document Description: USB Connector	Rev: 1.2
Date: Tuesday, June 26, 2007	Sheet 24 of 35	

1394a OHCI Link Layer Controller



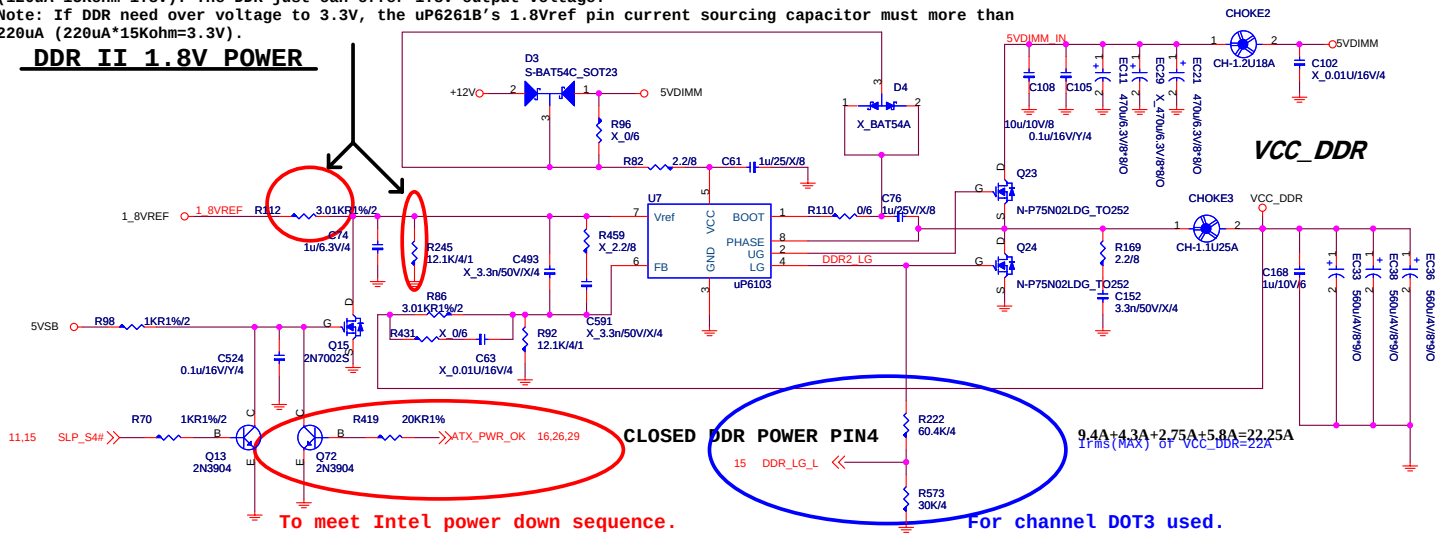
MICRO-STAR INT'L CO.,LTD	
MS-7345	
Size: Custom	Document Description: IEEE-1394 VIA-VT6308
Rev: 1.2	
Date: Friday, May 18, 2007	Sheet 25 of 35


5VDIMM FOR DDR
Change Package
Used SLP_S5# for AMT
GPIO,Defualt=L
H:Support S0/S3/S5
L:Support S0/S3
Cost down; Only stuff R449.
Note: The Dual_CTRL must used GPIO27 or other default "Output-Low"
VCC1_5REF
To avoid the 5VSB droop when V1_5 power up
near U36 Pin10
SB 1.5V 2.75A
GPIO for over voltage
V1_5SET_0=0 V1_5SET_1=0 1.8V
V1_5SET_0=1 V1_5SET_1=0 1.7V
V1_5SET_0=0 V1_5SET_1=1 1.6V
V1_5SET_0=1 V1_5SET_1=1 1.5V
V_1P5_ICH
For over voltage
5VSB FOR Rear USB
Change Package
5VSB FOR Front USB
Change Package
GPIO for USB voltage
H:Follow 5VDIMM
L:Always off
reference Voltage
(Channel only)
DDR REF
NB 1.25V REF
V_FSB_VTT REF
near U36 Pin12
1.2V 5.8A
3VSB
LED (for Fintek 71882)
Update from SLP_S3# to VRM_PGD
PWROK DELAY
VID before PWROK >3ms
Remove U24(7414 delay control), Add Q64,Q61,Q65.
SB 1.05V 2A
GPIO for over voltage
H:1.05V
L:1.15V
For over voltage
Remove U24(7414 delay control), Modify VID_GD# to PWM and CPU for power sequence.
MICRO-STAR INT'L CO.,LTD
MS-7345
ACPI controller UPI
Rev 1.2
Wednesday, June 20, 2007
Sheet 26 of 35

The uP6261B 1.8Vref output connect a resistance =15K ohm that sourcing current must more than 120uA (120uA*15Kohm=1.8V). The DDR just can offer 1.8V output voltage.
Note: If DDR need over voltage to 3.3V, the uP6261B's 1.8Vref pin current sourcing capacitor must more than 220uA (220uA*15Kohm=3.3V).

Iripple=21*0.6*0.8/1=10.08A
2.22*3*1.7=11.322A>10.08A

DDR II 1.8V POWER

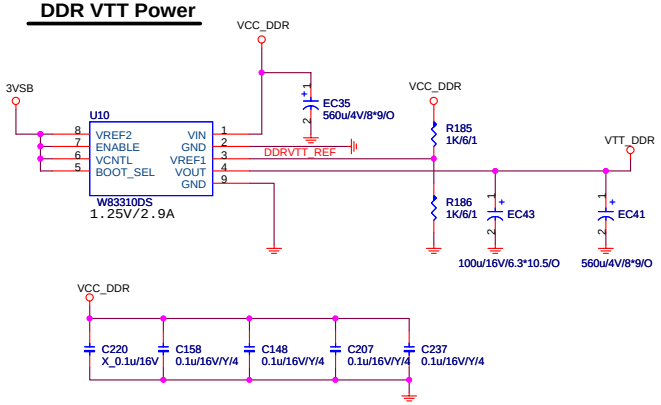


To meet Intel power down sequence.

For channel DOT3 used.

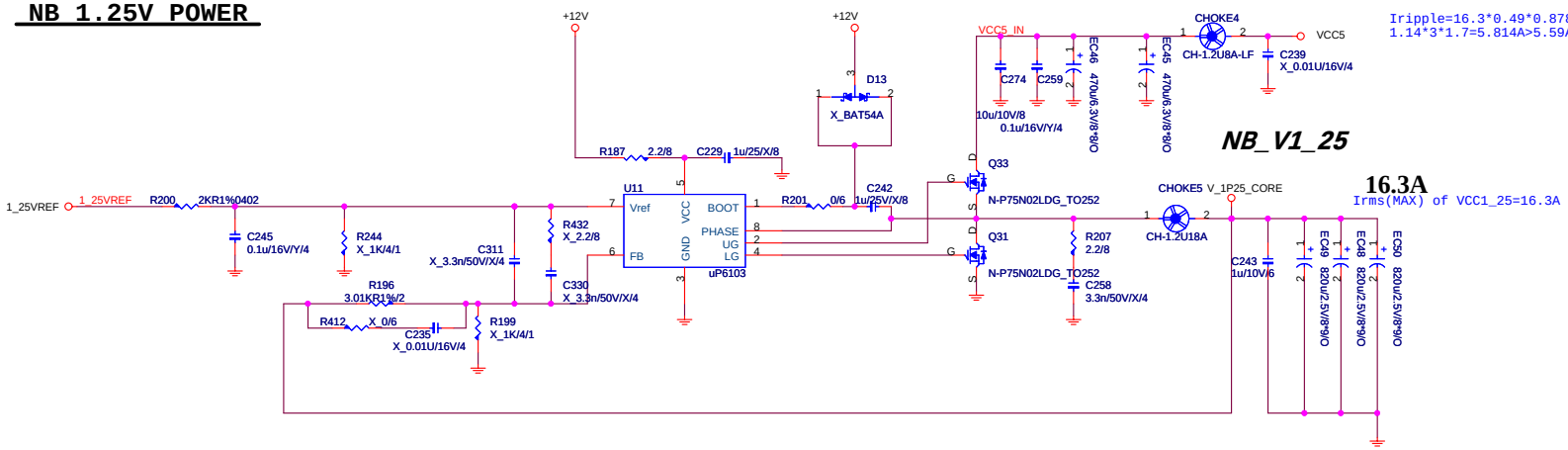
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

DDR VTT Power



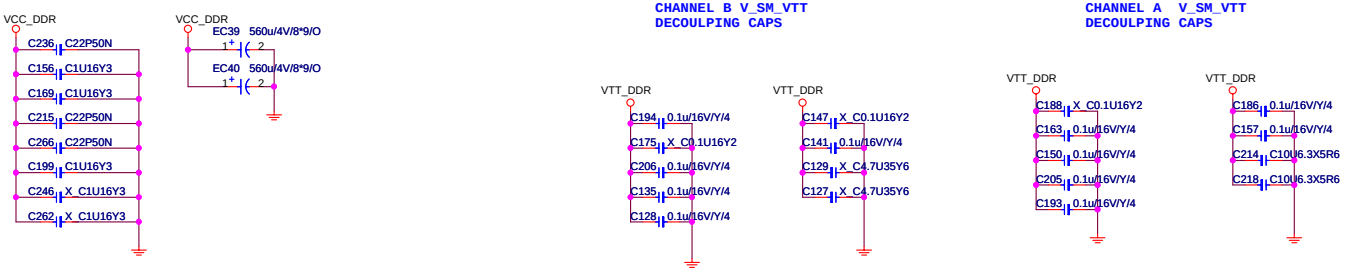
de- VCC_DDR high frequency noise.

NB 1.25V POWER

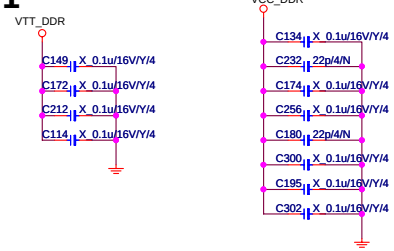


Iripple=16.3*0.49*0.878/1=7A
1.14*3*1.7=5.814A>5.59A

16.3A
Irms(MAX) of VCC1_25=16.3A



For EMI

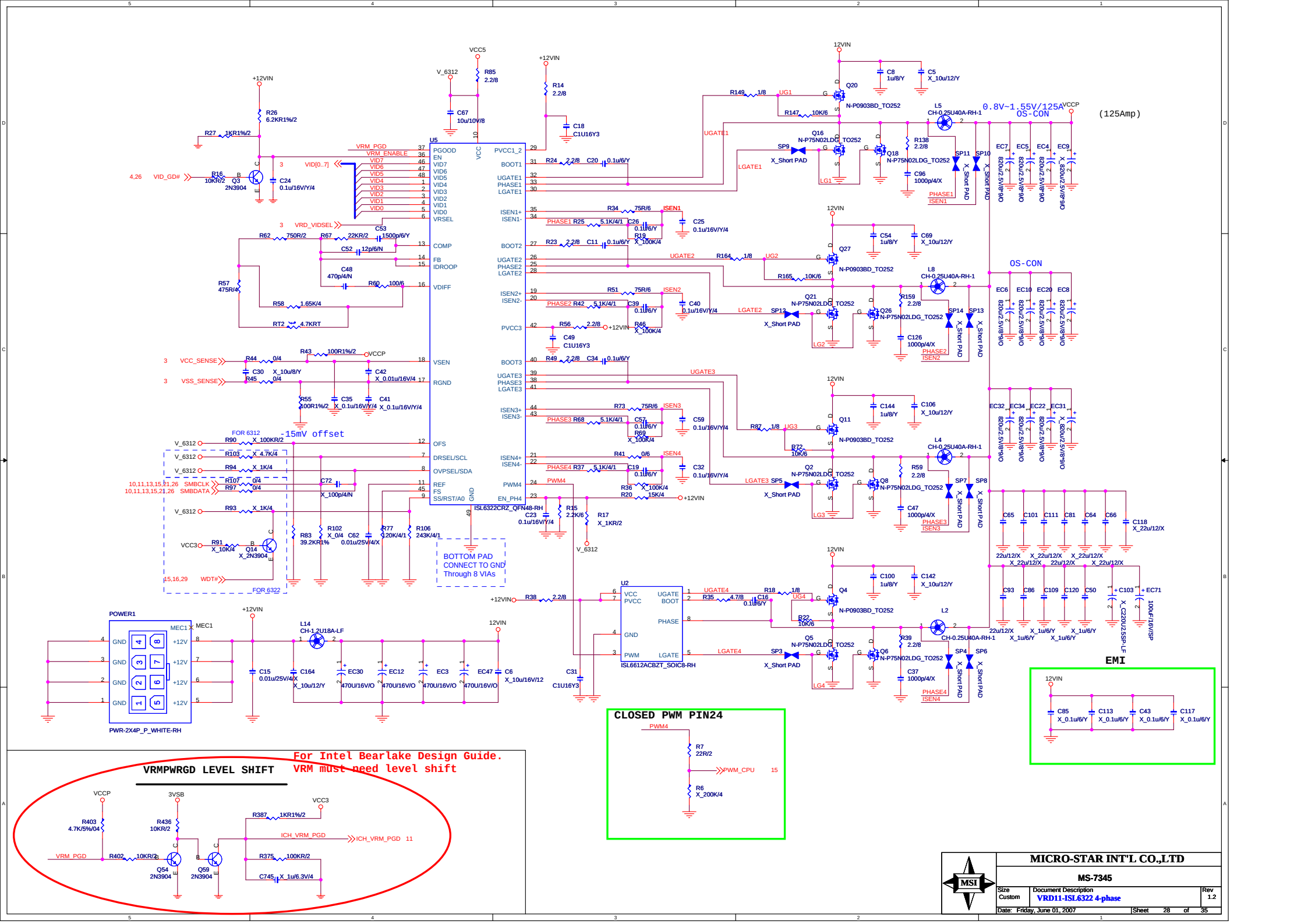


MICRO-STAR INT'L CO.,LTD

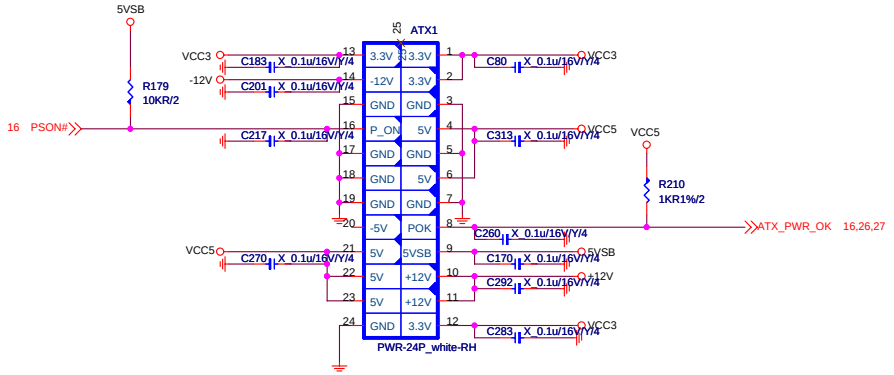
MS-7345

Size	Document Description	Rev
Custom	NB Core Power & DDR Power	1.2

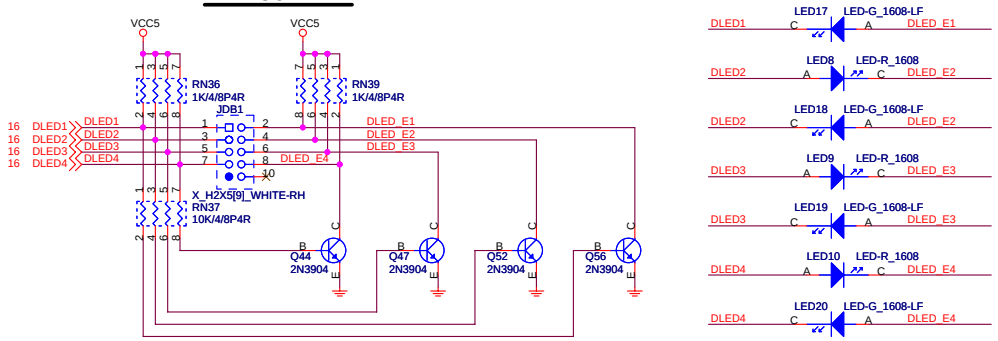
Date: Wednesday, June 20, 2007 Sheet 27 of 35


U5
ISL6322CRZ_QFN48-RH
U2
ISL6612ACBZT_SOIC8-RH
POWER1
PWR-2X4P_P_WHITE-RH
0.8V~1.55V/125A
(125Amp)
OS-CON
EMI
-15mV offset
FOR 6312
FOR 6322
BOTTOM PAD
CONNECT TO GND
Through 8 VIAs
CLOSED PWM PIN24
VRMPWRGD LEVEL SHIFT
For Intel Bearlake Design Guide.
VRM must need level shift
MICRO-STAR INT'L CO.,LTD
MS-7345
VRD11-ISL6322 4-phase
Date: Friday, June 01, 2007
Sheet 28 of 35
Rev 1.2

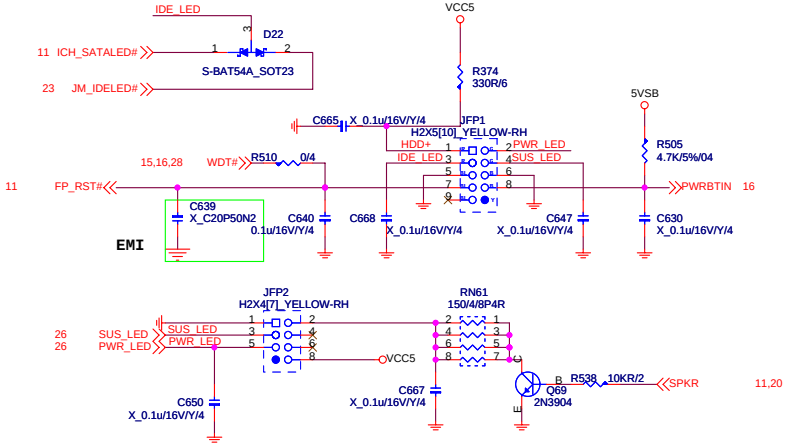
ATX POWER CONNECTOR



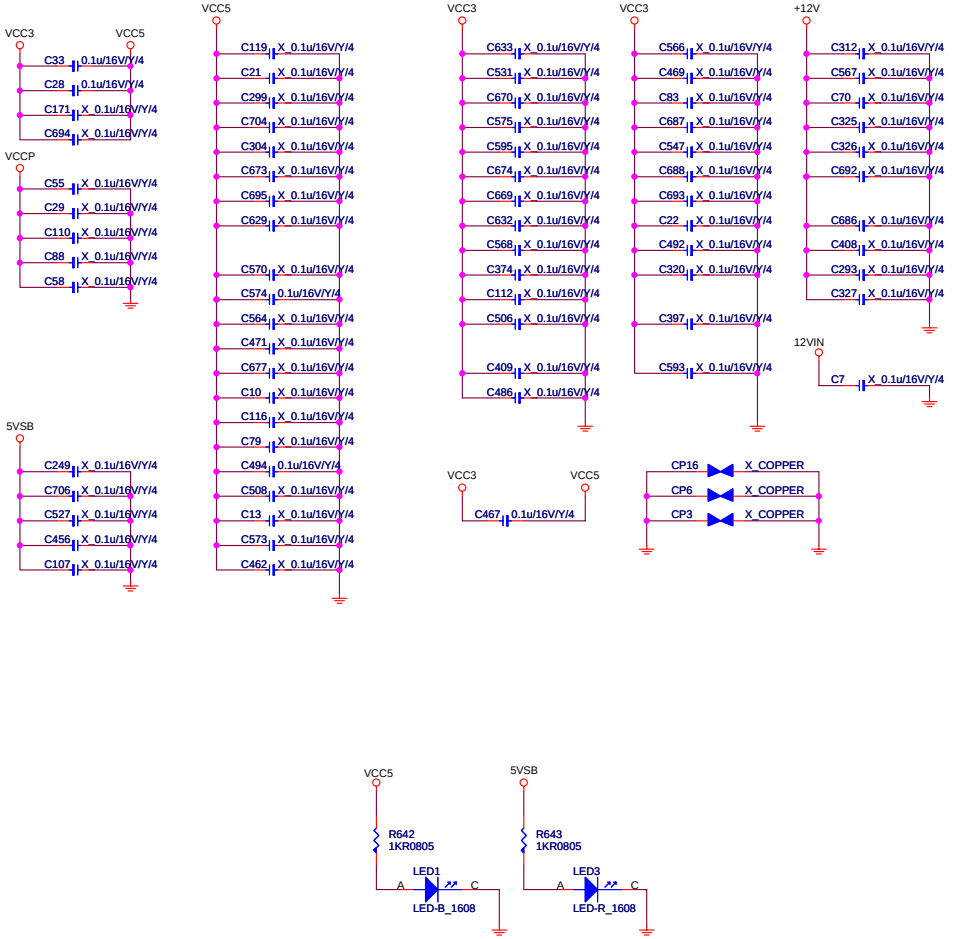
DEBUG LED



FRONT PANNEL



Cap. for EMI & Power



MICRO-STAR INT'L CO.,LTD	
MS-7345	
Size: Custom	Document Description: ATX PWR-Connector & Front Panel & EMI
Rev: 1.2	
Date: Friday, May 18, 2007	Sheet 29 of 35

Option : cfg-7345-GT(601-7345-02S)
1.INTEL G33 cfg-7345-GT(601-7345-07S(PCB1.1))
2.ICH9R cfg-7345-GT(601-7345-050(PCB1.1))
3.Audio RTL888T

Option : cfg-7345-G(601-7345-01S)
1.INTEL G33 cfg-7345-G(601-7345-06S(PCB1.1))
2.ICH9R
3.Audio RTL888

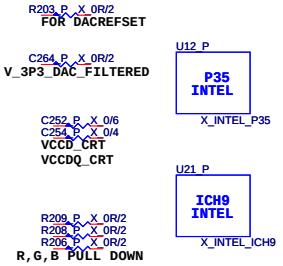
Option : cfg-7345-PT(601-7345-04S)
1.INTEL P35 cfg-7345-PT(601-7345-09S(PCB1.1))
2.ICH9R MP BOM:cfg-7345-PT(601-7345-070(PCB1.1))
3.Audio RTL888T

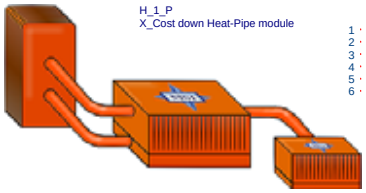
Option : cfg-7345-P(601-7345-03S)
1.INTEL P35 cfg-7345-P(601-7345-08S(PCB1.1))
2.ICH9R MP BOM:cfg-7345-P(601-7345-010(PCB1.1))
3.Audio RTL888

Option : cfg-7345-PCD(601-7345-05S)
Cost down
1.INTEL P35 cfg-7345-PCD(601-7345-10S(PCB1.1))
2.ICH9 cfg-7345-PCD(601-7345-020(PCB1.1))
3.Audio RTL888
4.北橋,南橋 Kwoger heatsink
5.Remove 後IO 的 SPDIF OUT

Option : cfg-7345-PCDH
Cost down(PCB1.1)
1.INTEL P35 cfg-7345-PCDH(601-7345-030(PCB1.1))
2.ICH9R
3.Audio RTL888
4.北橋,南橋Cost down Heat-Pipe module
5.Remove 1394
6.Remove 後IO 的 SPDIF OUT

Option Parts

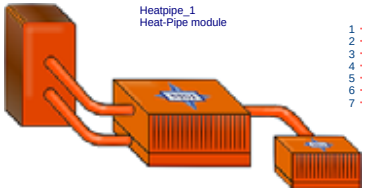




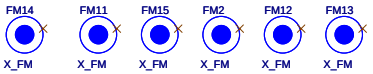
業務需求: 新增P35 Neo2-FIR BOM (PCB 1.1)
(1).7345_11_0524_FIR.ECR跟7345_11_FIR.avl for 601-7345-010.(New BOM)
1.remove rear Spdif out
2.remove E31-0800340-A21(CIRCU-PIPE)
3.add E31-0800341-A21(COST DOWN PIPE)會另發MP minor change 文做備註
cfg-7345-FIR(601-7345-040(PCB1.1))

MS-7345 業務需求 請增加新BOM (G33+ICH9R+ALC888)
1) 根據601-7345-050 (G33 Platinum) 去修改, 可直接出文.
2) Remove ALC888T function
3) Add ALC888 function cfg-7345-GG(601-7345-060(PCB1.1))
4) Remove VOIP connector
5) PM 會發MP minor change 備註

PD0-0734512-D05,昆穎(定穎大陸),
PD0-0734512-Y34,元茂

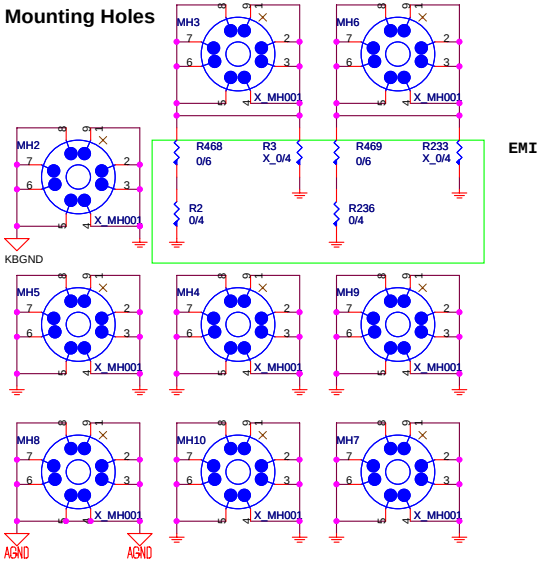


Optical Fiducial Marks-120

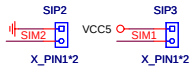


Optical Fiducial Marks-100

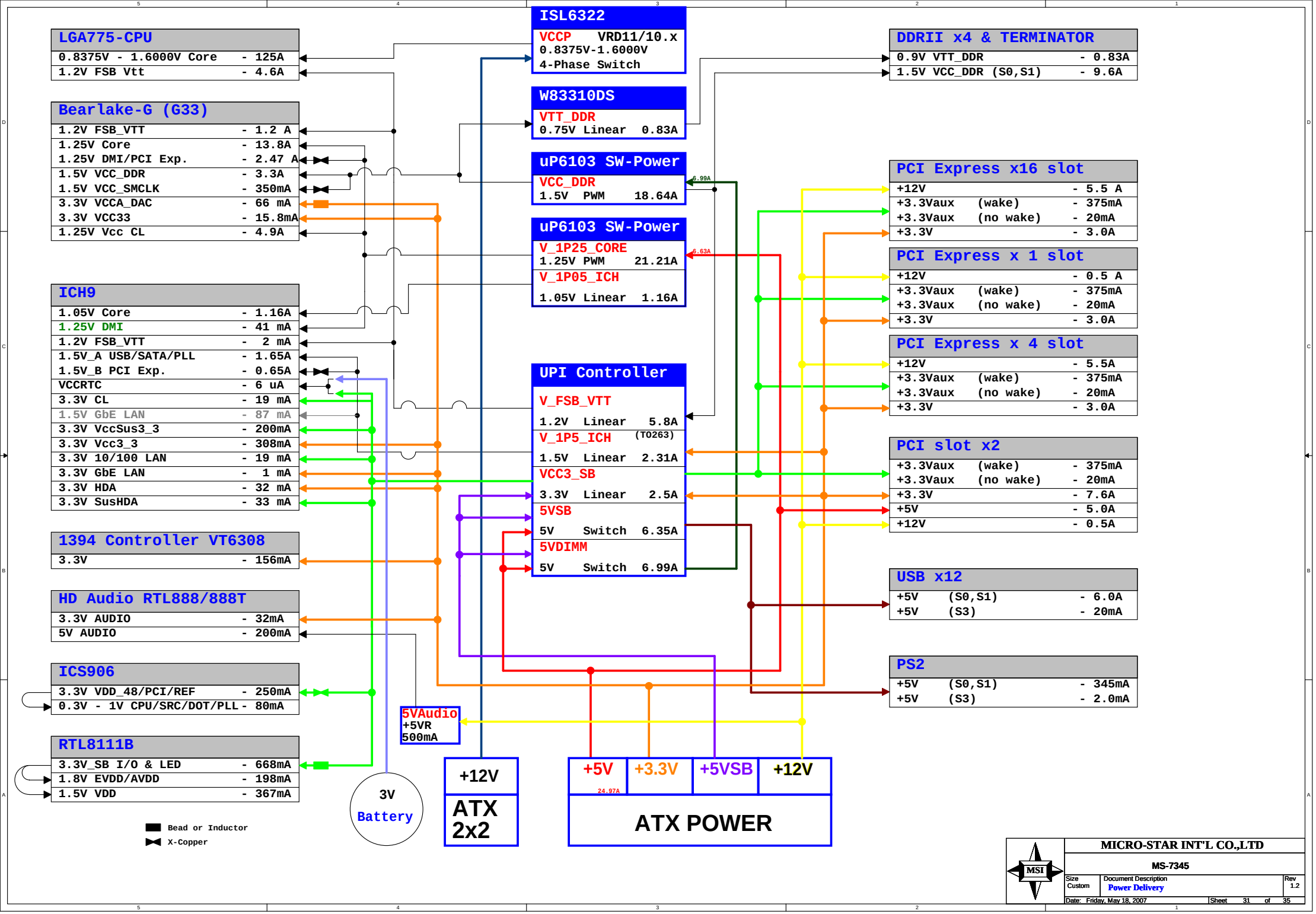
Mounting Holes



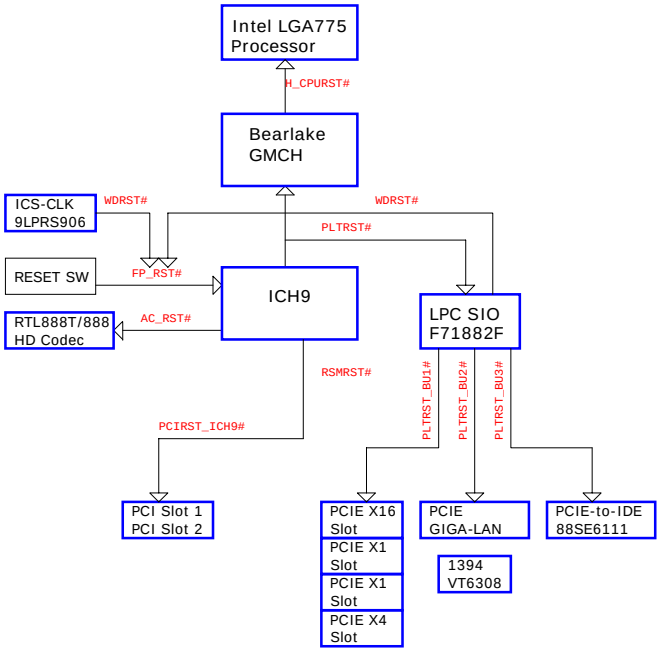
Simulation



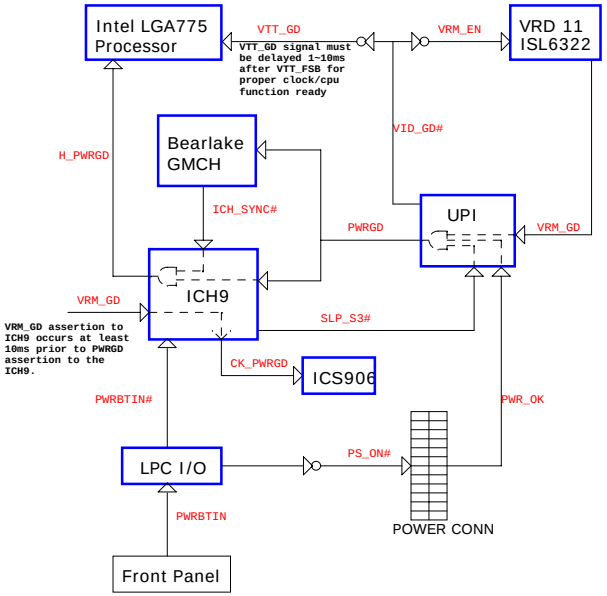
MICRO-STAR INT'L CO.,LTD	
MS-7345	
Size: Custom	Document Description: Manual Parts & Option Parts
Rev: 1.2	
Date: Tuesday, June 26, 2007	Sheet 30 of 35


LGA775-CPU
0.8375V - 1.6000V Core - 125A
1.2V FSB Vtt - 4.6A
Bearlake-G (G33)
1.2V FSB_VTT - 1.2 A
1.25V Core - 13.8A
1.25V DMI/PCI Exp. - 2.47 A
1.5V VCC_DDR - 3.3A
1.5V VCC_SMCLK - 350mA
3.3V VCCA_DAC - 66 mA
3.3V VCC33 - 15.8mA
1.25V Vcc CL - 4.9A
ICH9
1.05V Core - 1.16A
1.25V DMI - 41 mA
1.2V FSB_VTT - 2 mA
1.5V_A USB/SATA/PLL - 1.65A
1.5V_B PCI Exp. - 0.65A
VCCRTC - 6 uA
3.3V CL - 19 mA
1.5V GbE LAN - 87 mA
3.3V VccSus3_3 - 200mA
3.3V Vcc3_3 - 308mA
3.3V 10/100 LAN - 19 mA
3.3V GbE LAN - 1 mA
3.3V HDA - 32 mA
3.3V SusHDA - 33 mA
1394 Controller VT6308
3.3V - 156mA
HD Audio RTL888/888T
3.3V AUDIO - 32mA
5V AUDIO - 200mA
ICS906
3.3V VDD_48/PCI/REF - 250mA
0.3V - 1V CPU/SRC/DOT/PLL - 80mA
RTL8111B
3.3V_SB I/O & LED - 668mA
1.8V EVDD/AVDD - 198mA
1.5V VDD - 367mA
Bead or Inductor
X-Copper
ISL6322
VCCP VRD11/10.x
0.8375V-1.6000V
4-Phase Switch
W83310DS
VTT_DDR
0.75V Linear 0.83A
uP6103 SW-Power
VCC_DDR
1.5V PWM 18.64A
6.99A
uP6103 SW-Power
V_1P25_CORE
1.25V PWM 21.21A
6.63A
V_1P05_ICH
1.05V Linear 1.16A
UPI Controller
V_FSB_VTT
1.2V Linear 5.8A
V_1P5_ICH (TO263)
1.5V Linear 2.31A
VCC3_SB
3.3V Linear 2.5A
5VSB
5V Switch 6.35A
5VDIMM
5V Switch 6.99A
5VAudio
+5VR
500mA
3V
Battery
+12V
ATX
2x2
+5V
24.97A
+3.3V
+5VSB
+12V
ATX POWER
DDRII x4 & TERMINATOR
0.9V VTT_DDR - 0.83A
1.5V VCC_DDR (S0,S1) - 9.6A
PCI Express x16 slot
+12V - 5.5 A
+3.3Vaux (wake) - 375mA
+3.3Vaux (no wake) - 20mA
+3.3V - 3.0A
PCI Express x 1 slot
+12V - 0.5 A
+3.3Vaux (wake) - 375mA
+3.3Vaux (no wake) - 20mA
+3.3V - 3.0A
PCI Express x 4 slot
+12V - 5.5A
+3.3Vaux (wake) - 375mA
+3.3Vaux (no wake) - 20mA
+3.3V - 3.0A
PCI slot x2
+3.3Vaux (wake) - 375mA
+3.3Vaux (no wake) - 20mA
+3.3V - 7.6A
+5V - 5.0A
+12V - 0.5A
USB x12
+5V (S0,S1) - 6.0A
+5V (S3) - 20mA
PS2
+5V (S0,S1) - 345mA
+5V (S3) - 2.0mA
MICRO-STAR INT'L CO.,LTD
MS-7345
Size Custom
Document Description
Power Delivery
Rev 1.2
Date: Friday, May 18, 2007
Sheet 31 of 35

RESET MAP



PWROK MAP



12V

5V

3.3V

1.5VREF

NB 1.25V Core

VDDR

SB 1.5V

V_FSB_VTT

VID_GD

VTT_PWGD

VRM_EN

CPU VCore

VRMGD to SB

CK_PGD

CHIP_GD

PL_RST

PCI_RST

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7345	
Size: Custom	Document Description: Reset Map & PWROK Map	Rev: 1.2
Date: Friday, May 18, 2007	Sheet 32 of 35	

ICH8

GPIO	Alt Func	I/O/NC	Power	Tol	Default	Signal Name
GPIO[0]	BM_BUSY#	I/O	Core	3.3V	GPI	
GPIO[1]	TACH1	I/O	Core	3.3V	GPI	SYS1_FANTAC
GPIO[5:2]	PIRQ[H:E]#	I/OD	Core	5V	GPI	PIRQ#[H:E]
GPIO[7:6]	TACH[3:2]	I/O	Core	3.3V	GPI	SYS2/3_FANTAC
GPIO[8]	unmuxed	I/O	Resume	3.3V	GPI	
GPIO[9]	WOL_EN	I/O	Resume	3.3V	Native	
GPIO[10]	CLGPIO1	I/O	Resume	3.3V	GPI	
GPIO[11]	SMBALERT#	I/O	Resume	3.3V	Native	
GPIO[12]	unmuxed	I/O	Resume	3.3V	GPO	
GPIO[13]	unmuxed	I/O	Resume	3.3V	GPI	SIO_PME#
GPIO[14]	CLGPIO2	I/O	Resume	3.3V	GPI	
GPIO[15]	unmuxed	I/O	Resume	3.3V	Native	
GPIO[16]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[17]	TACH0	I/O	Core	3.3V	GPI	CPU_FANTAC
GPIO[18]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[19]	SATA1GP	I/O	Core	3.3V	GPI	
GPIO[20]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[21]	SATA0GP	I/O	Core	3.3V	GPI	
GPIO[22]	SCLOCK	I/O	Core	3.3V	GPI	
GPIO[23]	LDRQ1#	I/O	Core	3.3V	Native	
GPIO[24]	CLGPIO0	I/O	Resume	3.3V	GPO	
GPIO[25]	STP_CPU#	I/O	Resume	3.3V	Native	
GPIO[26]	S4_STATE#	I/O	Resume	3.3V	Native	
GPIO[27]	QRT_STATE0	I/O	Resume	3.3V	GPO	
GPIO[28]	QRT_STATE1	I/O	Resume	3.3V	GPO	
GPIO[29]	OC5#	I/O	Resume	3.3V	Native	OC#4
GPIO[30]	OC6#	I/O	Resume	3.3V	Native	OC#6
GPIO[31]	OC7#	I/O	Resume	3.3V	Native	OC#6
GPIO[32]	unmuxed	I/O	Core	3.3V	GPO	SPI_WP#
GPIO[33]	unmuxed	I/O	Core	3.3V	GPO	SPI_HOLD_GPO#
GPIO[34]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[35]	SATACLKREQ#	I/O	Core	3.3V	GPO	
GPIO[36]	SATA2GP	I/O	Core	3.3V	GPI	
GPIO[37]	SATA3GP	I/O	Core	3.3V	GPI	
GPIO[38]	SLOAD	I/O	Core	3.3V	GPI	
GPIO[39]	SDATAOUT0	I/O	Core	3.3V	GPI	
GPIO[43:40]	OC[4:1]#	I/O	Resume	3.3V	Native	OC#0;OC#4
GPIO[47:44]	OC[11:8]#	I/O	Resume	3.3V	Native	OC#8;OC#10
GPIO[48]	SDATAOUT1	I/O	Core	3.3V	GPI	
GPIO[49]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[50]	REQ1#	I/O	Core	5V	Native	PREQ1#
GPIO[51]	GNT1#	I/O	Core	3.3V	Native	PGNT1#
GPIO[52]	REQ2#	I/O	Core	5V	Native	PREQ2#
GPIO[53]	GNT2#	I/O	Core	3.3V	Native	PGNT2#
GPIO[54]	REQ3#	I/O	Core	5V	Native	PREQ3#
GPIO[55]	GNT3#	I/O	Core	3.3V	Native	PGNT3#
GPIO[56]	GLAN_DOCK#	I/O	Resume	3.3V	GPI	
GPIO[57]	CLGPIO5	I/O	Resume	3.3V	GPI	
GPIO[58]	SPI_CS1#	I/O	Resume	3.3V	GPI	SPI_CS1#
GPIO[59]	OC#0	I/O	Resume	3.3V	Native	OC#0
GPIO[60]	LINKALERT#	I/O	Resume	3.3V	Native	

SIO(F71882)

PIN NAME	USAGE	Input/Output	NOTES
GPIO[2:0]	MCH_BSEL2:0]	OUTPUT	PROGRAMED BSEL[2:0] OUTPUT
GPIO3	PCIEX1#	OUTPUT	PROGRAMED X1/X4 OPTION OUTPUT
GPIO4	UNUSED		
GPIO5	UNUSED		
GPIO6	UNUSED		
GPIO7	WDT#	OUTPUT	WATCH DOG TIMER RESET OUTPUT
GPIO10	DLED1	OUTPUT	DEBUG LED OUTPUT 1
GPIO11	UNUSED		
GPIO12	UNUSED		
GPIO13	BEEP	OUTPUT	
GPIO14	UNUSED		
GPIO15	DLED2	OUTPUT	DEBUG LED OUTPUT 2
GPIO16	DLED3	OUTPUT	DEBUG LED OUTPUT 3
GPIO17	UNUSED		
GPIO20	PLTRST_BU#1	OUTPUT	PCI RESTE BUFFER1
GPIO21	PLTRST_BU#2	OUTPUT	PCI RESTE BUFFER2
GPIO22	PLTRST_BU#3	OUTPUT	PCI RESTE BUFFER3
GPIO23	UNUSED		
GPIO24	PWR_OK	INPUT	ATX POWER OK INPUT
GPIO26	PWRBTIN	INPUT	FRONT PANNEL POWER BUTTON
GPIO27	PWRBTN#	OUTPUT	POWER BUTTON BUFFER OUT
GPIO30	SLP_S3#	INPUT	FRONT SOUTBRIDGE S3#
GPIO31	PSON#	OUTPUT	OUTPUT FOR ATX POWER ON
GPIO32	DLED4	OUTPUT	DEBUG LED OUTPUT 4
GPIO33	UNUSED		
GPIO40	SYS2_FANTAC	INPUT	
GPIO41	UNUSED		
GPIO42	IRTX	OUTPUT	
GPIO43	IRRX	INPUT	
VIDIN[2:0]	CPU_BSEL[2:0]	INPUT	CPU BSEL[2:0] INPUT
VIDIN3	UNUSED	INPUT	RESERVED FOR PCIE X4 INDICATION

DDR-II DIMM Config.

DEVICE	ADDRESS	CLOCK	
DIMM 1	00	P/N_DDR0_A	P/N_DDR2_A
DIMM 2	01	P/N_DDR3_A	P/N_DDR5_A
DIMM 3	10	P/N_DDR0_B	P/N_DDR2_B
DIMM 4	11	P/N_DDR3_B	P/N_DDR4_B

PCI Config.

DEVICE	MCP1 INT Pin	REQ# / GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	CK_P_33M_S1
PCI Slot 2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	CK_P_33M_S2
1394	PIRQ#D	PREQ#2 PGNT#2	AD18	CK_P_33M_1394

HW Ver.0A Change to Ver.0B List:
2006/12/23
1/.Remove Q54 and R374and short Q54 B,C pin for power sequence.(page26)
2.U24 power change from VCC3 to 3VSB for power sequence.(page26)
3.Change EC42 from 470u to 820u for V_FSB_VTT power noise.(page26)
4.Change EC52 from 470u to 820u for SB1_05 power noise.(page26)
5.Change EC53 from 470u to 820u for SB1_5 power noise.(page26)
5.CPU_GTLREF resistor value R119 , R115, R128, R104 change from 50ohm to 100ohm for pull-up(intel suggestion)(page4)
6.CPU_GTLREF resistor value R124 , R117 , R141 , R105 change from 100ohm to 200ohm for pull-down.(intel suggestion)(page4)
7.MCH_GTLREF resistor value R190 change from 50ohm to 100ohm for pull-pu.(intel suggestion)(page6)
8.MCH_GTLREF resistor value R195 change from 100ohm to 200ohm for pull-down.(intel suggestion)(page6)
9.SRCOMP[3:0] R223 , R227 , R184 , R182 change from 20ohm to 19.1ohm.(intel suggestion)(page7)
10.DDR2 termination RN16 , RN26 , RN11 , RN14 , RN27 , RN12 , R171 change from 39ohm to 43ohm.(intel suggestion)(page14)
11.Add CK_DOT96_MCH_DP pull-high 1.25V and CK_DOT96_MCH_DN pull-down for non-graphic SKU.(intel suggestion)(page6)
12.RIRQ[H:A] pull-up 2.7Kohm to VCC5.(intel suggestion)(page22)
13.USB have two group [5:0] EHCI#1,[6:11EHCI#2 , please one group to real and one group to front.(intel suggestion)(page24)
14.Audio VREFOUT_E and VREFOUT_F swap.(for schematic error)(page20)
15.Audio BASS and CEN_OUT swap.(for schematic error)(page20)
2007/1/5
1.Update E-SATA SATA_TX0/TX#0 and SATA_RX0/RX#0 swap,SATA_TX1/TX#1 and SATA_RX1/RX#1 swap.(Fix can not find E-SATA HD issue)
(Please update CIS data base new libry,this libry have describe TX and RX pin name)(Page18)
2007/1/9
1.Add VRMPWPGD Circuit level shift for ICH VRMPWRGD.(Intel Design Guide page193)(Page11)
2.Power team Suggest VRD11-ISL6322 14,15,16pin circuit change.(For intel 05B spec)(Page 28)
3.Power team other suggest R62=330ohm,R57=0ohm,RT2=4.7Kohm,R58=1.6Kohm,R83=39.2Kohm.(Page 28)
2007/01/15
1.Q19 change package.(page26)
2.Only stuff R449 for DUAL CTRL.(page26)
3.Q30,Q29 change package to U35.(page26)
4.Q64,Q65 change package to U34.(page26)
5.Add Q17 for avoid the 5VSB droop when V1_5 power up.(page26)
6.Remove U24(7414 delay control), Add Q64,Q61,Q65 and meet intel power sequencing.(page26)
7.Add Q72,R419 to meet intel power down sequence.(page27)
8.Add R222,R573 for DDR DOC.(page27)
9.Add VRM_PGD level shift circuit.(Intel DG)(page 28)
2007/01/17
1.Change UPI 7501 pin6 from SLP_S4# to SLP_S5#,For AMT support.(Page 26)
2.Update CHIP_PWGD circuit. If used SLP_S3# will to fast active low on S0-->S5.(Page 26)
3.VCC1_5VREF used V_1P25_CORE to control UPI 7707 pin3(EN),let V_1P25_CORE and V_1P5_ICH at the same time power up and power down.
(Add R357=200K and R358=27K)(Page 26)
2007/01/26
1.Change clear CMOS from jump to button.(Page11)
2.Add D18 for F71882 IO VBAT power.
3.Change to ICS906 clock GEN.(Page15)
4.F71882 SIN2,DCD2,RI2,CTS2#,DSR2# input pin
add pull high 4.7K to VCC3 when non-used COM2.(Fintek AP note)(Page16)
5.Change VSYNC and HSYNC circuit.(Page17)
6.5VDDCCL and 5VDDCDA pull high VCC5 from 8.2Kohm to 2.2Kohm.
(Fix DDC_CLK and DDC_DATA time issue)(Page17)
7.Add CPUFAN DIP CAP EC104.(Page 18)
8.Add SYSFAN2 DIP CAP EC105.(Page18)
9.Add SYSFAN3 DIP CAP EC106.(Page 18)
10.Change audio from STA9227 to RTL888T and 888 co-lay.(Page 20)
11.Remove 1394 common chock but reserve it.(Page 25)
12.Power Team suggestion R62=681ohm,R57=475ohm
R58=1.65Kohm,R67=22Kohm.(fix load line test failed)(Page 28)
2007/02/07
1.Update USB2*2 connect 料號"N53-16M0081-K06",footprint "USB_A4_16_1".(Page24)
2.Update Power1 connect 料號"N93-08M0081-H06",footprint"POWCONN_D8".(Page28)
3.Update sysfan1 from 4pin FAN to 3pin FAN.(Page 18)
4.Update Bearlake from A0 to A1 料號"B01-LE82BE5-I06".(Page 6,7,8,9)
5.Update ICH9 A1 料號"B01-801IB05-I06".(Page 10,11,12)
6.Co-lay intersil switch power on DDR power and NB power.(Page 27)
HW Ver.0B Change to Ver.10 List:
2007/02/12
1.Change R393 from connect VRM_GD to ICH_VRM_PGD.(Fix boot issue.)(Page 26)
2.Add R460 for SYS1_FANTAC.(Page 18)
3.Add R470 for Q63 turn on.(Page 26)
4.CN10 "C12-4712813-W08" is singl souce change CN10 料號 to "C12-4711013-Y01".(Page 20)
5.Add R244 and R245.(UPI suggestion)(Page 27)
6.Add GPIO23_SIO and GPIO17_SIO for detect ALC888/888T.(Page 16)
2007/0314
1.UPI suggestion R283=4.22K R288=10k, C404=0.1uF. C231=NC, C572=NC. R222=30K, R573=15K, C63=NC,
R431=NC, C74=1uF, R200=2K, R412=NC, C235=NC,R48=510R,R53=10K.(Page26,27)
2.Add SYSFAN4 and SYSFAN5 circuit.(Page18)
3.Remove BEEP circuit(Audio and Fintek I/O),just keep SB BEEP circuit.(Page16,20,29)
4.VGA HSYNC,VSYNC pull down CAP from 33P to 10P.(For fix The Hsync,Vsync of Rise-Voltage Range quality has glitch)(Page17)
5.Update Bearlake from A1 to A2 G33料號"B01-082BL25-I06".(Page 6,7,8,9)
6.Update Bearlake from A1 to A2 P35料號"B01-082BL15-I06".(Page 6,7,8,9)
7.Update ICH9R A2 料號"B01-801IR05-I06".(Page 10,11,12)
8.Update Upi 6261 from A to B 料號"I32-0626119-U33".(Page 26)
9.Remove IR function.(Page 16)
10.Add DLED(8) on board.(Page 29)
11.Add LED(6) on PCI,PCI-E slot.(Page10,21,22)
12.Power team suggestion Q27,Q20,Q11,Q4-make NIKOS-0903(PN: D03-0903BDB-N03) to be main source.(Page 28)
13.Power team suggestion Q16,Q18,Q21,Q26,Q2,Q8,Q5,Q6-make NIKOS-75N02(PN: D03-75N022B-N03) to be main source.(Page 28)
14.Audio SKYPE connect(JSLC1) add 防呆(料號跟FOOTPRINT change).(Page 20)
15.Remove R5 VID_GD pull high(重複Pull high).(Page 4)
16.R393 connect VRM_PGD change to connect ICH_VRM_PGD.(For fix Q64 can not turn on issue)(Pgae26)
17.USB mode add R470 for Q63 turn on.(Page26)
18.Add R460=27Kohm for FAN speed detect.(Page18)
19.ICSn Clock GEN Pin9 must pull down,Pin64 must pull high for clock GEN straping.(Page15)
20.ICS Clock GEN change to Ver.C 料號"I11-RS90622-I02".(Page15)
21.Update Heatpipe 料號"E31-0800340-A21".(Page30)
22.Add NB_SB heatsink for cost down.(Page30)

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MS-7345

Size: Custom | Document Description: Revision History | Rev: 1.2

Date: Friday, May 18, 2007 | Sheet 34 of 35

HW Ver.10 Change to Ver.1.1 List:
1.Add EC57 and EC58 for 3VSB and 5VSB drop.(Page 26)
2.Change CPU Vcore CAP from 560u to 820u.(Page 28)
3.Add JB1,JB2 for OC used.(Page 15)
4.R401,R419 from 4.7Kohm to 20Kohm for ATX_PER_OK to tune on 3904.(Page 26,27)
5.ATX_PWR_OK pull up R210=1K to VCC5.(Page 29)

HW Ver.1.1 Change to Ver.1.2 List:
1.Audio 10u/10V(EC68,69,75,76,72,73,70,80) DIP CAP change to SMD CAP.(Page 20)
2.1394 Extenal components(R88,R84,R81,R71,R74,C60,C68) placement from connect side to chip side.(Page 25)
3.1394 R532=6.34K-->6.2K,C622=0.1u-->1u.(Page 25)
4.VRD ODT R6=200K-->no stuff,R7=100K-->22ohm.(Page 28)
5.JUMP cricuit change.(Page 15)
6.Audio CD-G circuit change.(Page 20)
7.E-SATA port0,1 and SATA port2,3 swap.(Page 18)

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MS-7345

Size	Document Description	Rev
Custom	Revision History	1.2

Date: Friday, May 18, 2007 | Sheet 35 of 35