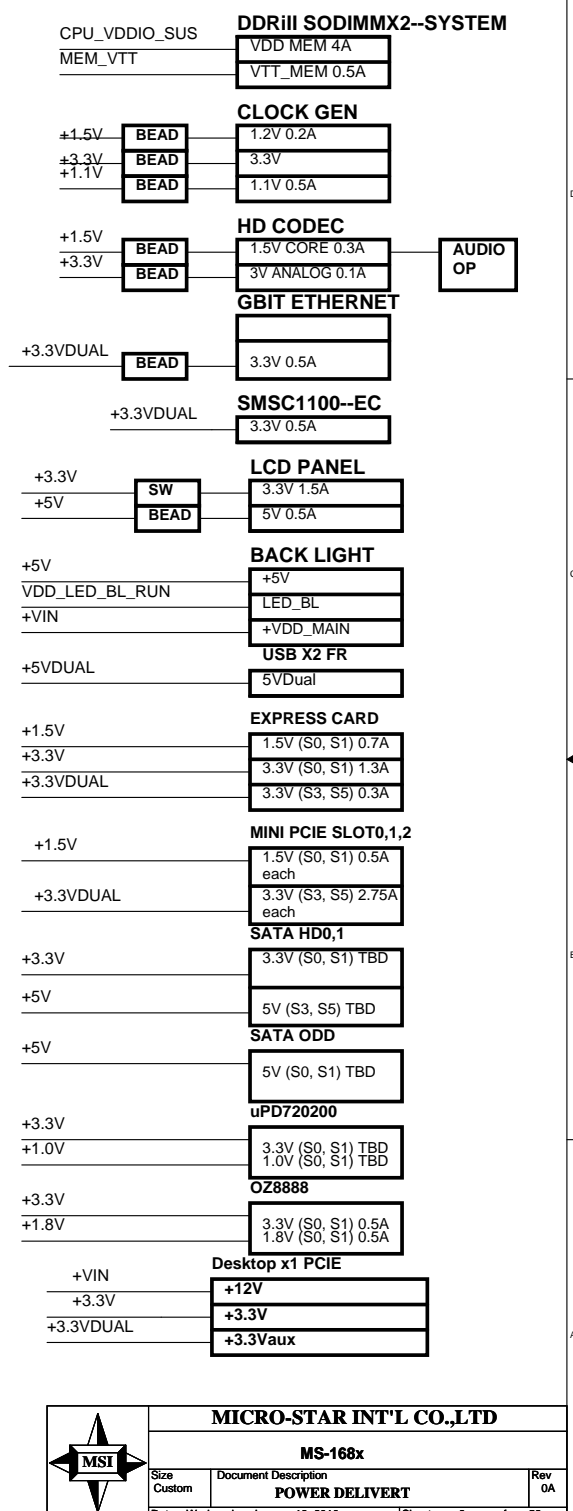
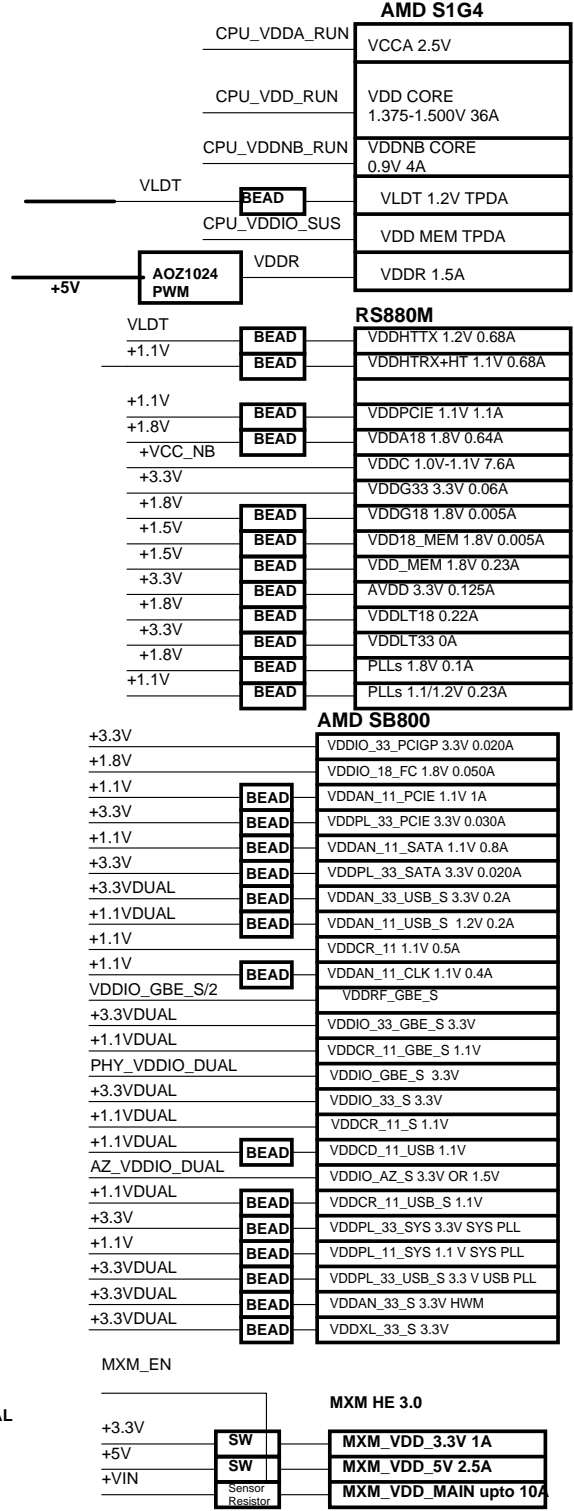
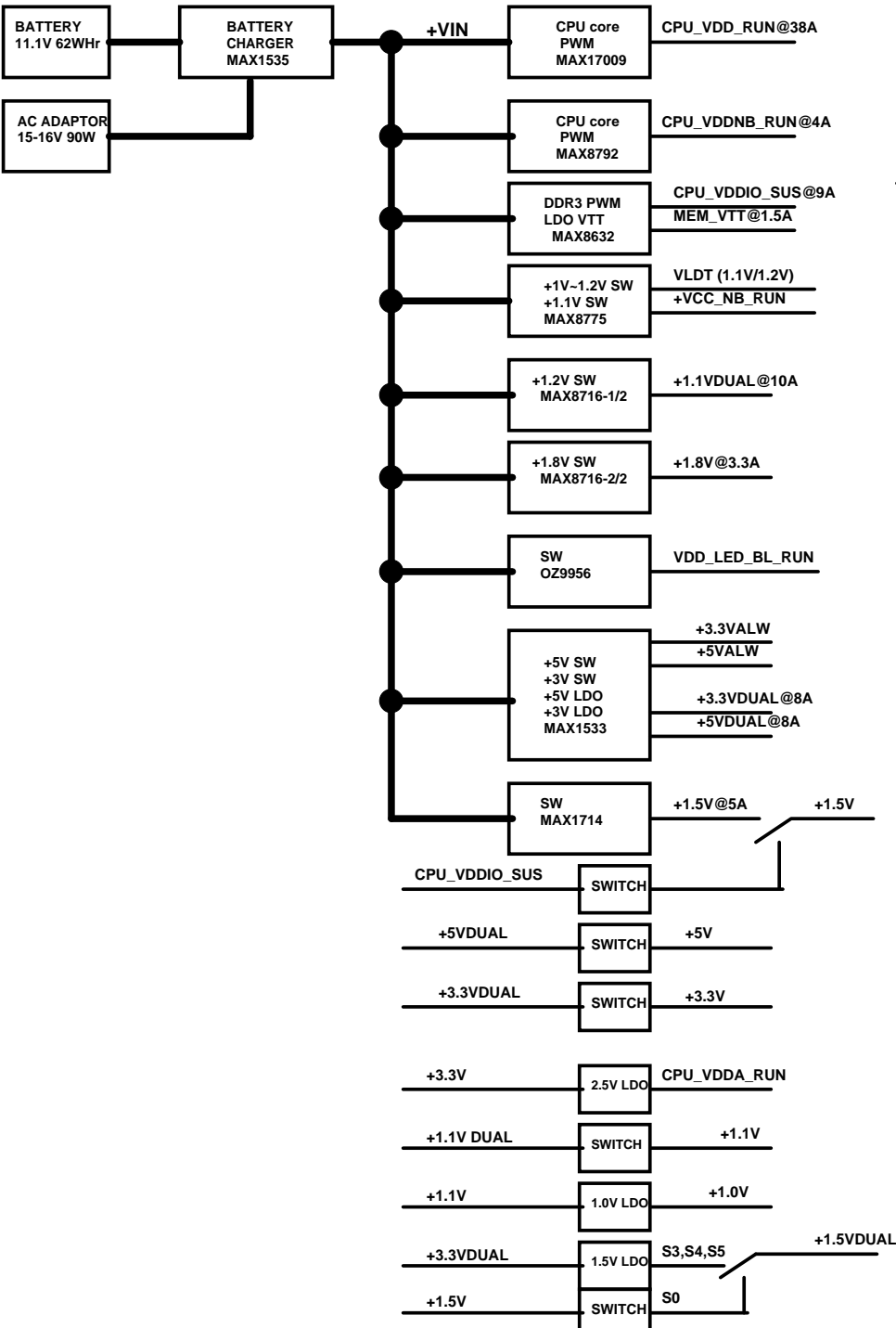


<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-168x</b>		
Size Custom	Document Description <b>BLOCK DIAGRAM</b>	Rev 0A
Date: Wednesday, January 13, 2010	Sheet	1 of 52

# TABLE OF CONTENTS

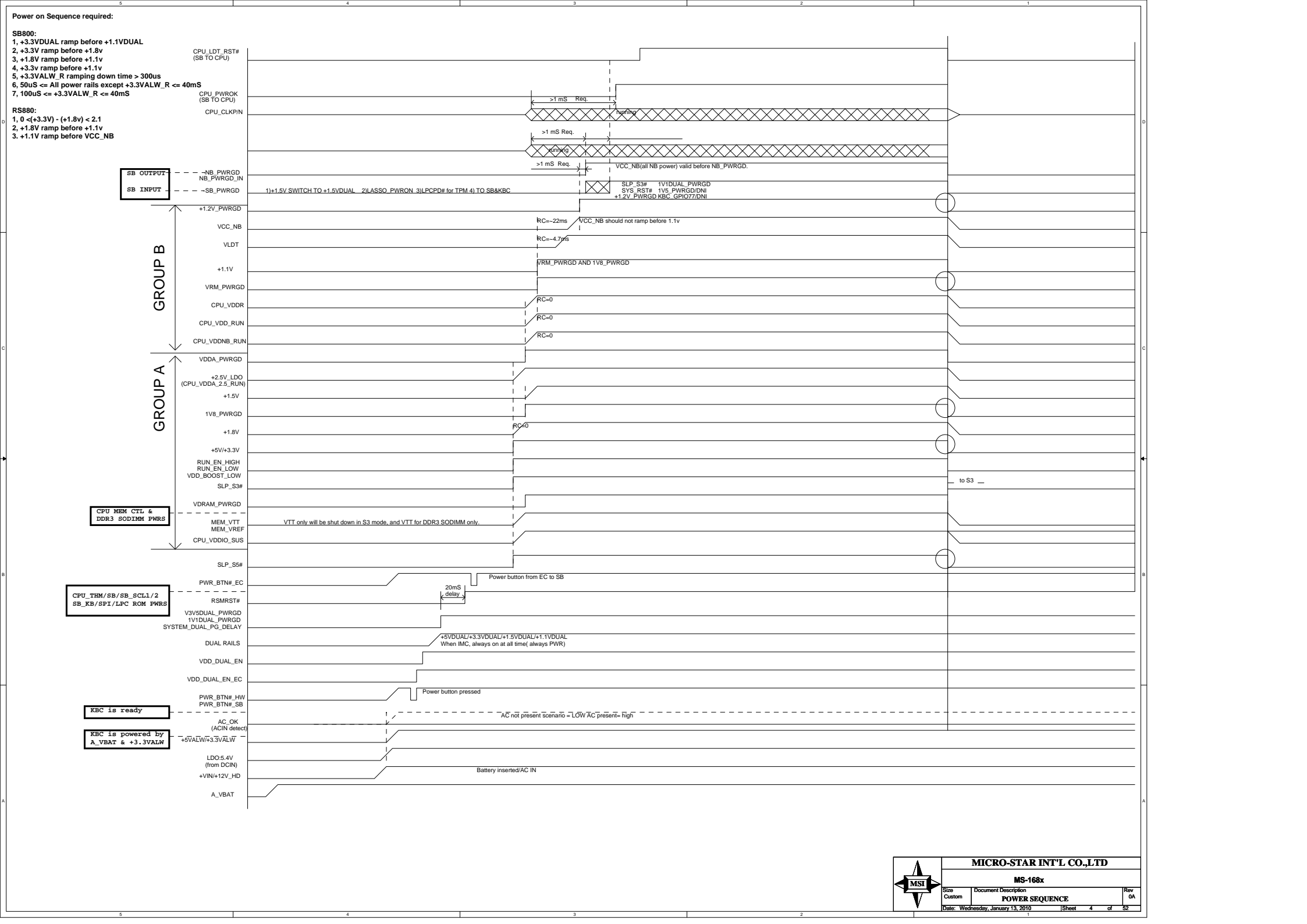
P01 : BLOCK DIAGRAM	P32 : MXM PWR / MISC
P02 : TABLE OF CONTENTS	P33 : MXM 3.0 EDGE
P03 : POWER DELIVERY CHART	P34 : LVDS / CRT SWITCH
P04 : POWER SEQUENCE CHART	P35 : LVDS CON / BACKLIGHT
P05 : CLOCK DISTRIBUTION	P36 : CRT / LASSO CONN
P06 : MISC TABLES	P37 : EDP / DPD
P07 : BATTERY CHARGER	P38 : DPB / DPC
P08 : CPU CORE PWR	P39 : USB3.0 (1)
P09 : CPU MEM PWR	P40 : USB3.0 (2)
P10 : 1V1DUAL / 1V1 /18V /3V3 /5V	P41 : SATA CONN / DEBUG
P11 : 1V5 / 1V5DUAL	P42 : HD AUDIO CODEC
P12 : NBCORE / VLDT	P43 : HD AUDIO CONN
P13 : SYSTEM POWER	P44 : 1394 / SD READER
P14 : S1G4 HT I/F	P45 : FP / BT / CIR
P15 : S1G4 DDRIII MEMORY I/F	P46 : USB2.0 PORTS
P16 : S1G4 CTRL / DEBUG	P47 : LAN PHY (B50610)
P17 : S1G4 PWR / GND	P48 : MINI PCIE SLOT 0, 3
P18 : DDR3 SODIMMS A/B CHANNLE	P49 : MINI PCIE SLOT 1, 2
P19 : DDR3 SODIMMS DECOUPLING	P50 : X4 GPP / PCIE EXPRESS CARD
P20 : EXTERNAL CLOCK GEN	P51 : LOM (57760)
P21 : RS880M HT I/F	P52 : KBC - SMSC1100L
P22 : RS880M PCIE I/F	P53 : KBCBIOS / KBD /MOUSE
P23 : RS880M SYSTEM	P54 : CONFIG ROM / LPC ROM / TPM
P24 : RS880M SPMEM/STRAPS	P55 : RESET / FAN / LED / PWRGD
P25 : RS880M POWER	P56 : ACPI CONN
P26 : SB8X0 PCIE/PCI/CPU/LPC/CLK	P57 : DEBUG - POST LEDS
P27 : SB8X0 GPIO/USB/AZ/RGMII	P58 : DUAL RAIL ENABLE
P28 : SB8X0 SATA/IDE/HWM/SPI	P59 : DISCHARGE CIRCUIT
P29 : SB8X0 POWER / DECOUPLING	P60 : SB800 A11 PU RES
P30 : SB8X0 STRAPS	P61 : CHANGE HISTROY
P31 : PCIE SWITCH	P62 : POWER ON SEQUENCE CHART



**MICRO-STAR INT'L CO.,LTD**

**MS-168x**

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<b>POWER DELIVERT</b>		
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**SB800:**  
 1, +3.3VDUAL ramp before +1.1VDUAL  
 2, +3.3V ramp before +1.8v  
 3, +1.8v ramp before +1.1v  
 4, +3.3v ramp before +1.1v  
 5, +3.3VALW\_R ramping down time > 300us  
 6, 50uS <= All power rails except +3.3VALW\_R <= 40mS  
 7, 100uS <= +3.3VALW\_R <= 40mS

**RS880:**  
 1, 0 <(+3.3V) - (+1.8v) < 2.1  
 2, +1.8v ramp before +1.1v  
 3, +1.1v ramp before VCC\_NB

GROUP B

GROUP A

SB OUTPUT  
 --NB\_PWRGD  
 NB\_PWRGD\_IN  
 SB INPUT  
 --SB\_PWRGD

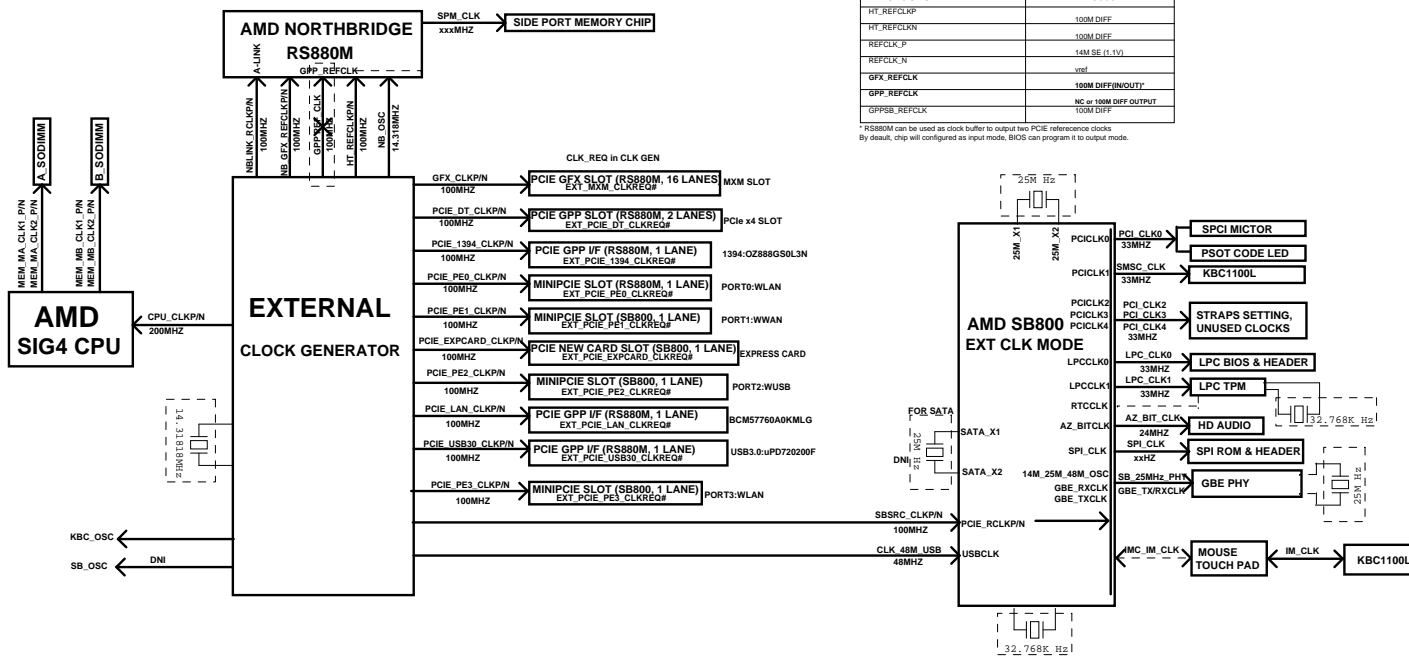
CPU MEM CTL &  
 DDR3 SODIMM PWRs

CPU\_THM/SB/SB\_SCL1/2  
 SB\_KB/SPI/LPC ROM PWRs

KBC is ready

KBC is powered by  
 A\_VBAT & +3.3VALW

# EXTERNAL CLOCK MODE

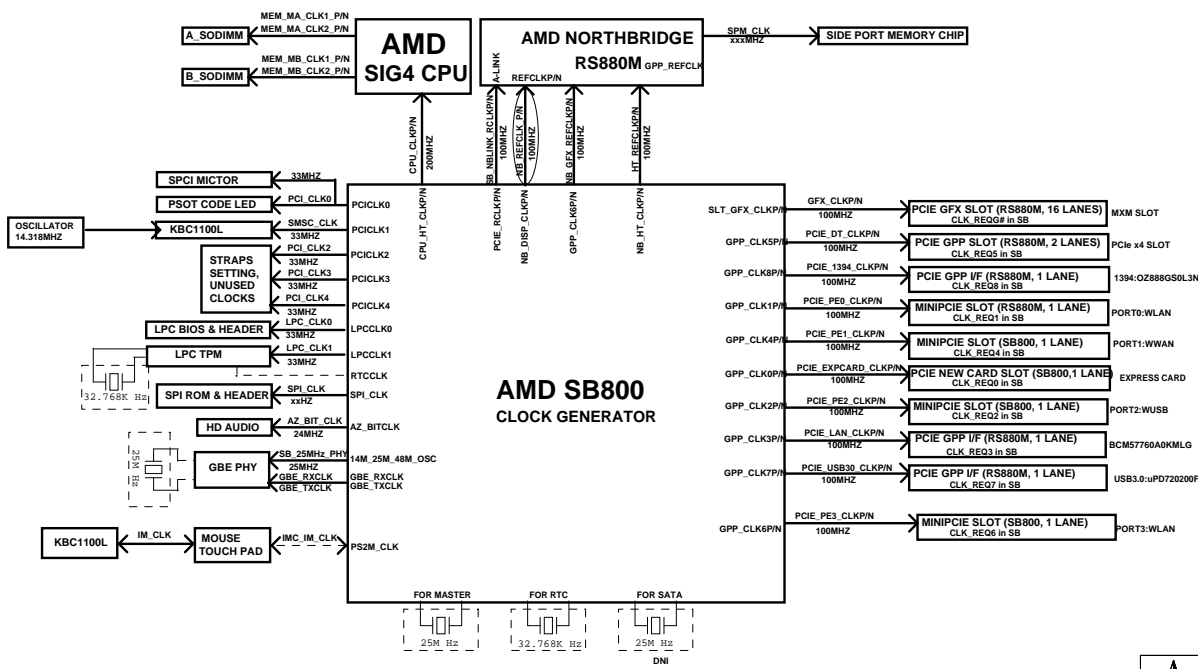


NB CLOCK INPUT TABLE

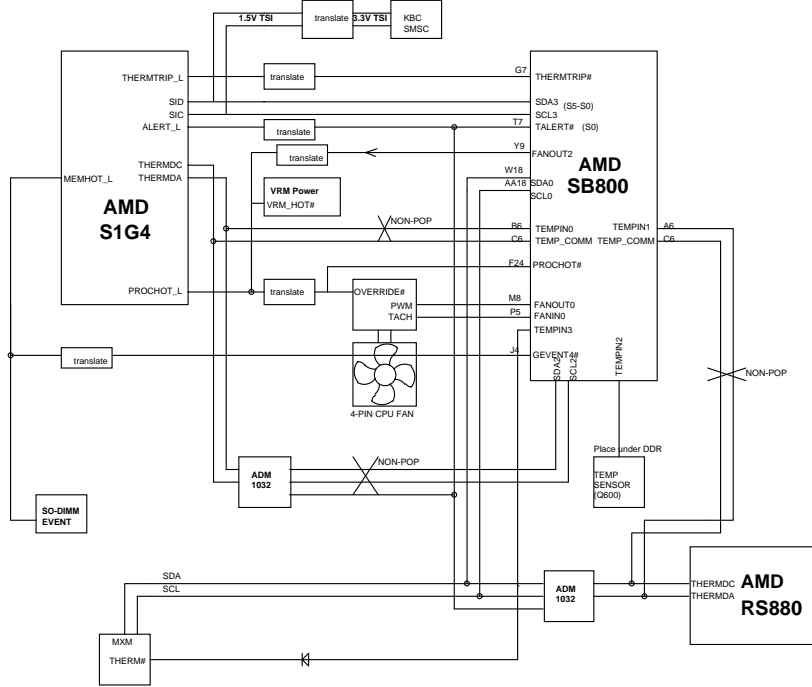
NB CLOCKS	RS880M
HT_REFLCKP	100M DREF
HT_REFLCKN	100M DREF
REFCLK_P	14M SE (1.1V)
REFCLK_N	14M SE (1.1V)
GFX_REFLCK	100M DREF/IN/OUTY
GPP_REFLCK	100M DREF/IN/OUTY
GPPSB_REFLCK	100M DREF

RS880M can be used as clock buffer to output two PCIe reference clocks  
 By default, chip will configured as input mode, BIOS can program it to output mode.

# INTERNAL CLOCK MODE

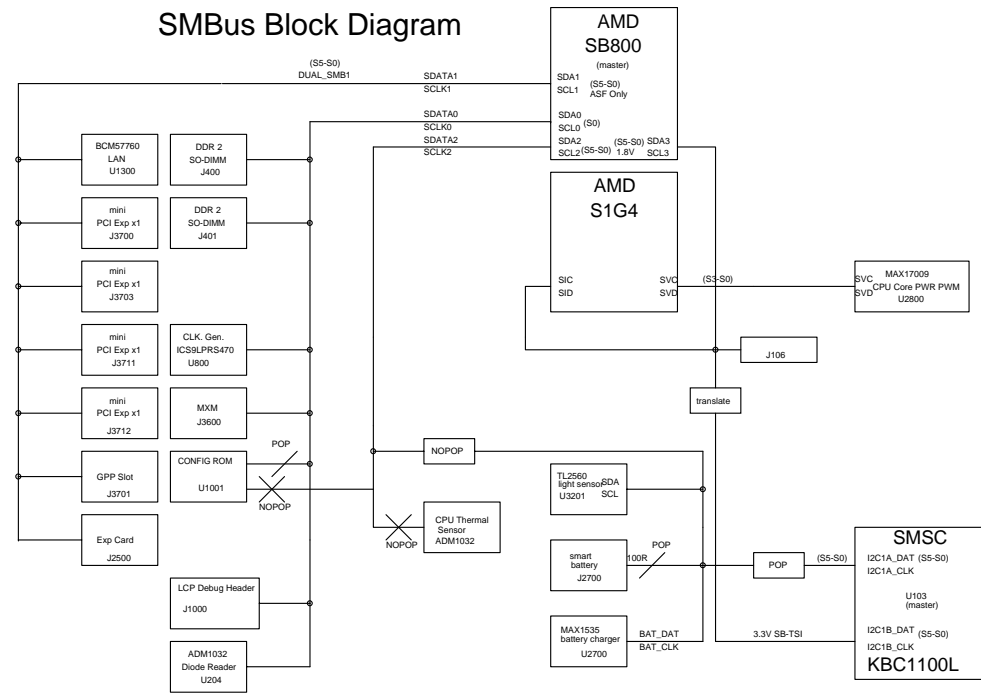


## Thermal Systems (Emergency Shutdown, Throttling, Fan Control)



Thermal disaster prevention is implemented by PROCHOT\_L and THERMTRIP\_L with hardware non-system dependant functions. Fan speed control will only be implemented by SB TSI software based implementation

## SMBus Block Diagram



## Power State / Voltage Rail Activity Summary

Global System State	Sleep State	Processor Power State	Description	RTC	ALW	DUAL	SUS	RUN
G0	S0	C0	Running	ON	ON	ON	ON	ON
G0	S0	C0	Running	P-state transitions under OS control	ON	ON	ON	ON
G0	S0	C1	Halt	ON	ON	ON	ON	ON
G0	S0	C2	Stop grant, caches snooperable	ON	ON	ON	ON	ON
G0	S0	C3	TBD	ON	ON	ON	ON	ON
G0	S0	C4	TBD	ON	ON	ON	ON	ON
G1	S1	OFF	Powered on suspend	ON	ON	ON	ON	ON
G1	S3	OFF	Suspend to RAM	ON	ON	ON	ON	OFF
G2	S4	OFF	Suspend to disk	ON	ON	ON	OFF	OFF
G2	S5	OFF	Soft-off	ON	ON	ON	OFF	OFF
G2/G3	S5 LOW	OFF	Battery IN	ON	ON	ON	OFF	OFF
G3	OFF	OFF	Mechanical off	ON	OFF	OFF	OFF	OFF

## Group Name Description

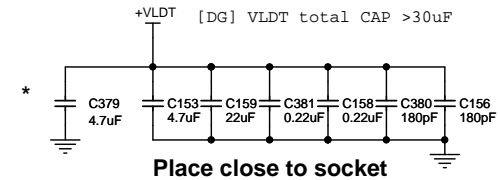
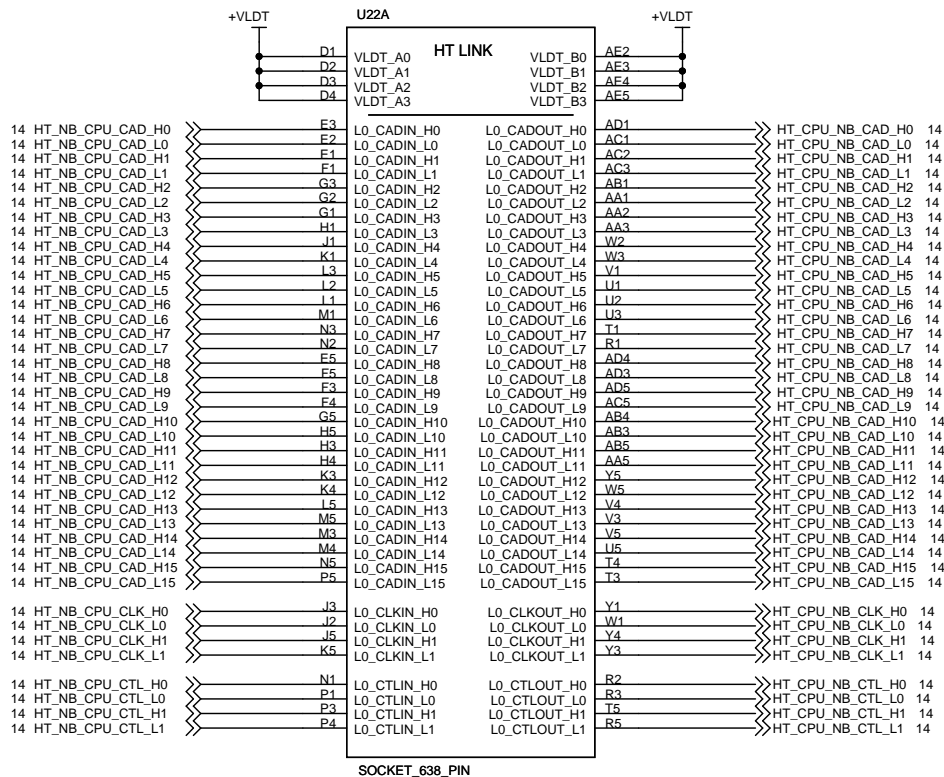
INT: Stuff when use internal clock generator  
 EXT: Stuff when use external clock generator  
 DNI: DO NOT INSTALL  
 KBC: Stuff when use external KBC  
 IMC: Stuff when use internal EC  
 A11: Resistors marked with "A11" is only for SB800A11 ONLY.



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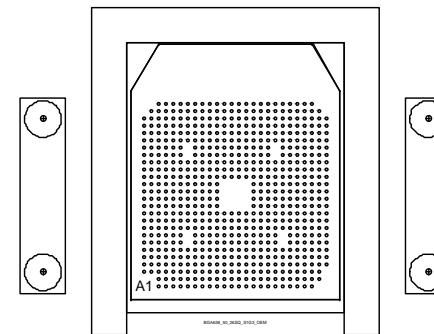
MS-168x

Size Custom	Document Description	Rev 0A
SMBUS BLOCK		
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**\* If VLDT is connected only on one side, one 4.7uF cap should be added to the island side**

[ChckList] Can change 22u\*1/4.7u\*2 to 10u\*3



[CheckList] If the I/O device does not support the CTLIN1 pair, pull up 51ohm



**MICRO-STAR INT'L CO.,LTD**

**MS-168x**

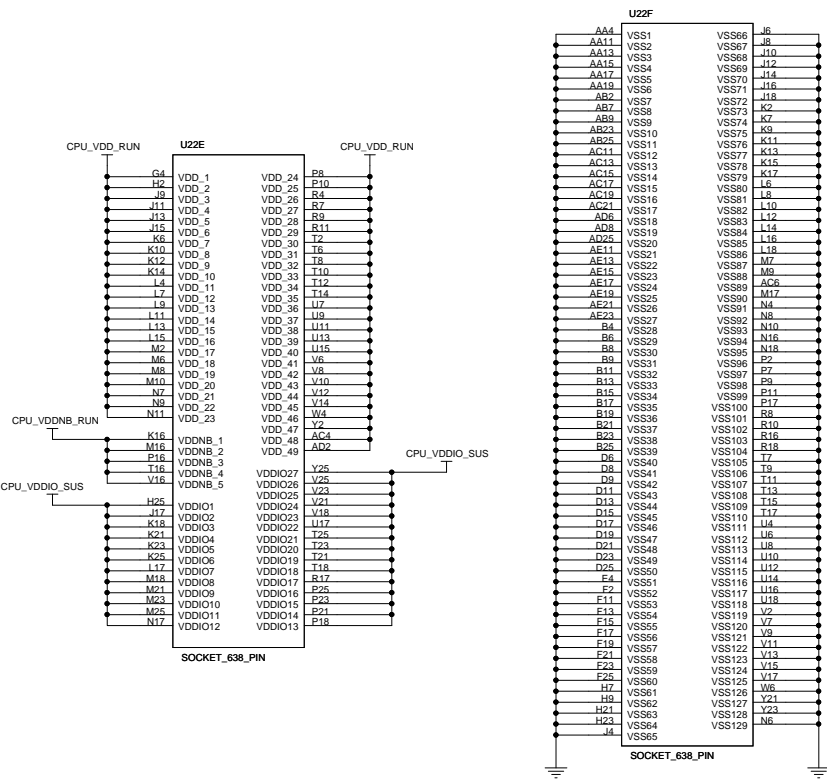
Size B	Document Description	Rev 0A
	<b>SIG4 HT I/F</b>	
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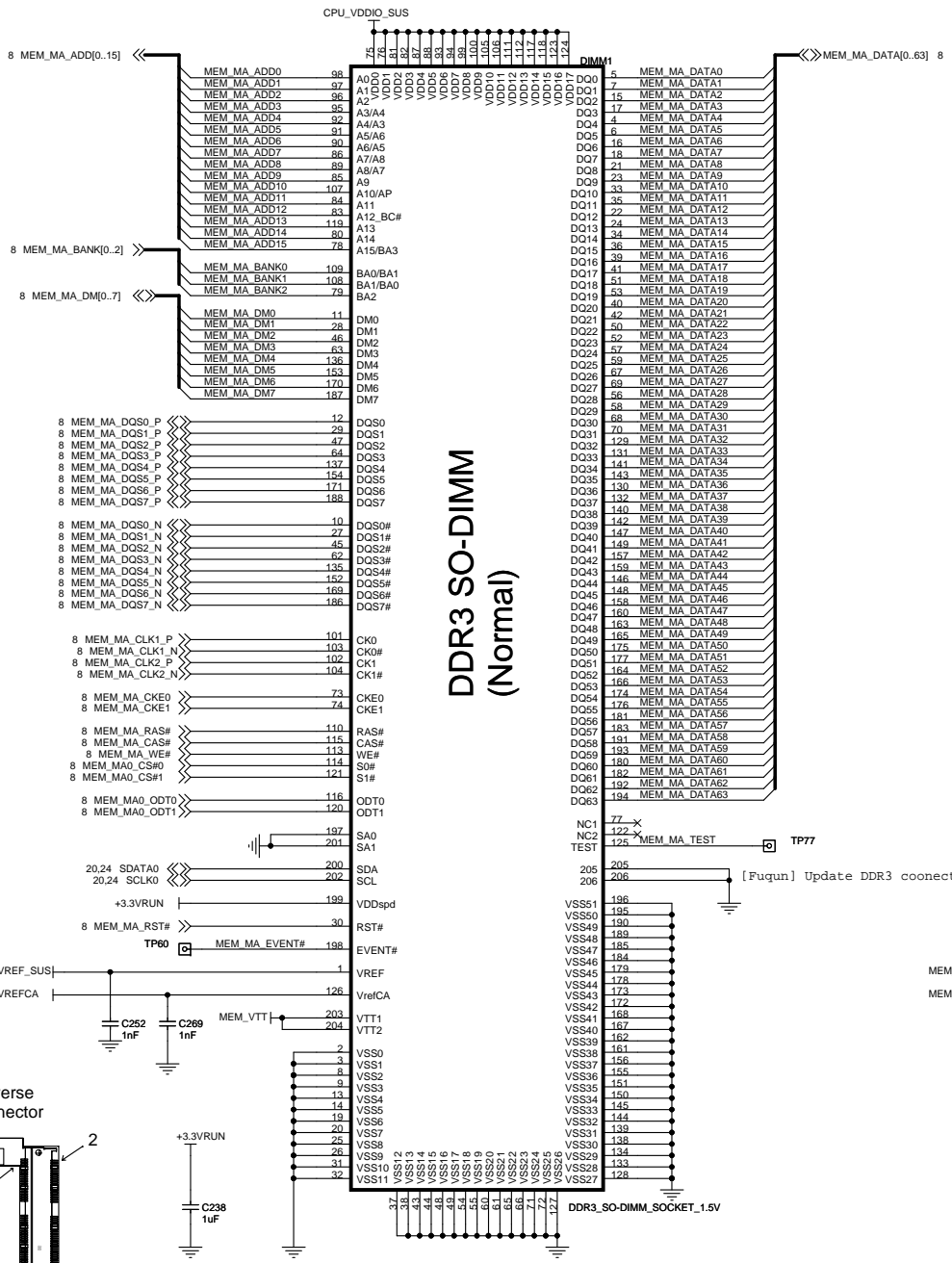




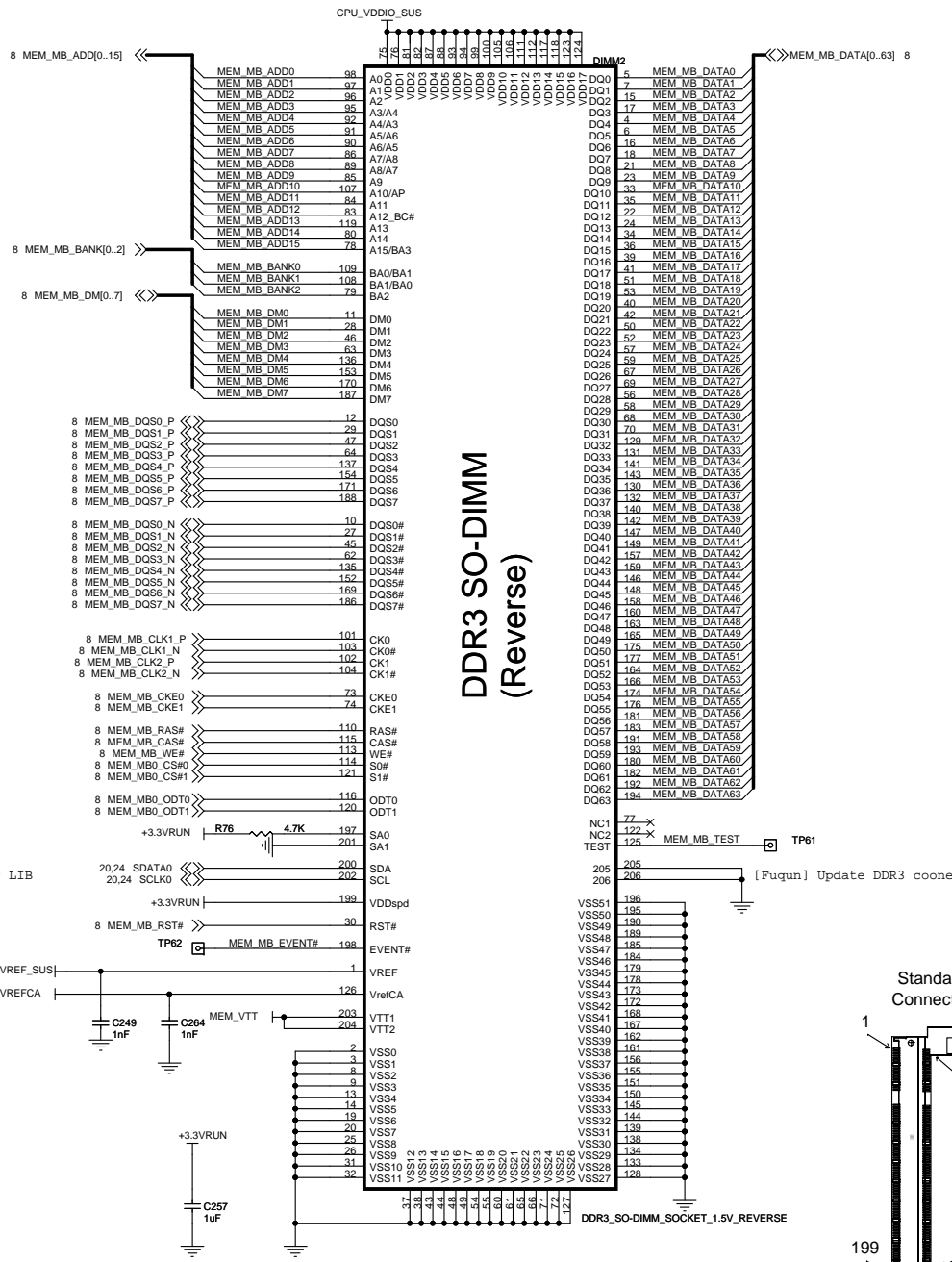


# PROCESSOR POWER AND GROUND

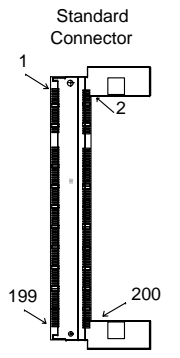
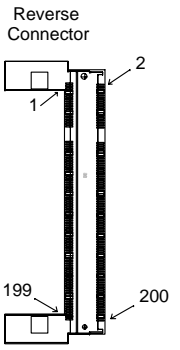




**DDR3 SO-DIMM (Normal)**



**DDR3 SO-DIMM (Reverse)**



5

4

3

2

1

D

C

B

A

D

C

B

A


5

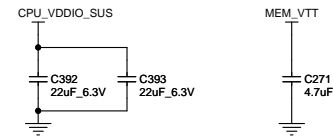
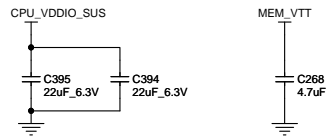
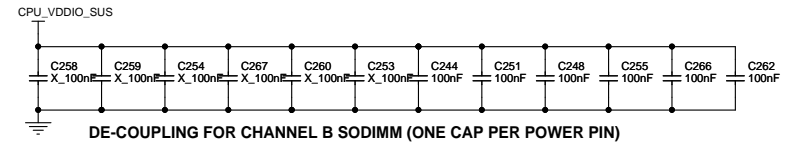
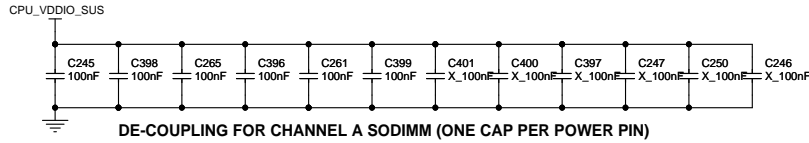
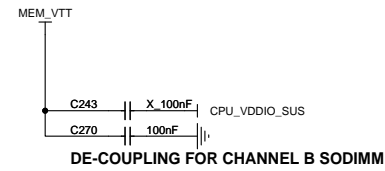
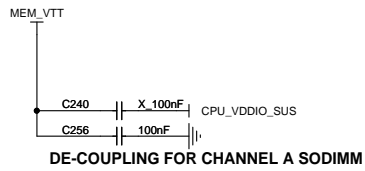
4

3

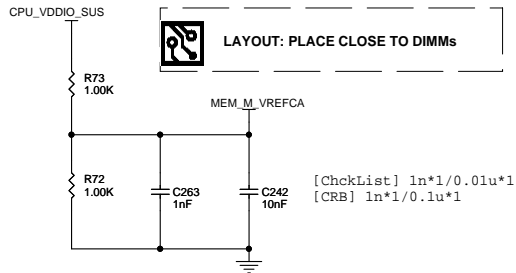
2

1

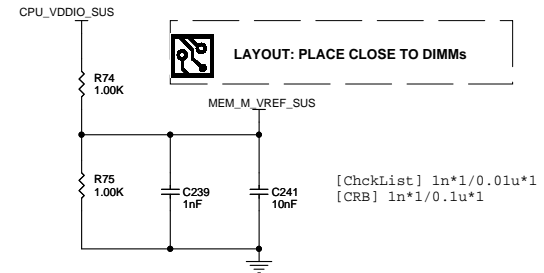
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	<b>MS-168x</b>		
Size A	Document Description <b>DDR3 SO-DIMM-B</b>	Rev 0A	
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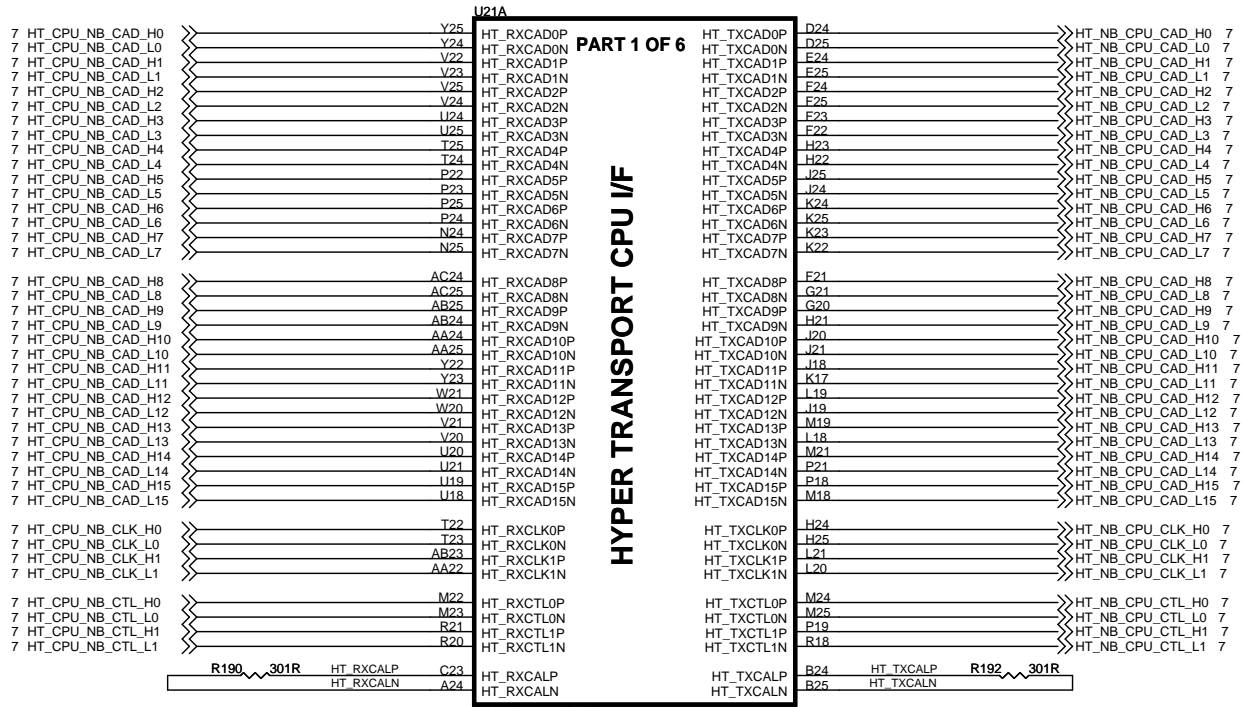
### MEM\_M\_VREFCA




### MEM\_VREF\_SUS



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-168x</b>		
Size Custom	Document Description <b>DDR3 DECOUPLING</b>	Rev 0A
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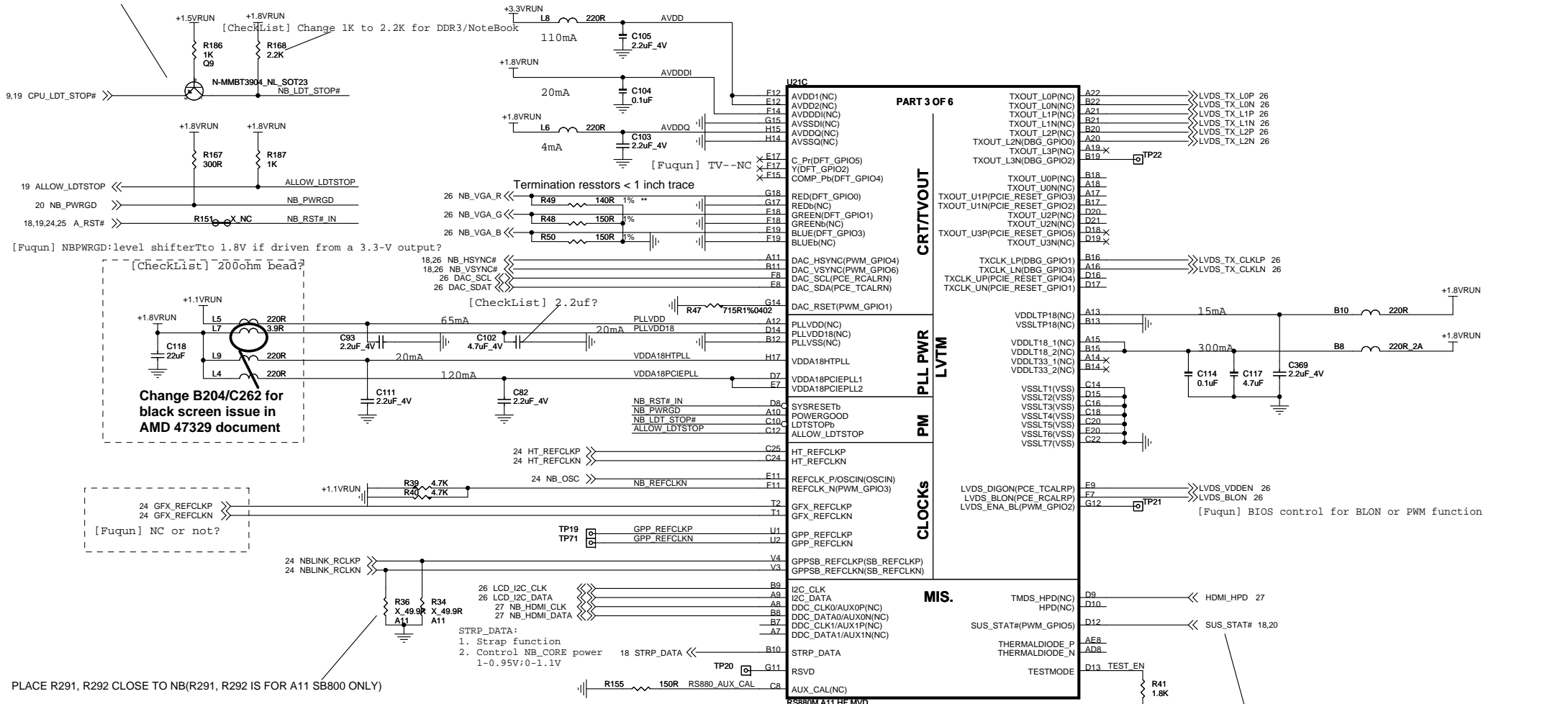


RS880M A11 HF MVD

			<b>MICRO-STAR INT'L CO.,LTD</b>	
			<b>MS-168x</b>	
Size B	Document Description <b>RS880M-HT</b>			Rev 0A
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DDR3 based CPU and mobile platforms--Level shift to 1.8V  
 DDR2 based CPU mobile platforms--No need level shift



Change B204/C262 for black screen issue in AMD 47329 document

[Fuqun] NC or not?

PLACE R291, R292 CLOSE TO NB(R291, R292 IS FOR A11 SB800 ONLY)

[Fuqun] SUS\_STAT#-->Not need connect to SB if Side-Port memory not implemented

**RS880M DEBUG PIN MAPPING**

DEBUG_OUT0	LVDS_DIGON
DEBUG_OUT1	LVDS_ENA_BL
DEBUG_OUT2	LVDS_BLON
DEBUG_OUT3	TMDS_HPD
DEBUG_OUT4	AUX1N
DEBUG_OUT5	AUX1P
DEBUG_OUT6	HPD
DEBUG_OUT7	AUX_CAL

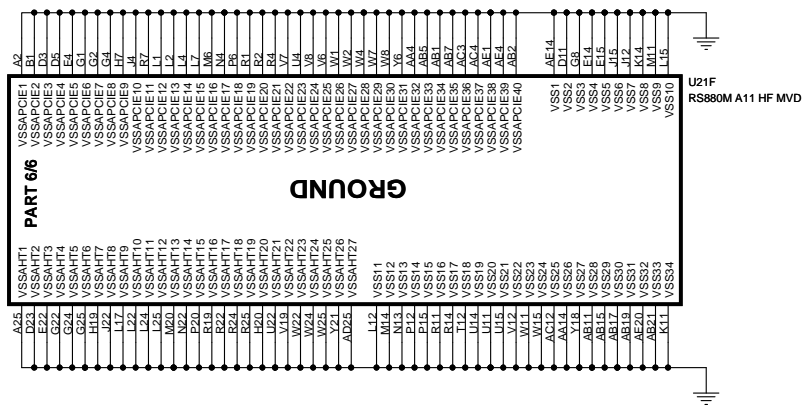
**MICRO-STAR INT'L CO.,LTD**

**MS-168x**

Size: Custom | Document Description: **RS880M-1/F** | Rev: 0A

Date: Friday, February 05, 2010 | Sheet: 16 of 52

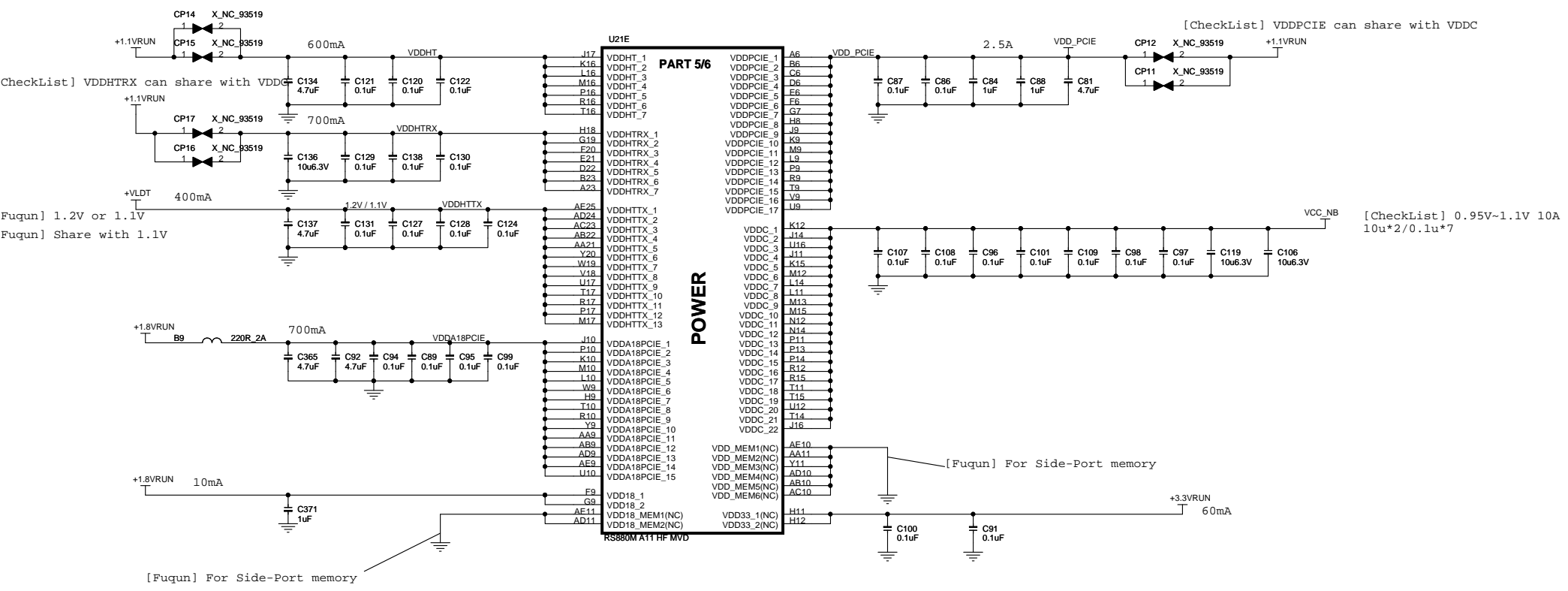




RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL33	NC

[CheckList] VDDHT can share with VDDC



[CheckList] VDDHTRX can share with VDDC

[CheckList] VDDPCIE can share with VDDC

[Fuqun] 1.2V or 1.1V

[Fuqun] Share with 1.1V

[CheckList] 0.95V~1.1V 10A  
10u\*2/0.1u\*7

[Fuqun] For Side-Port memory

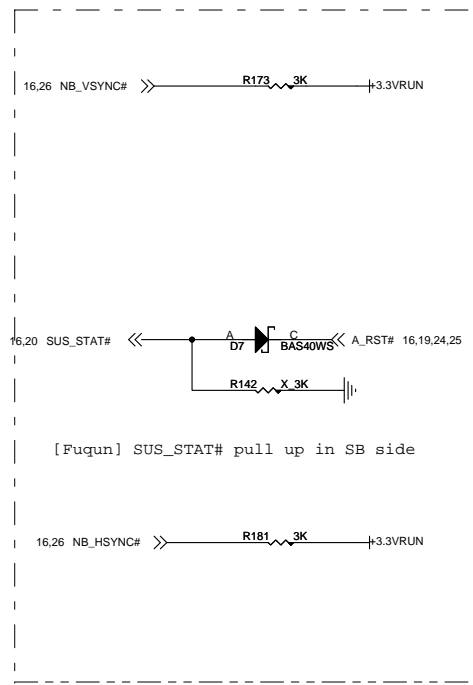
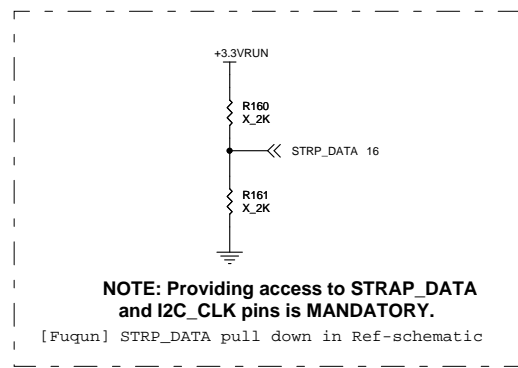
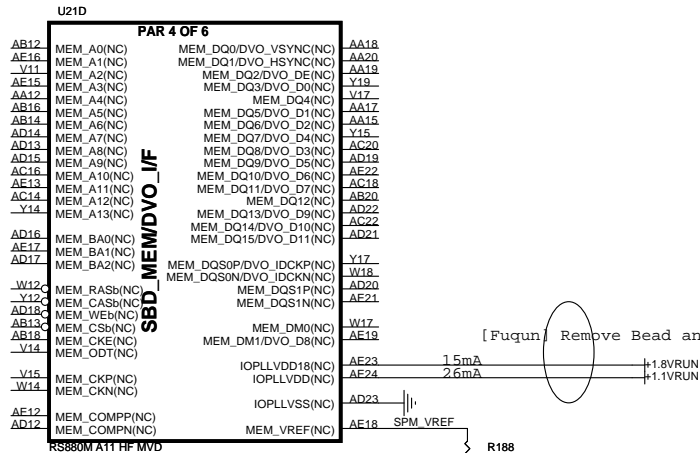
[Fuqun] For Side-Port memory

**MICRO-STAR INT'L CO.,LTD**

**MS-168x**

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**STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb**

Enables the Test Debug Bus using GPIO.

RS880M	
1 = Disable	
0 = Enable	

**DFT\_GPIO1: LOAD\_EEPROM\_STRAPS**

Selects Loading of STRAPS from EPROM

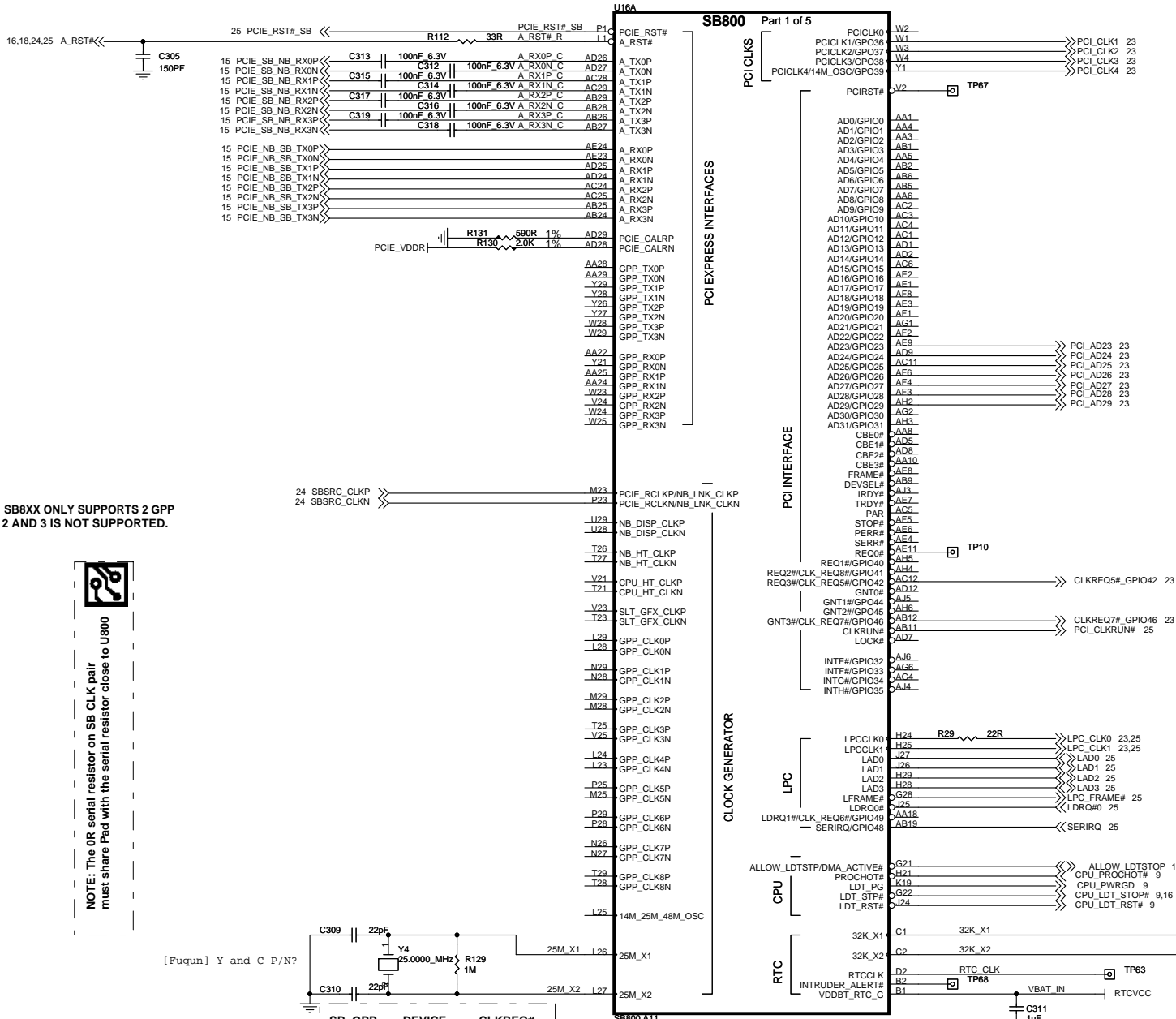
1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

**RS880M: Enables Side port memory**

RS880M:HSYNC#

Selects if Memory SIDE PORT is available or not  
 1 = Memory Side port Not available  
 0 = Memory Side port available  
 Register Readback of strap: NB\_CLKCFG:CLK\_TOP\_SPARE\_D[1]

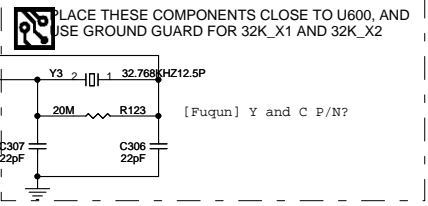
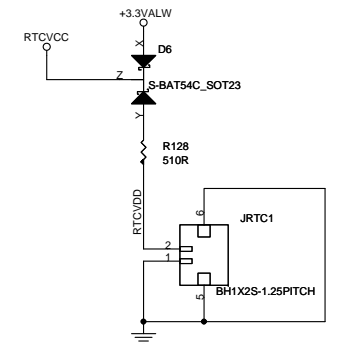
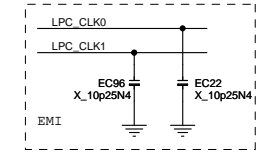
**PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600**



PEX\_STD\_SW#: Low - Standard(desktop) Swing Level Input(3T) - Low Swing Level Mode (Default)

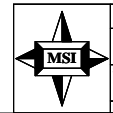
NOTE: SB8XX ONLY SUPPORTS 2 GPP PORT 2 AND 3 IS NOT SUPPORTED.

NOTE: The 0R serial resistor on SB\_CLK pair must share Pad with the serial resistor close to U800



PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K\_X1 AND 32K\_X2

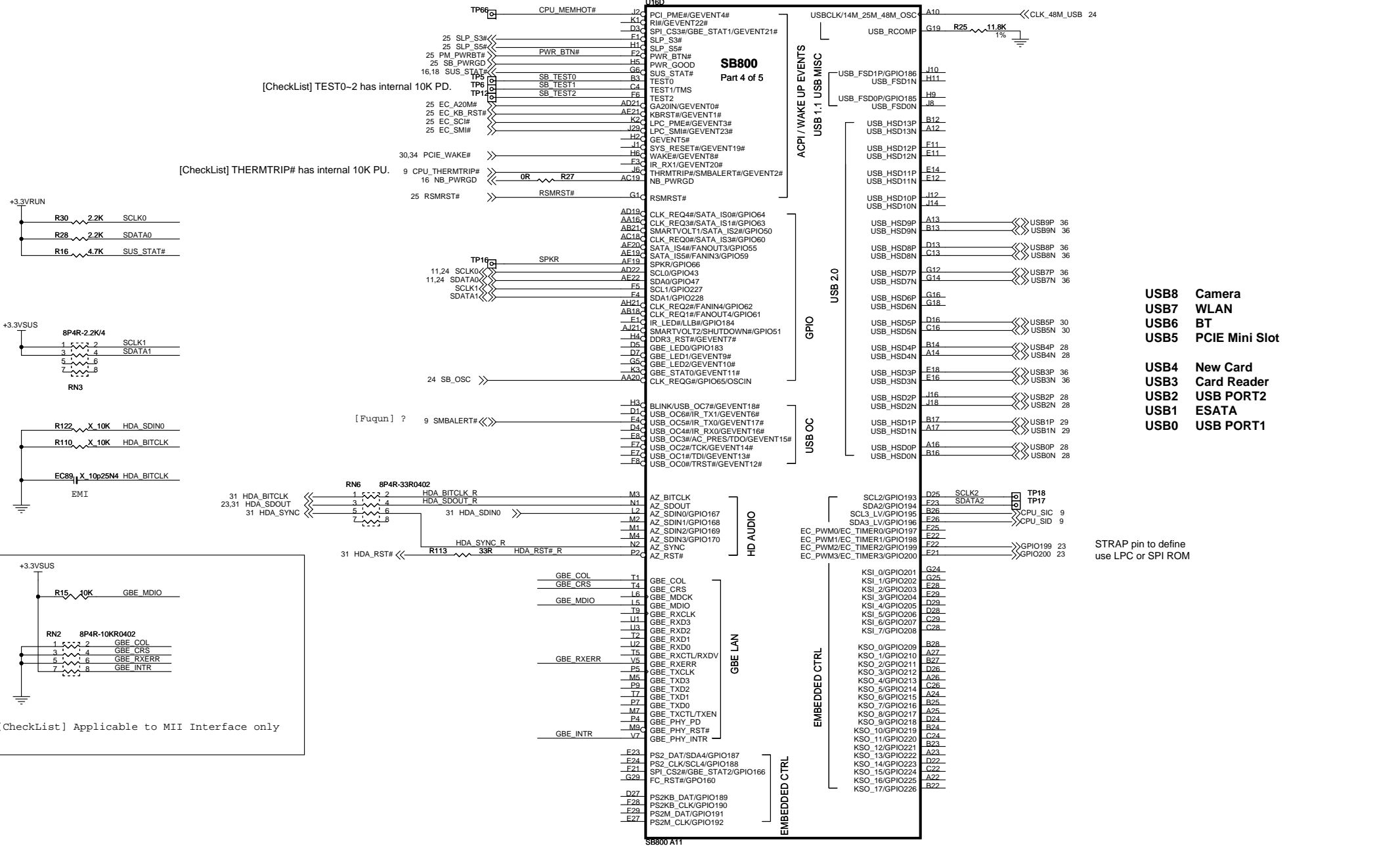
[Fuqun] Y and C P/N?



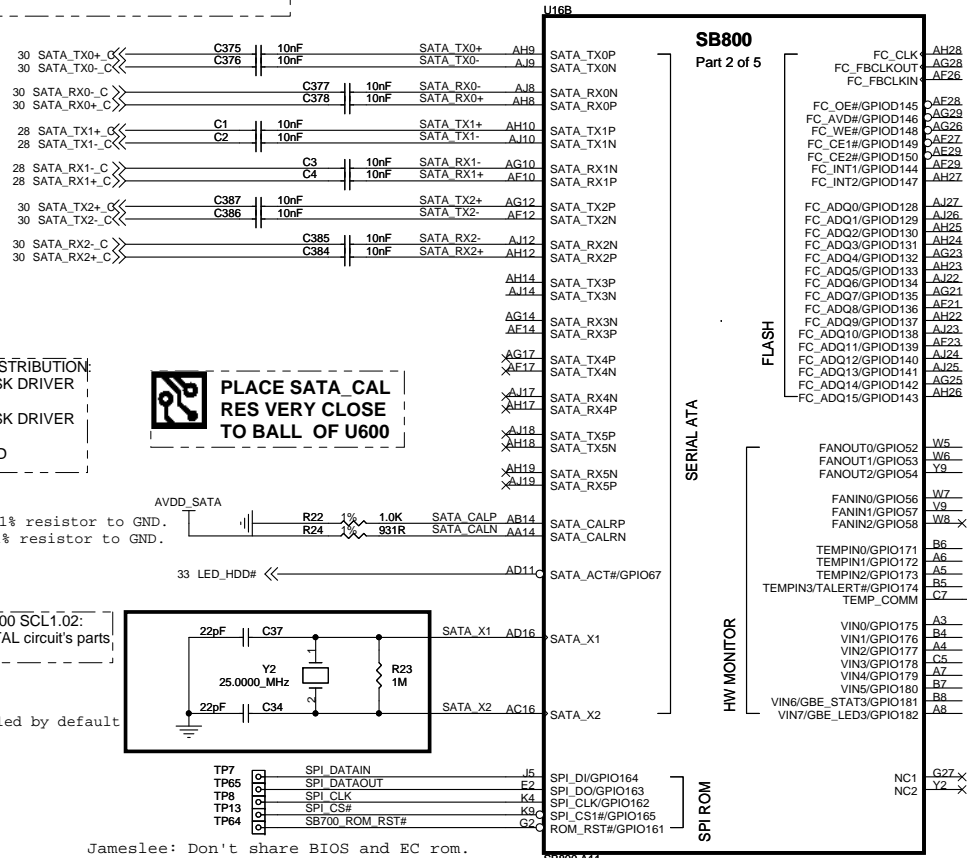
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-168x</b>		
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POWER EXPRESS SUPPORT		
PE_GPIO0 MXM RESET		H: Enable
PE_GPIO1 MXM POWER ENABLE		H: Enable
PE_GPIO2 MODE SWITCH(BY NB)		H:MXM L:NB
TMDS_HPDD0 MXM HOT PLUG		

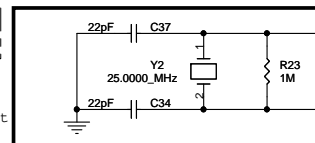
SB_GPP GFX_CLK	DEVICE	CLKREQ#	CLK_REQ#
0	MXM3.0 EXPRESS		0
1	PE0		1
2	PE2		2
3	LAN		3
4	PE1		4
5	X4DT		5
6	PE3		6
7	USB3.0		7
8	1394		8



SATA trace should use only 1 via on the trace. customers can use 2vias with GND via within 150mils of signal via as long as they can ensure that their platform meets SATA logo requirements. Return loss is expected to get affected with 2 vias. AMD platforms are validated with one via only

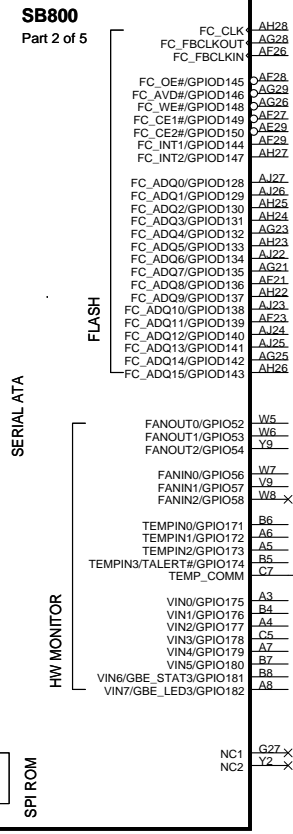


SATA\_CALRP:  
 SB8xx A11: 800-? 1% resistor to GND.  
 SB8xx A12: 1K-? 1% resistor to GND.



[Fuqun] Not installed by default

Jameslee: Don't share BIOS and EC rom.

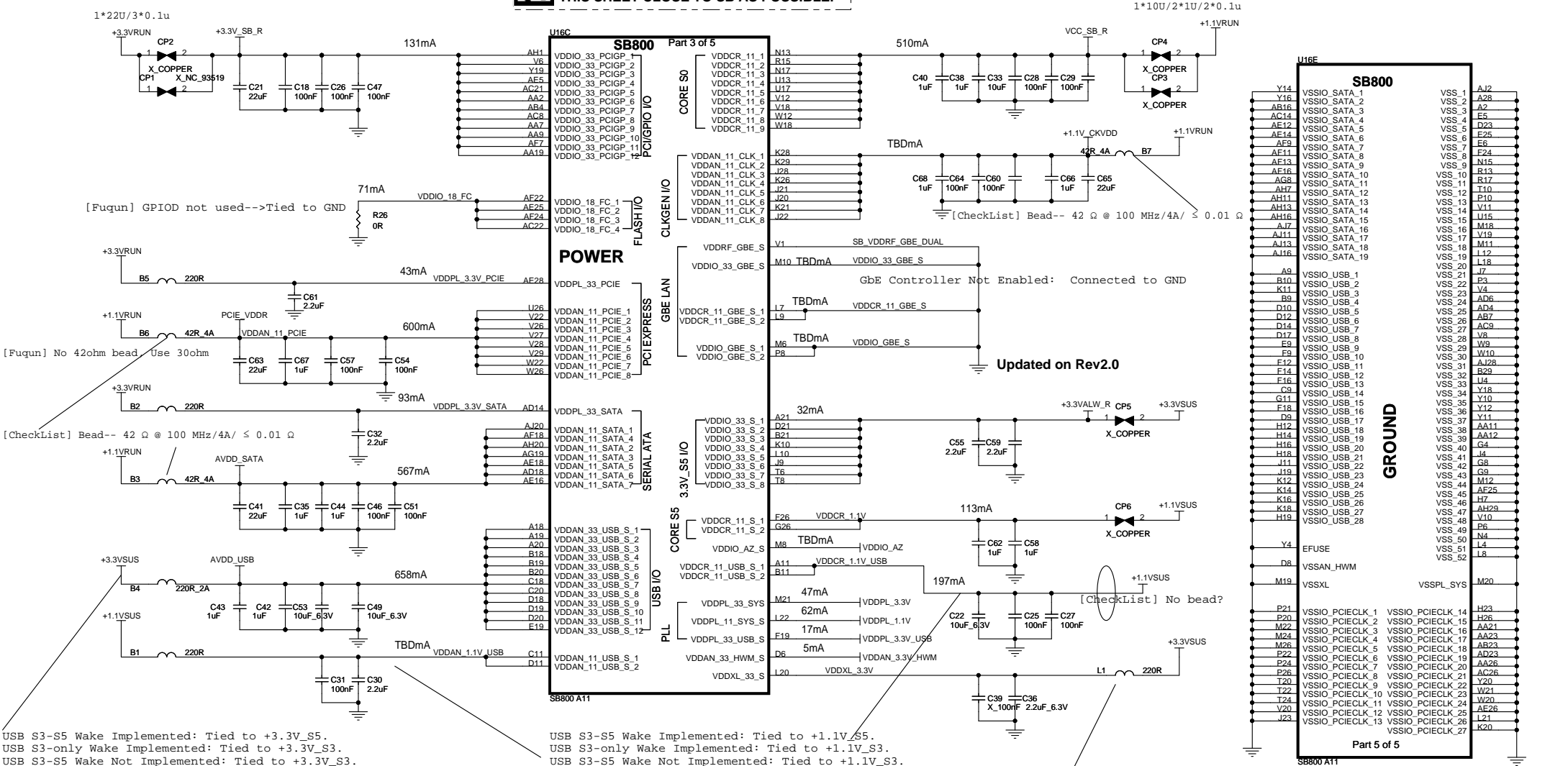


Connect C7 and D8, then go to GND directly.

[Fuqun] HWM need pull-low follow MS-124X?

**NOTE: ROUTE TEMP\_COMM AS A 10MIL TRACE**

**PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.**



[Fuqun] GPIOD not used-->Tied to GND

[Fuqun] No 42ohm bead Use 30ohm

[CheckList] Bead-- 42  $\Omega$  @ 100 MHz/4A/  $\leq$  0.01  $\Omega$

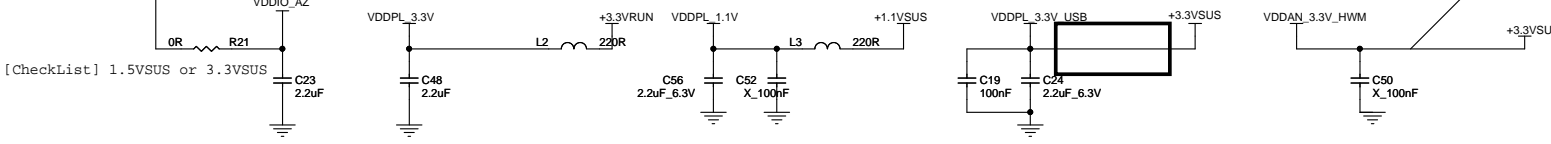
USB S3-S5 Wake Implemented: Tied to +3.3V\_S5.  
 USB S3-only Wake Implemented: Tied to +3.3V\_S3.  
 USB S3-S5 Wake Not Implemented: Tied to +3.3V\_S3.

USB S3-S5 Wake Implemented: Tied to +1.1V\_S5.  
 USB S3-only Wake Implemented: Tied to +1.1V\_S3.  
 USB S3-S5 Wake Not Implemented: Tied to +1.1V\_S3.

Wake on LAN supported: Tied to a +3.3V\_S5 rail

HWM not Implemented and not used as GPIOs: Bead and Decoupling caps not used.

To meet SB800 SCL1.02: Separate ferrite bead is not required for VDDPL\_33\_USB\_S, Del B603/600ohm bead.

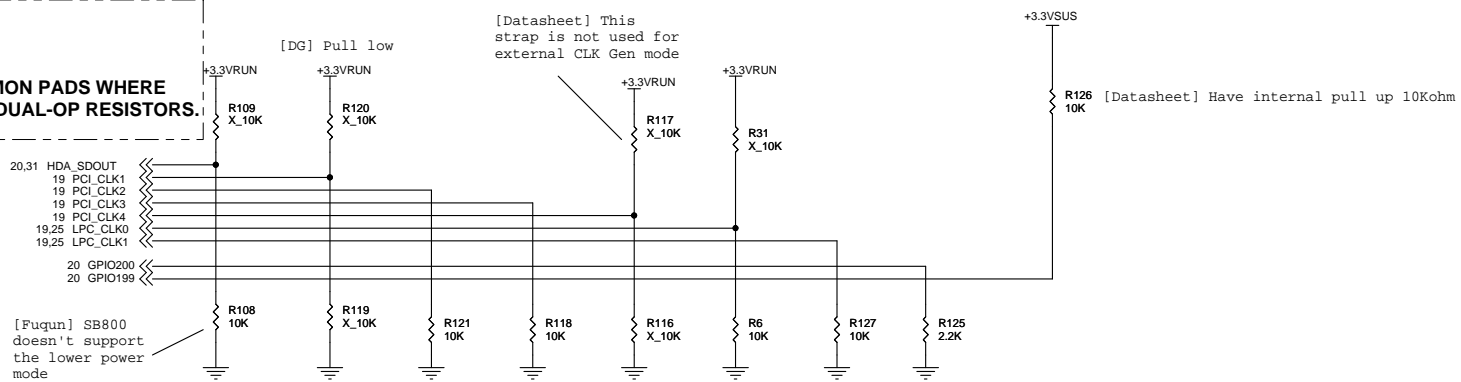


[CheckList] 1.5VSUS or 3.3VSUS

<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-168x</b>		
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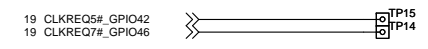
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



**REQUIRED STRAPS**

PULL HIGH	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

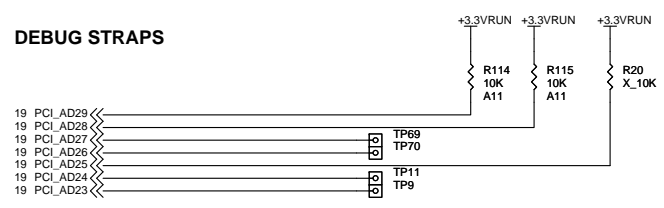
**SB PCIE EEPROM STRAPS**



PCI\_CLK1(SMSC\_CLK)-->SB820M: Only provision for pull-down is required, not installed by default--checklist  
 [Fuqun] GPIO199 NC in checklist  
 [Fuqun] PCI\_CLK4 high or low?

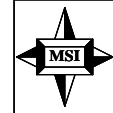
SB800 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

**DEBUG STRAPS**



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

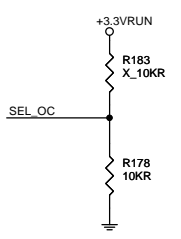
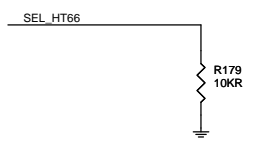
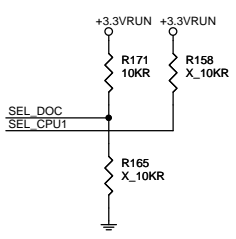
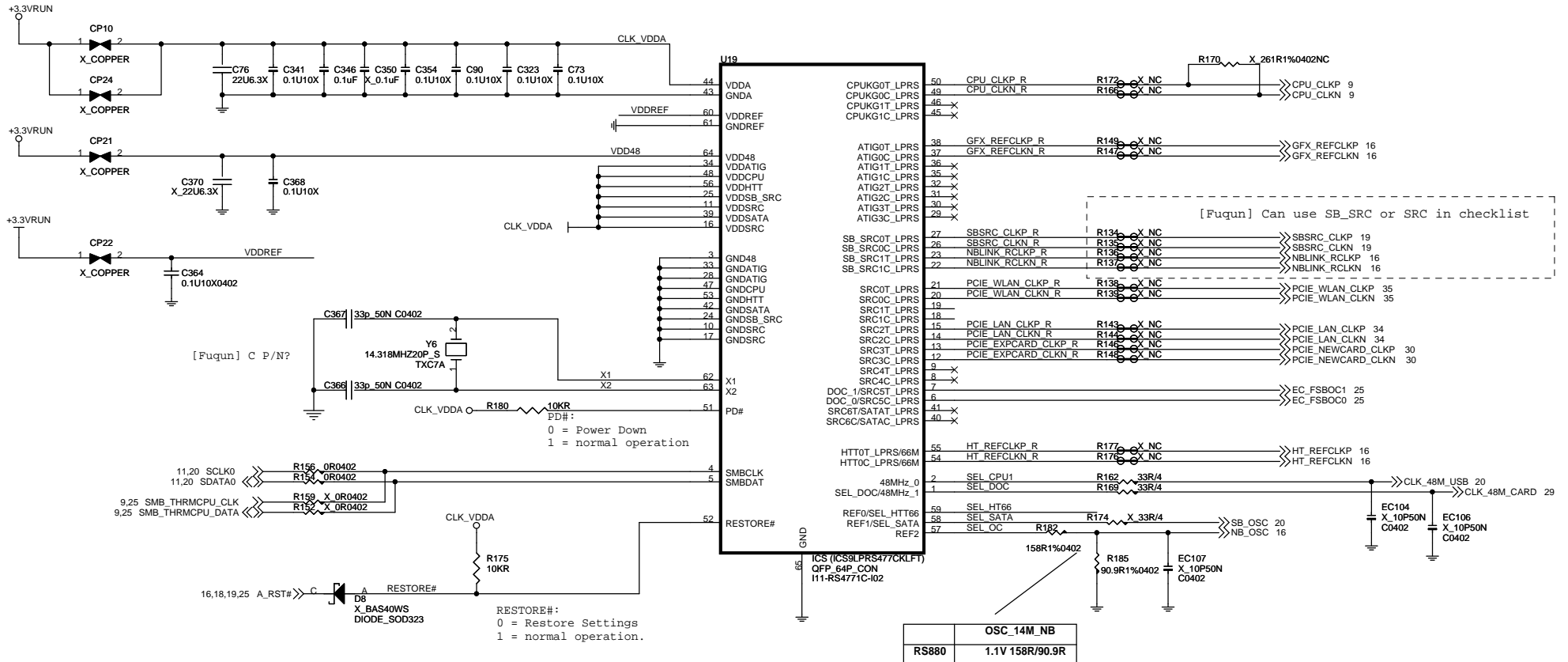
PCI23/24/26/27 have internal pull high 15kohm, But PCI25?  
 Why PCI28/29 pull high?



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-168x</b>		
Size Custom	Document Description <b>SB820-STRAPS</b>	Rev 0A
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- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U11
- 2- PUT DECOUPLING CAPS CLOSE TO U11 POWER PIN



SEL_DOC/48MHz-1	1	DOC INPUT
	0	SRCLK5
SEL_CPU1/48MHz-2	1	SRCLK7
	0	CPUKG1

SEL_HT66	1	66 MHz 3.3V single ended HTT clock
	0	100 MHz differential HTT clock
SEL_SATA	1	100MHz differential spreading SRC clock
	0	100 MHz spreading differential SATA clock

SEL_OC	1	Higher overclocking ability
	0	limited overclocking ability

	OSC_14M_NB
RS880	1.1V 158R/90.9R

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

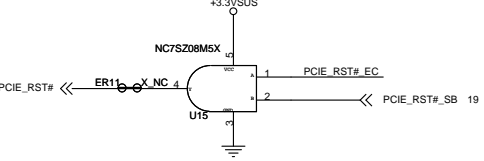
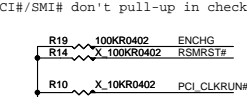
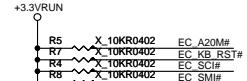
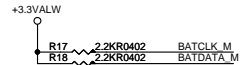
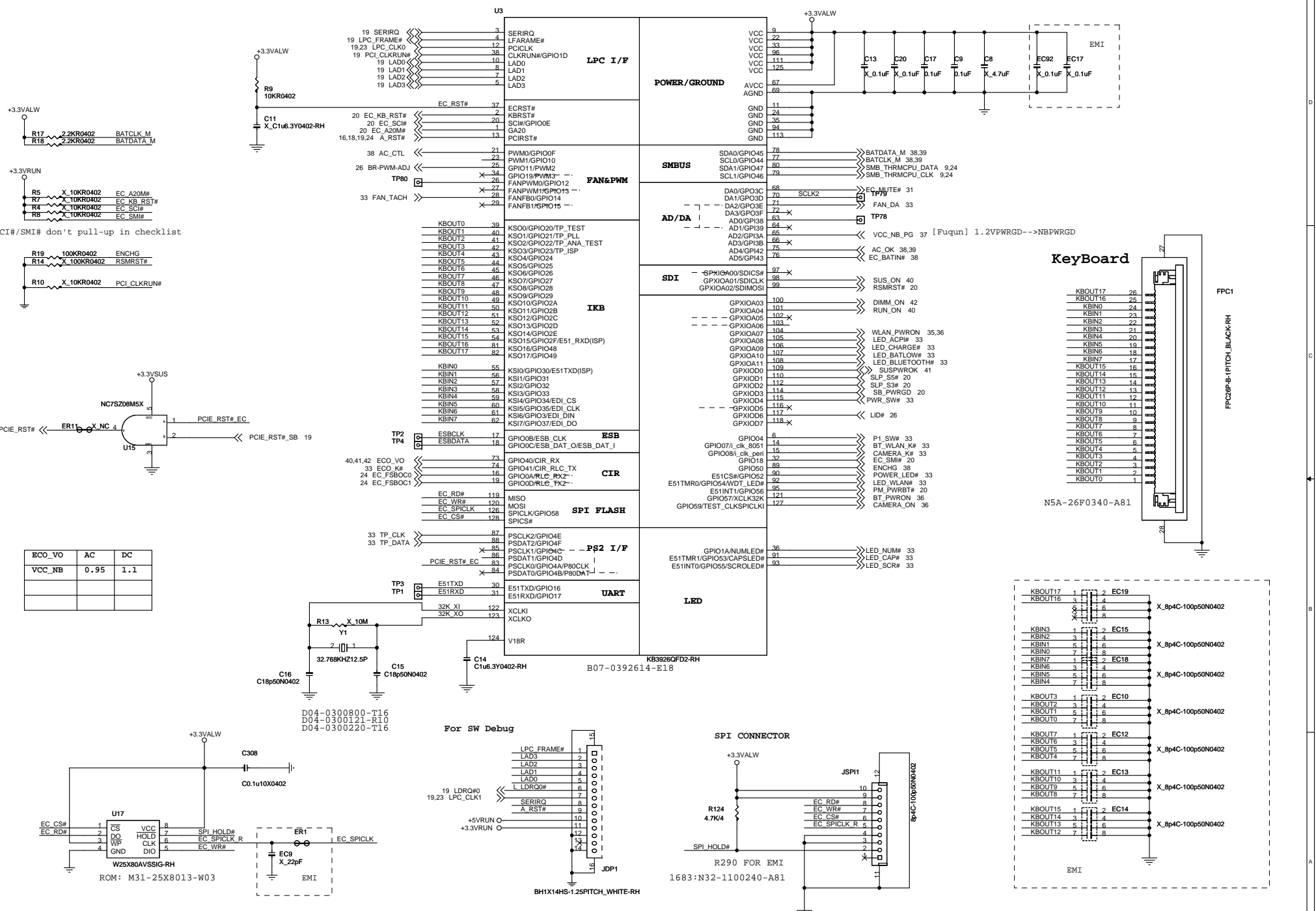
\* RS780 can be used as clock buffer to output two PCIe reference clocks  
By default, chip will configured as input mode, BIOS can program it to output mode.

**MICRO-STAR INT'L CO.,LTD**

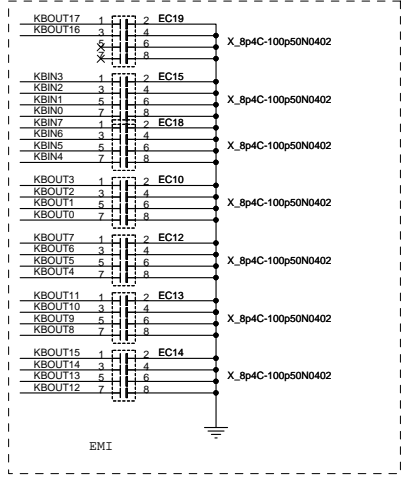
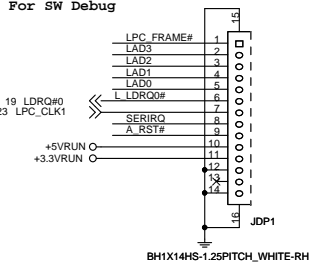
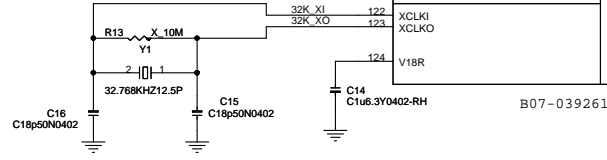
**MS-168x**

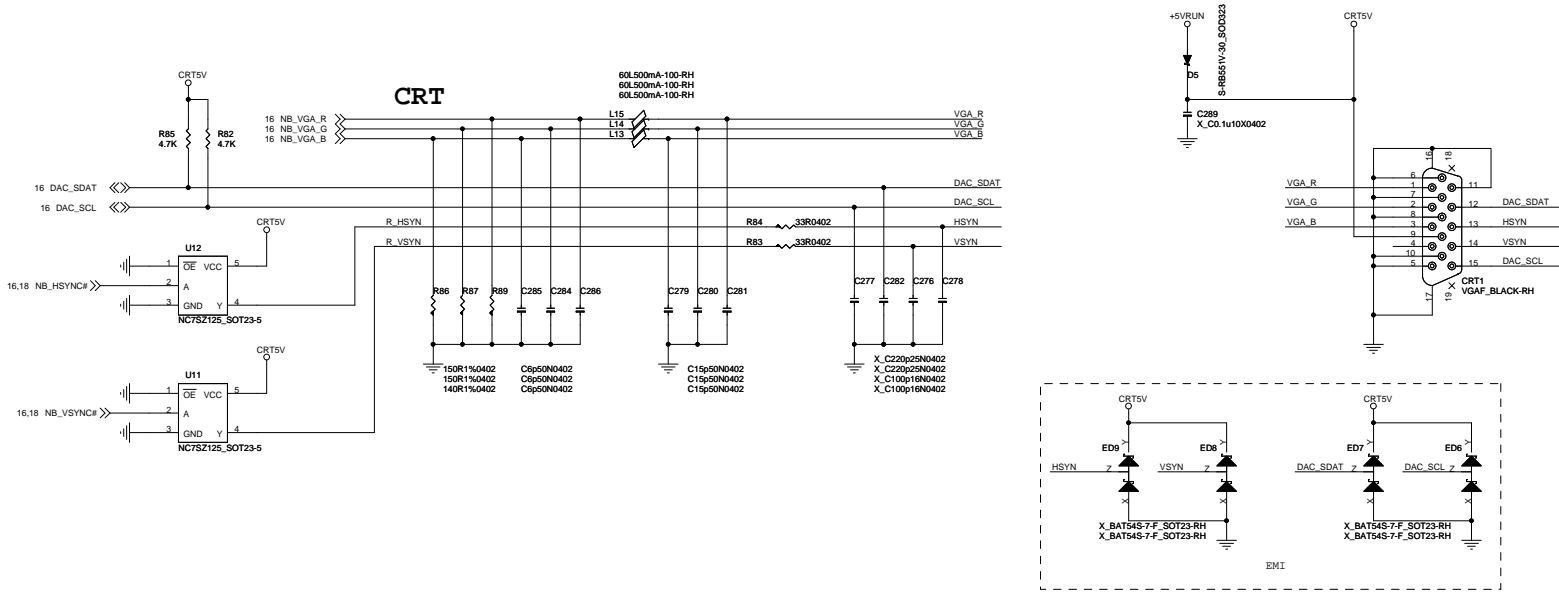
Size Custom	Document Description <b>CLK GEN</b>	Rev 0A
Date: Friday, February 05, 2010		Sheet 24 of 50



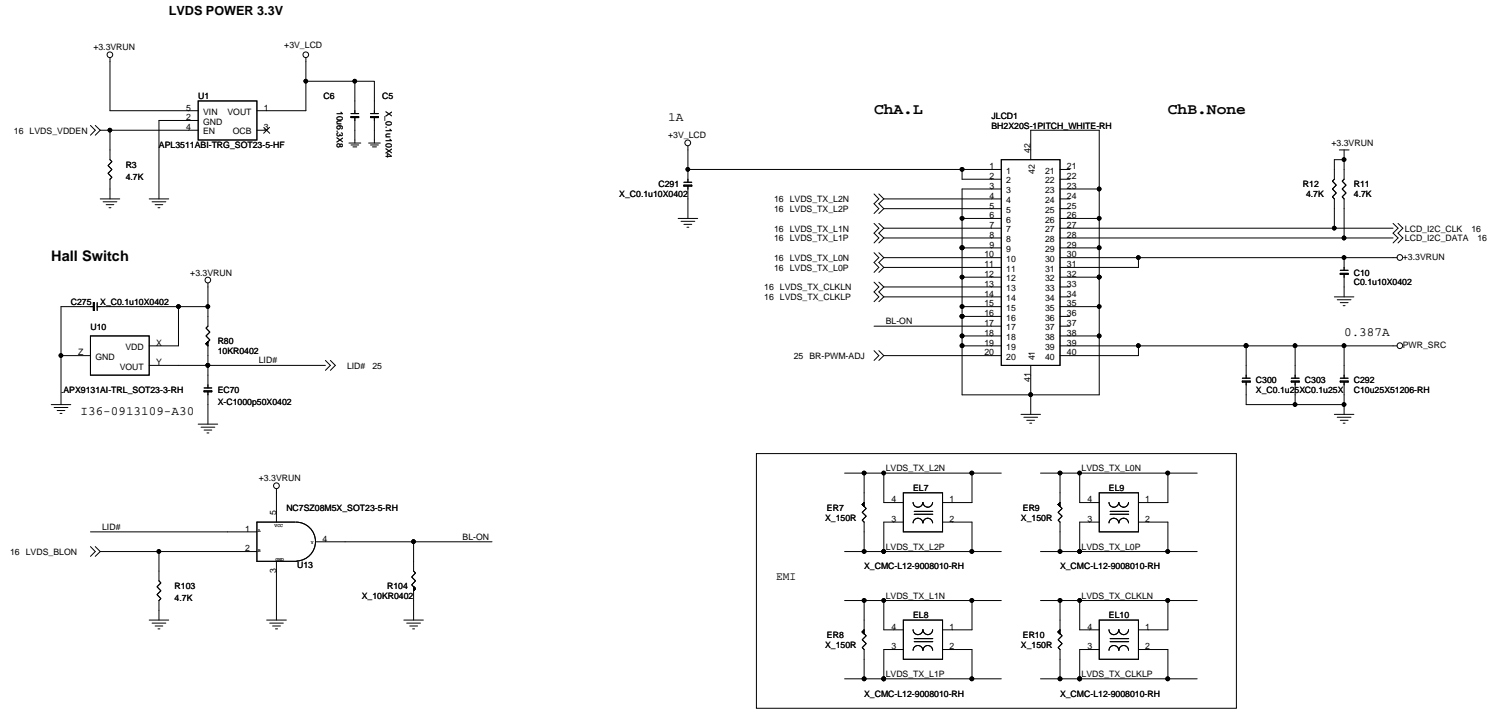


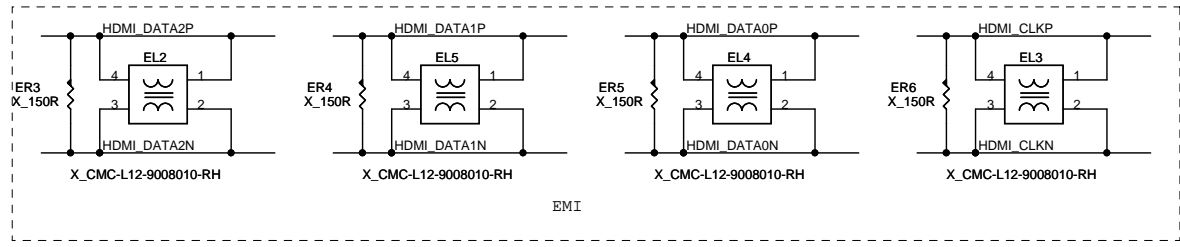
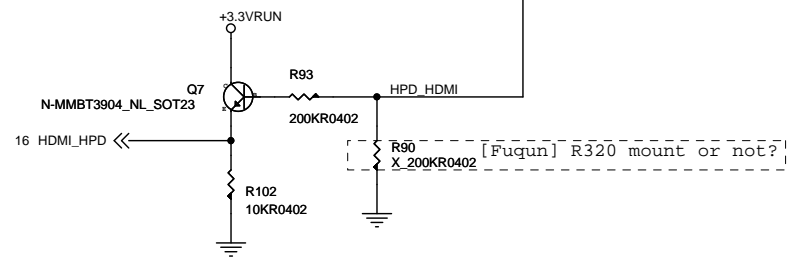
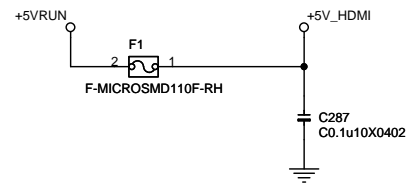
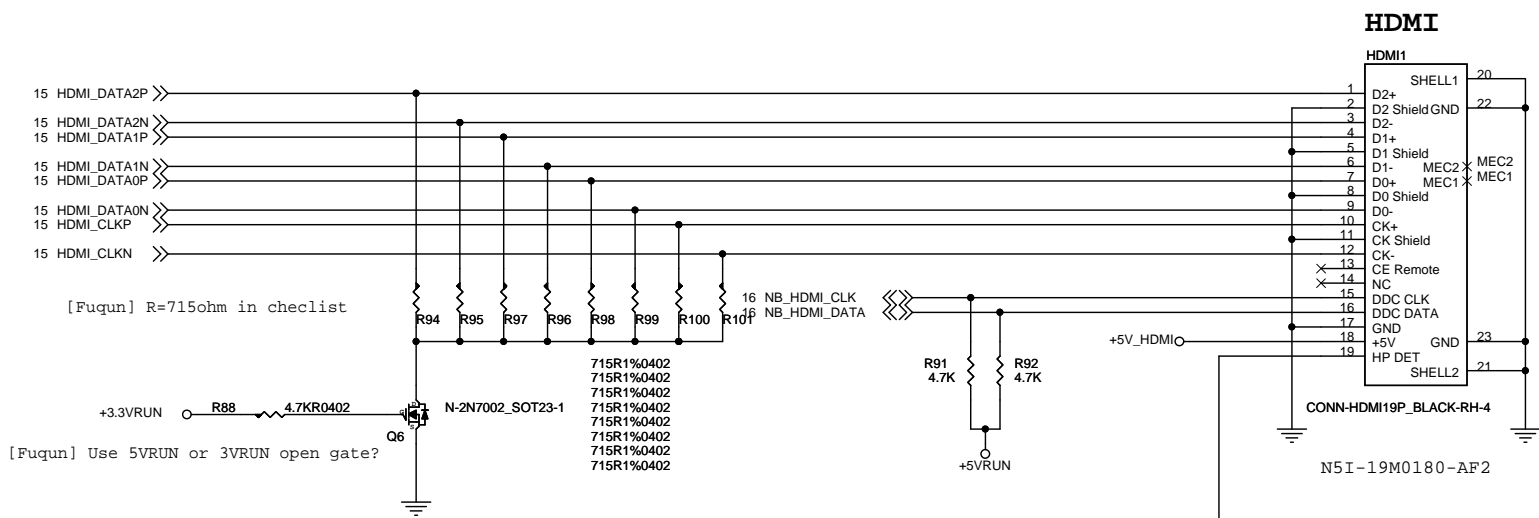
ECO_VO	AC	DC
VCC_NB	0.95	1.1



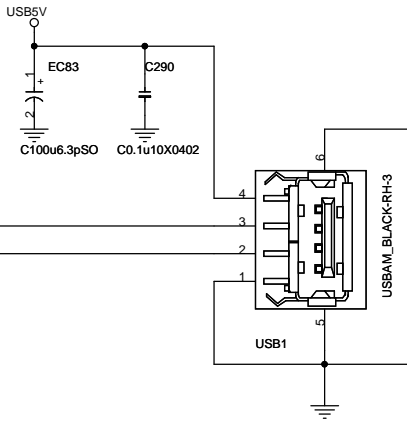
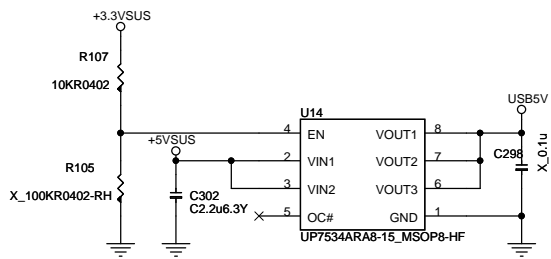


**LVDS**

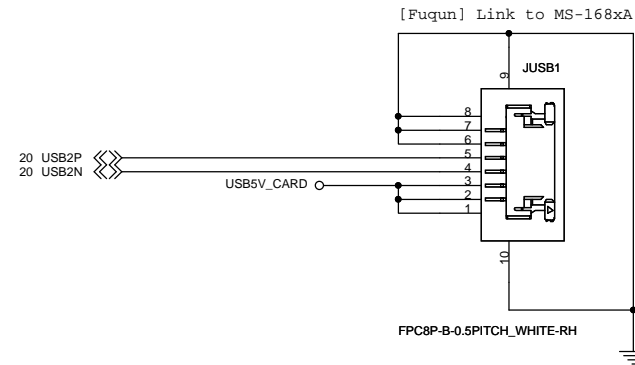
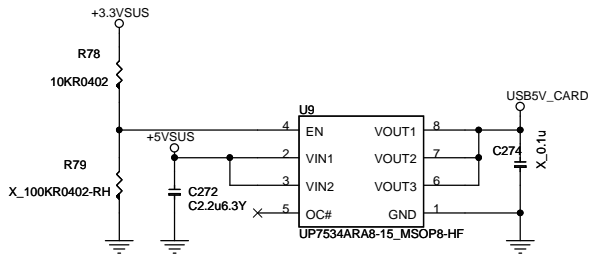
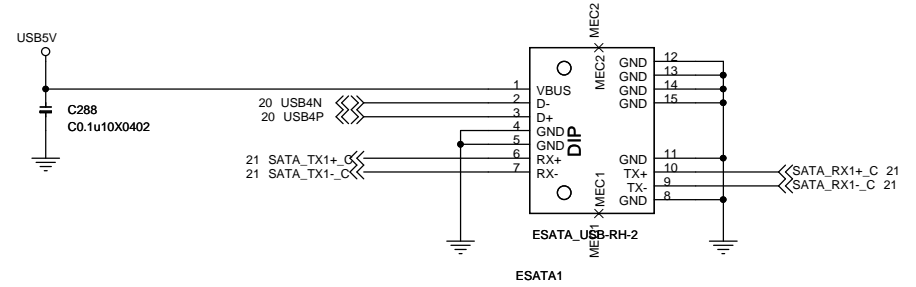
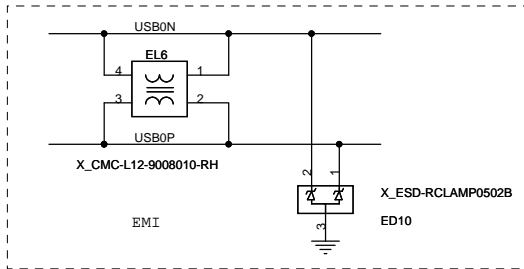





<b>MSI</b>		
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-168x</b>		
Size B	Document Description <b>HDMI</b>	Rev 0A
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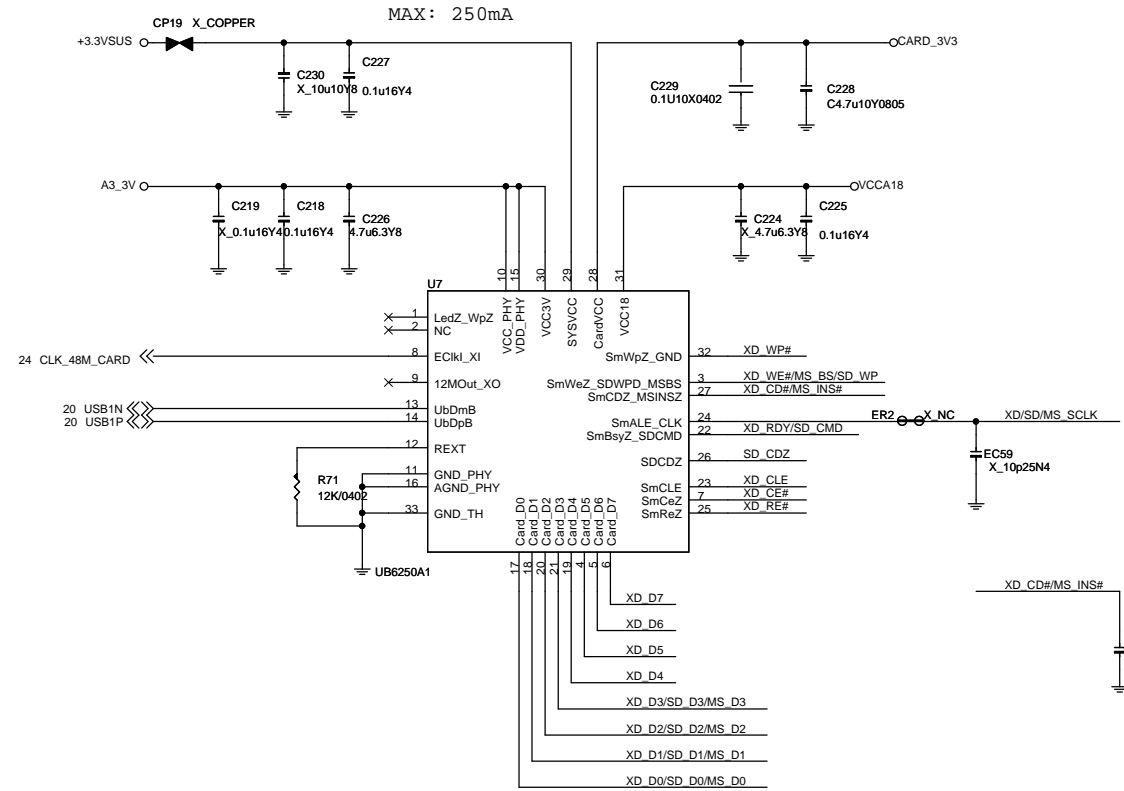


20 USB0N  
20 USB0P

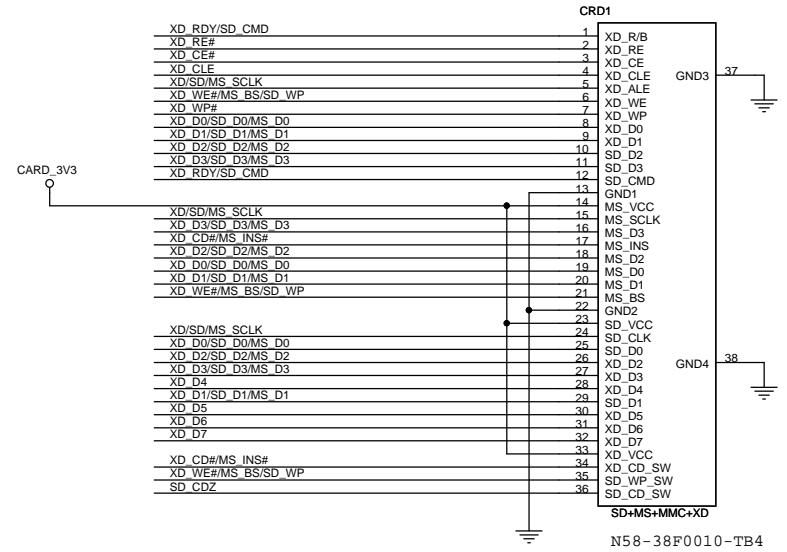


			<b>MICRO-STAR INT'L CO.,LTD</b>	
			<b>MS-168x</b>	
Size Custom	Document Description <b>USB and ESATA</b>		Rev 0A	
Date: Friday, February 05, 2010		Sheet 28 of 50		1

# Card Reader controller



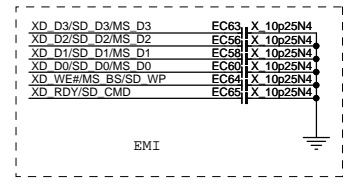
# Flash Card Socket



ENE UB6250 USB20 Flash Card Reader Controller

Pins for SD, MMC, MS, and xD memory cards

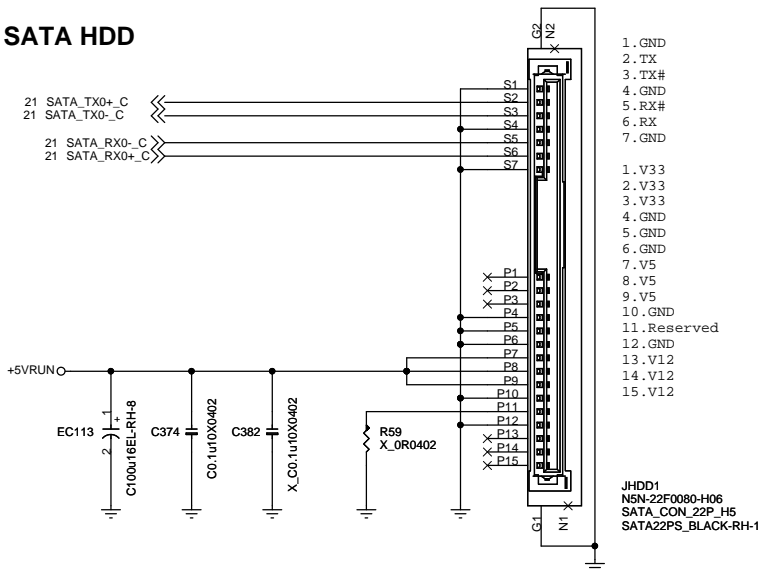
Name	No	I/O	XD	SD	MMC	MS
xDceZ	7	O	xD card EN			
xDcle	23	O	xD CMD latch EN			
xDAle	24	O	xD ADDR latch EN	SD clock	MMC clock	MS serial clock
xDbsyZ	22	B	xD Ready/busy	SD CMD/response	MMC CMD/response	
xDData0	17	B	xD D0	SD D0	MMC D0	MS D0
xDData1	18	B	xD D1	SD D1	MMC D1	MS D1
xDData2	20	B	xD D2	SD D2	MMC D2	MS D2
xDData3	21	B	xD D3	SD D3	MMC D3	MS D3
xDData4	19	B	xD D4		MMC D4	MS D4
xDData5	4	B	xD D5		MMC D5	MS D5
xDData6	5	B	xD D6		MMC D6	MS D6
xDData7	6	B	xD D7		MMC D7	MS D7
xDWeZ	3	B	xD W EN	SD WP		MS Busy
xDReZ	25	O	xD R EN			
xDWpZ	32	O	xD WP			
SDcdZ	26	I	SD CD		MMC CD	
xDcdZ	27	I	xD CD			MS CD



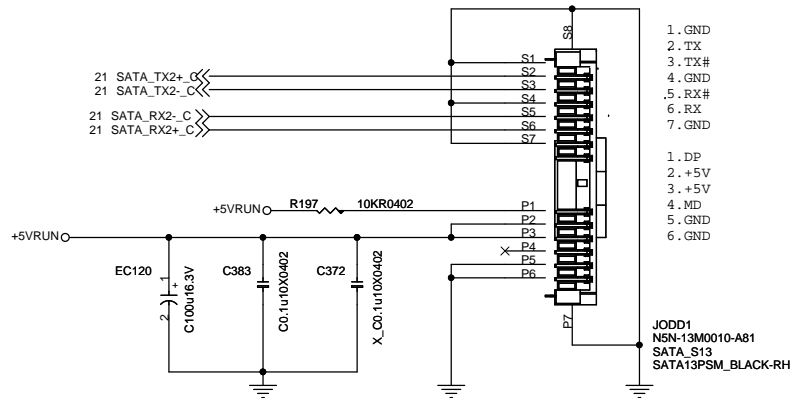
**MICRO-STAR INT'L CO.,LTD**  
**MS-168x**

Size Custom	Document Description <b>UB6250</b>	Rev 0A
Date: Friday, February 05, 2010		Sheet 29 of 52

### SATA HDD

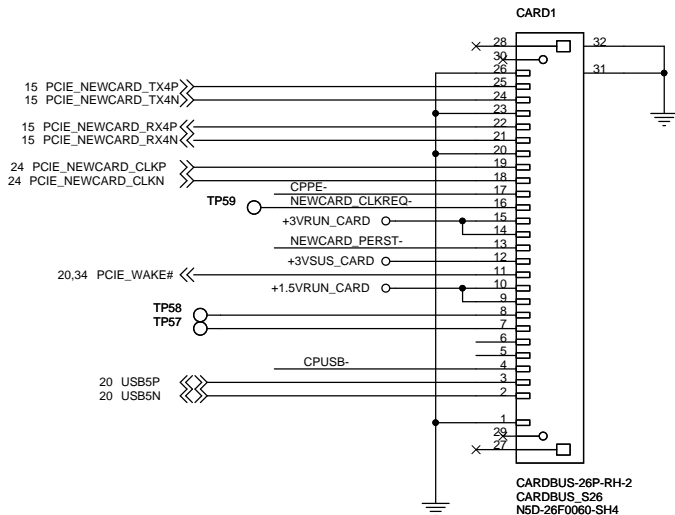
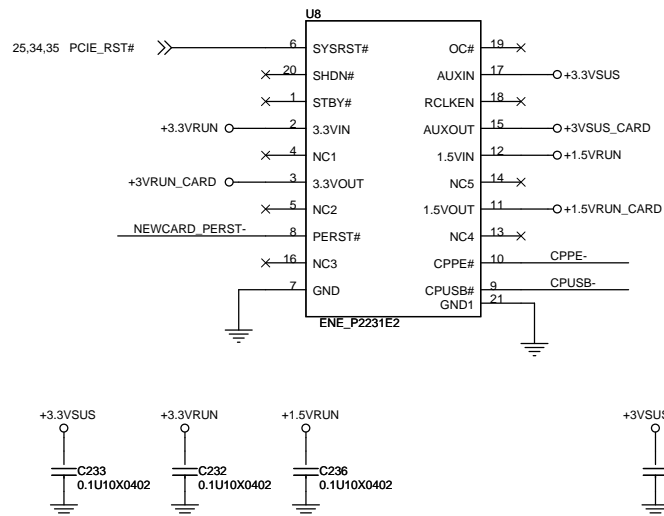


### SATA ODD



### NEW CARD

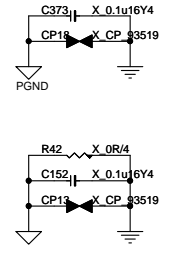
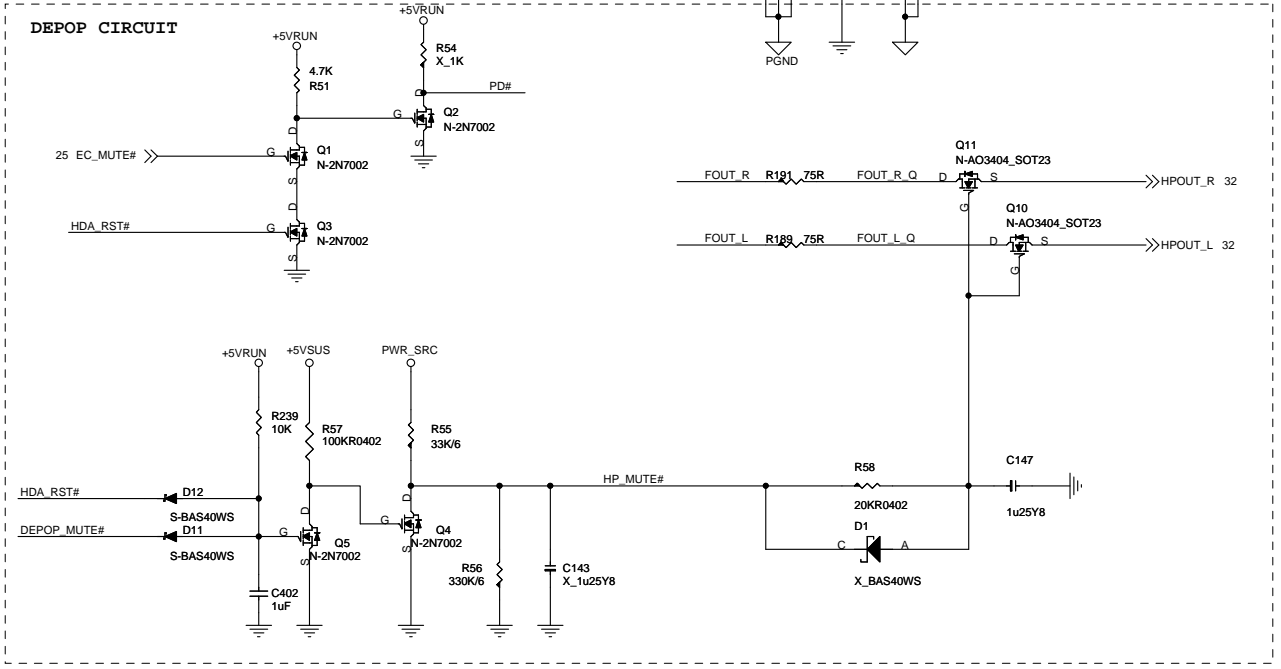
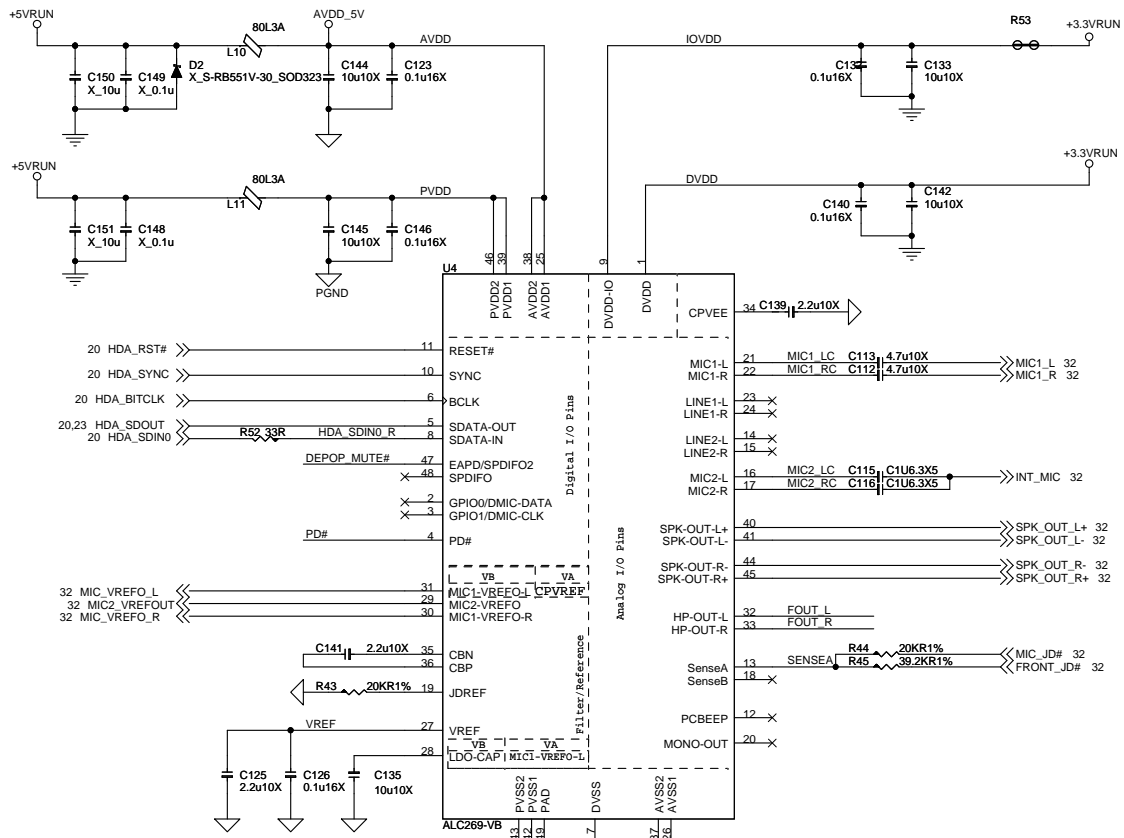
[CheckList] PCIE\_RST# and GPIO\_RST#-->PCIE device



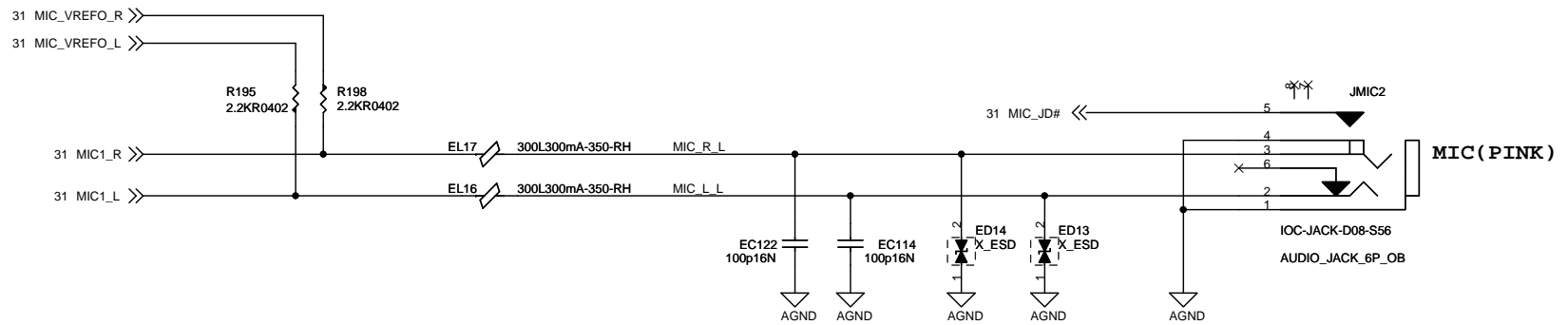
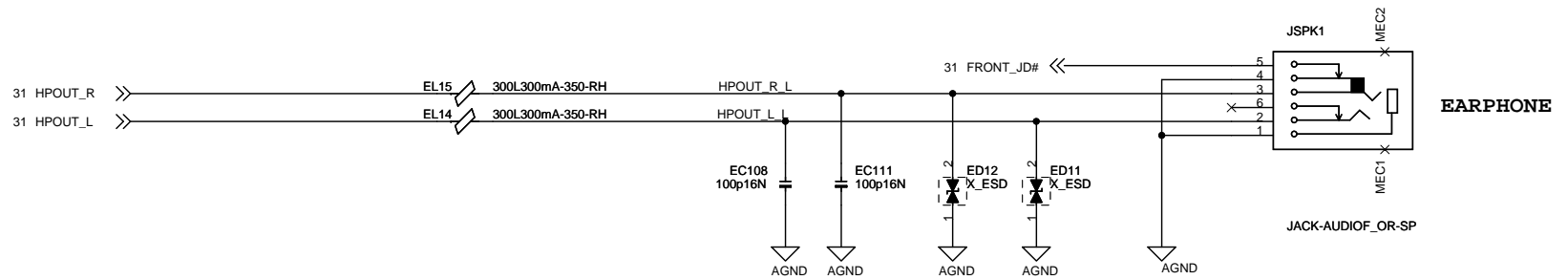
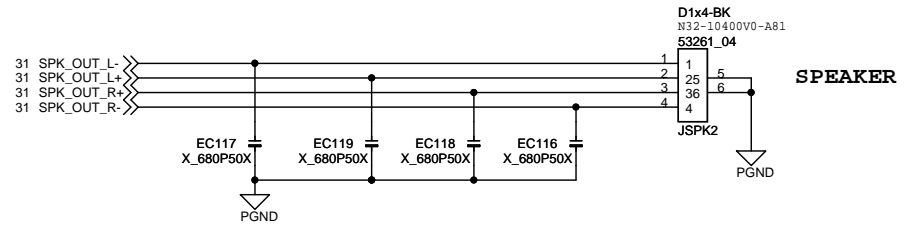
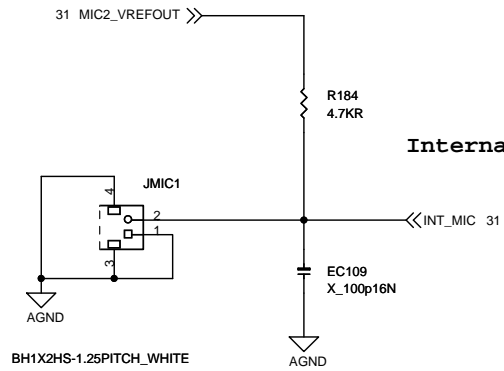
**MICRO-STAR INT'L CO.,LTD**

**MS-168x**

Size Custom	Document Description <b>HDD/ODD/NEW CARD</b>	Rev 0A
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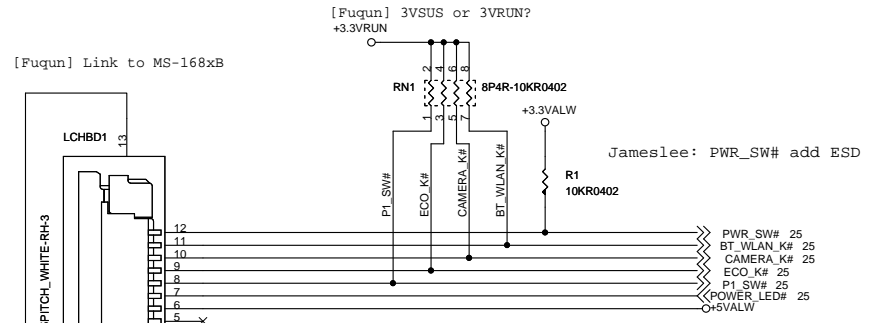
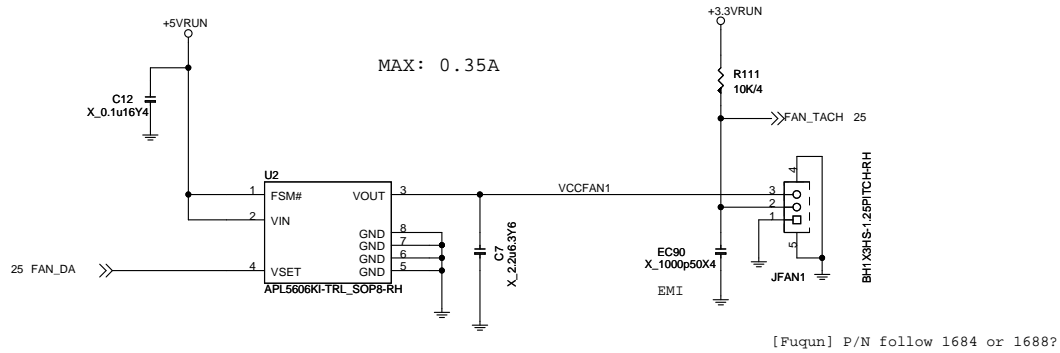
<b>MSI</b>		
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-168x</b>		
Size Custom	Document Description <b>ALC662</b>	Rev 0A
Date: Friday, February 05, 2010		Sheet 31 of 52



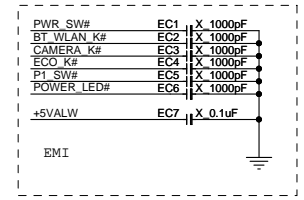
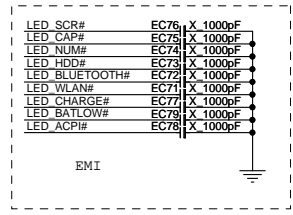
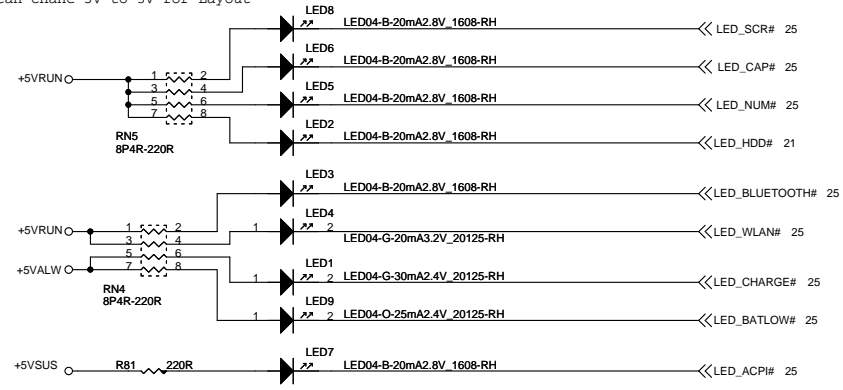
<b>MSI</b>			<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-168x</b>			<b>MS-168x</b>		
Size B	Document Description				Rev 0A
	<b>SPK / HP / MIC</b>				
Date: Friday, February 05, 2010				Sheet 32 of 52	



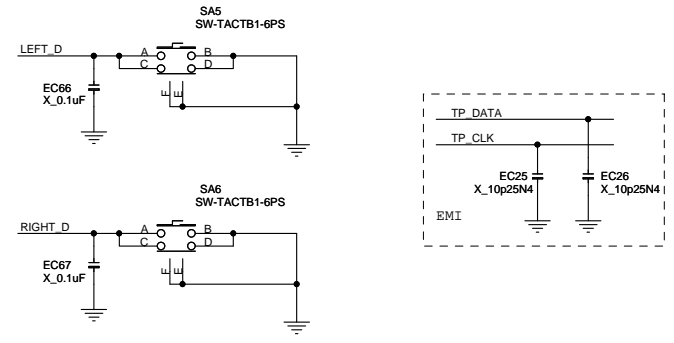
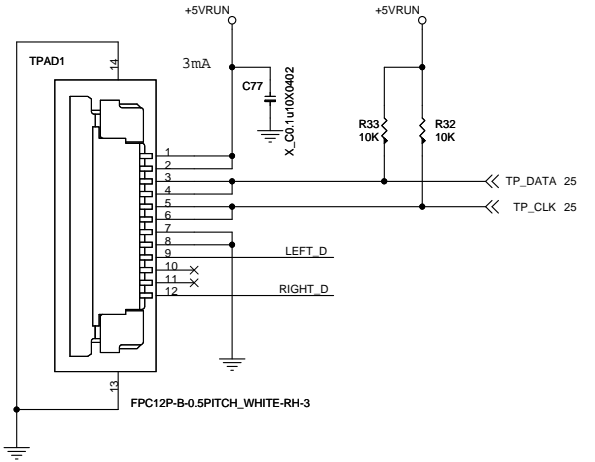
FAN

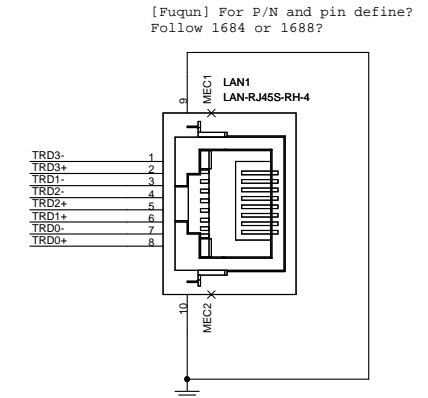
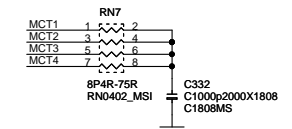
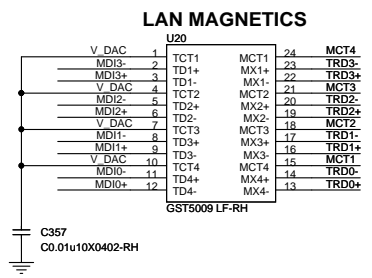
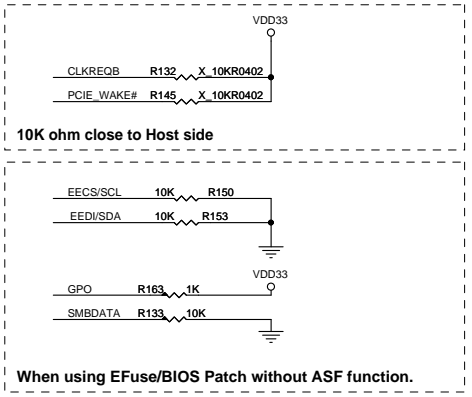
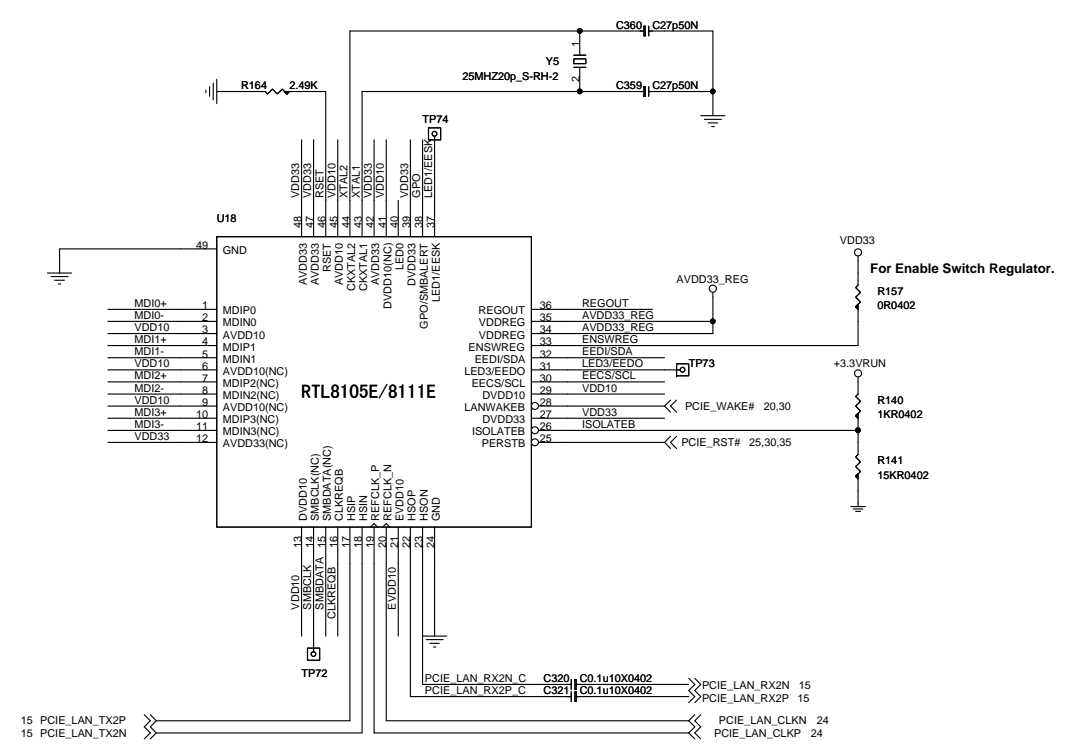
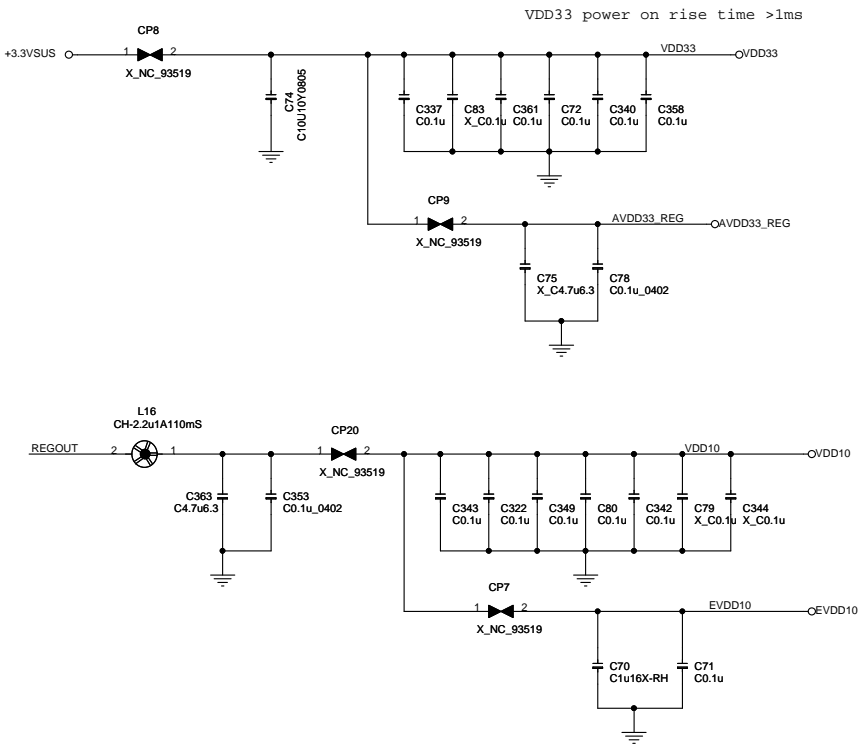


[Fuqun] Can chane 5V to 3V for Layout

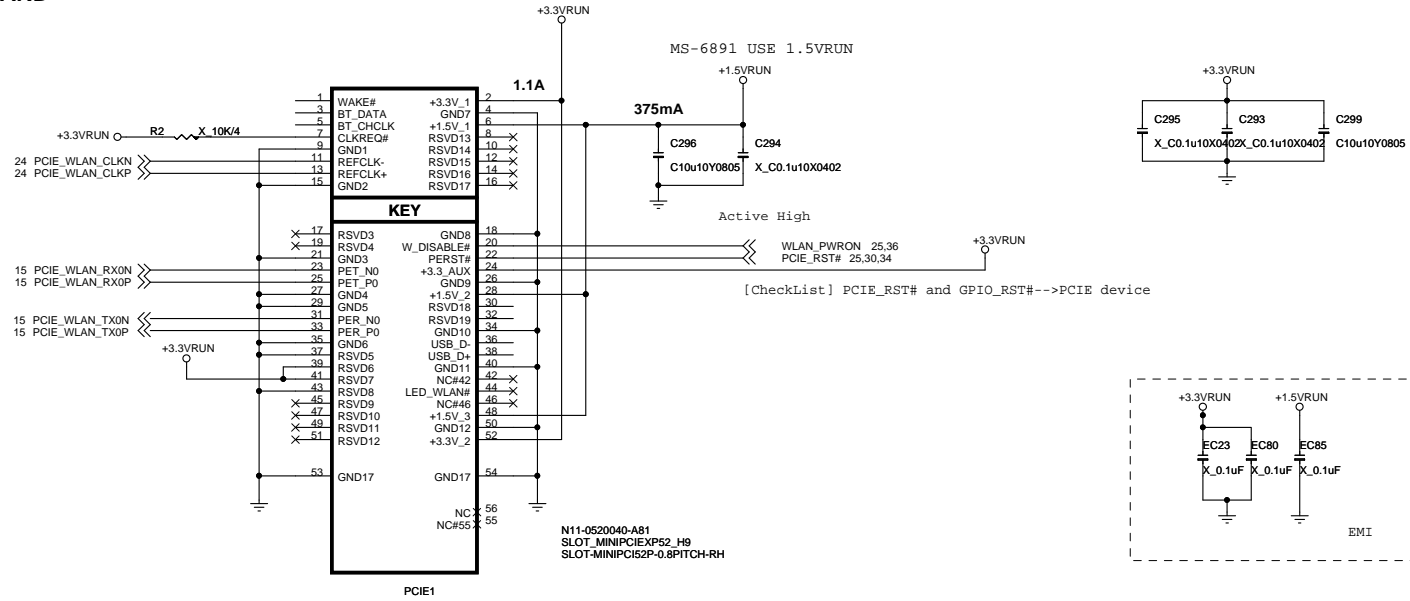


TOUCH PAD





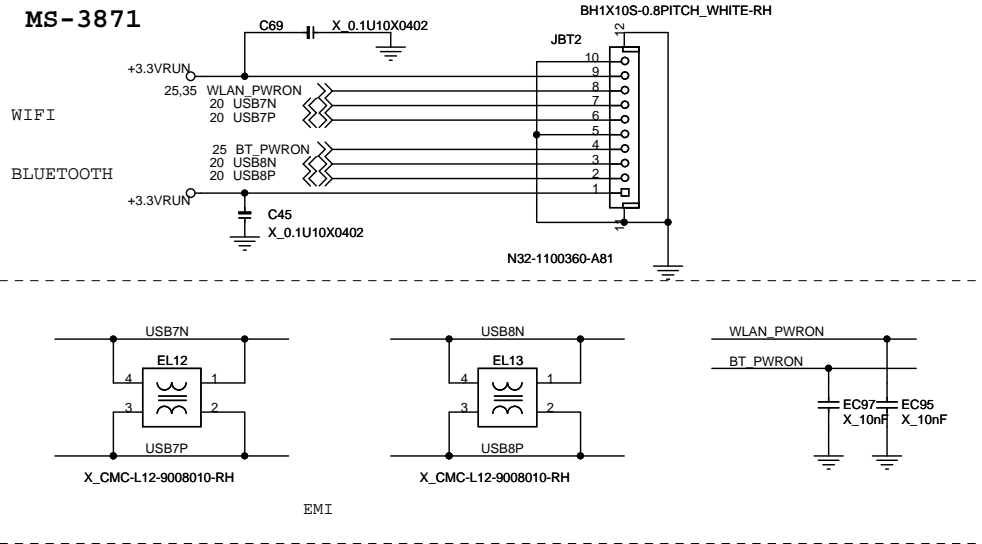
# WLAN CARD



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-168x</b>		
Size Custom	Document Description <b>MINI-PCIE</b>	Rev 0A
Date: Friday, February 05, 2010		Sheet 35 of 52

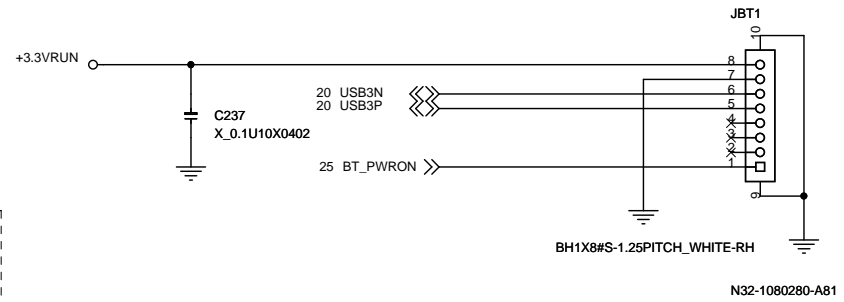
# BLUETOOTH

MS-3871



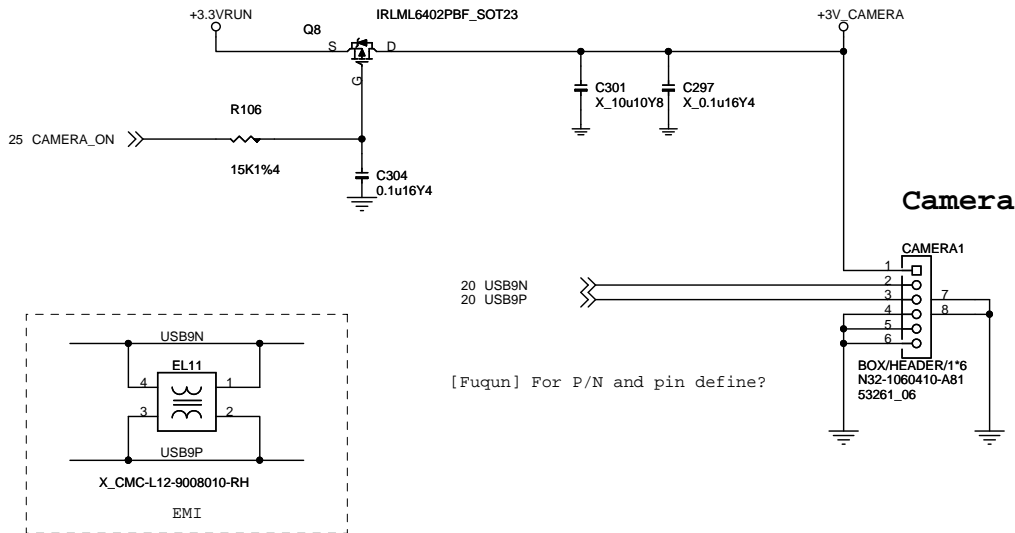
# BLUETOOTH


MS-3801

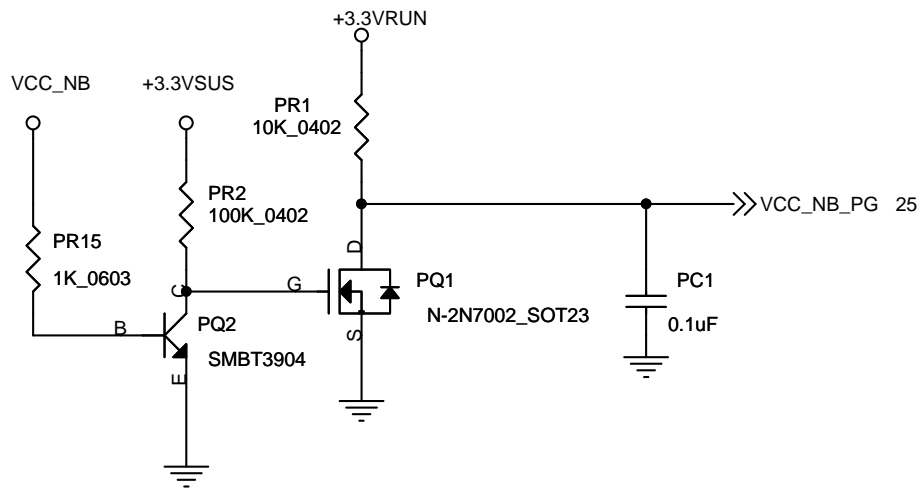



# CAMERA

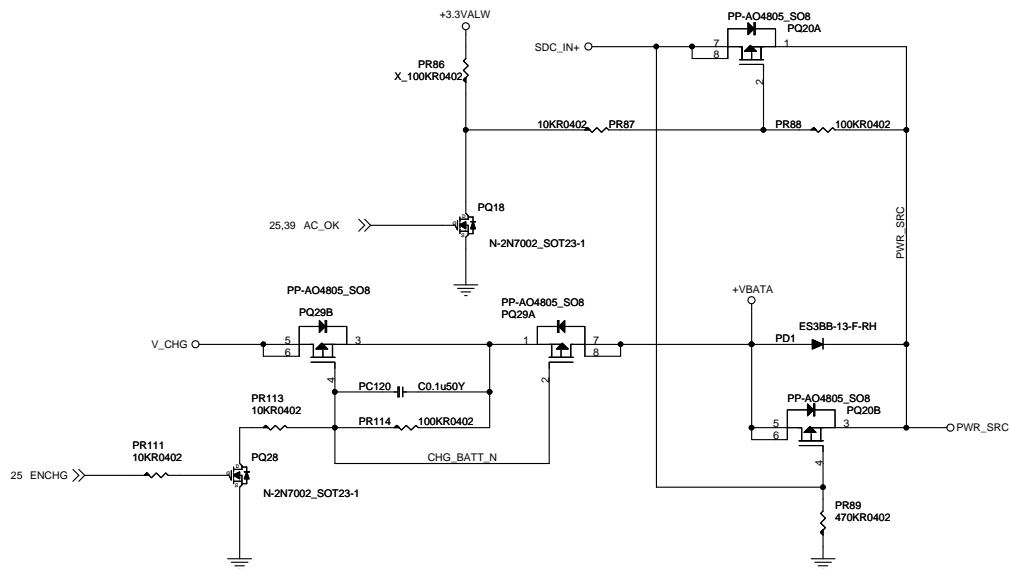
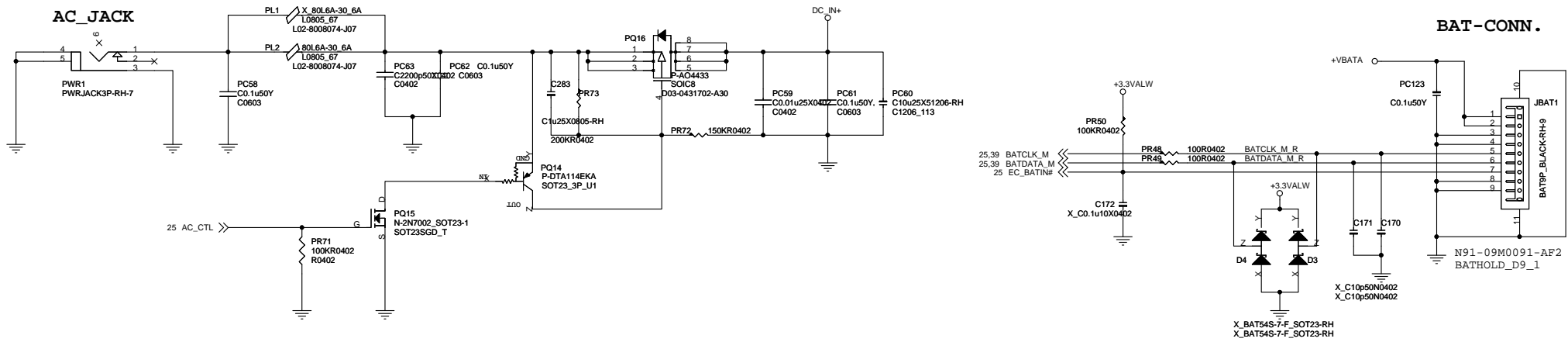
MAX: 130mA



			<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-168x</b>			<b>MS-168x</b>		
Size B	Document Description <b>CAMERA/BT</b>				Rev 0A
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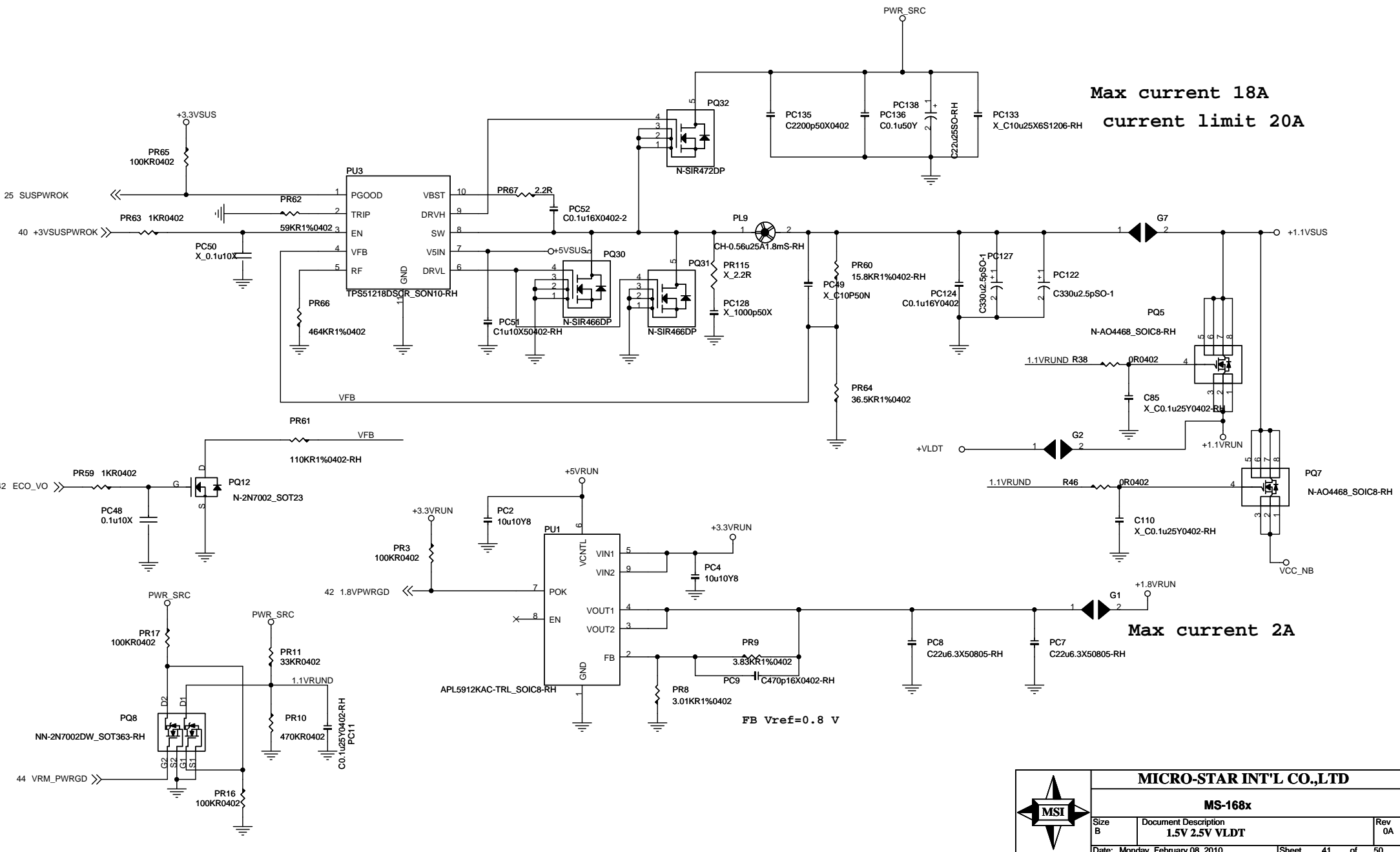
	<b>MICRO-STAR INT'L CO.,LTD</b>	
	<b>MS-168x</b>	
Size A	Document Description <b>POWER LOGIC</b>	Rev 0A
Date: Friday, February 05, 2010		Sheet 37 of 52











Max current 18A  
current limit 20A

Max current 2A

FB Vref=0.8 V

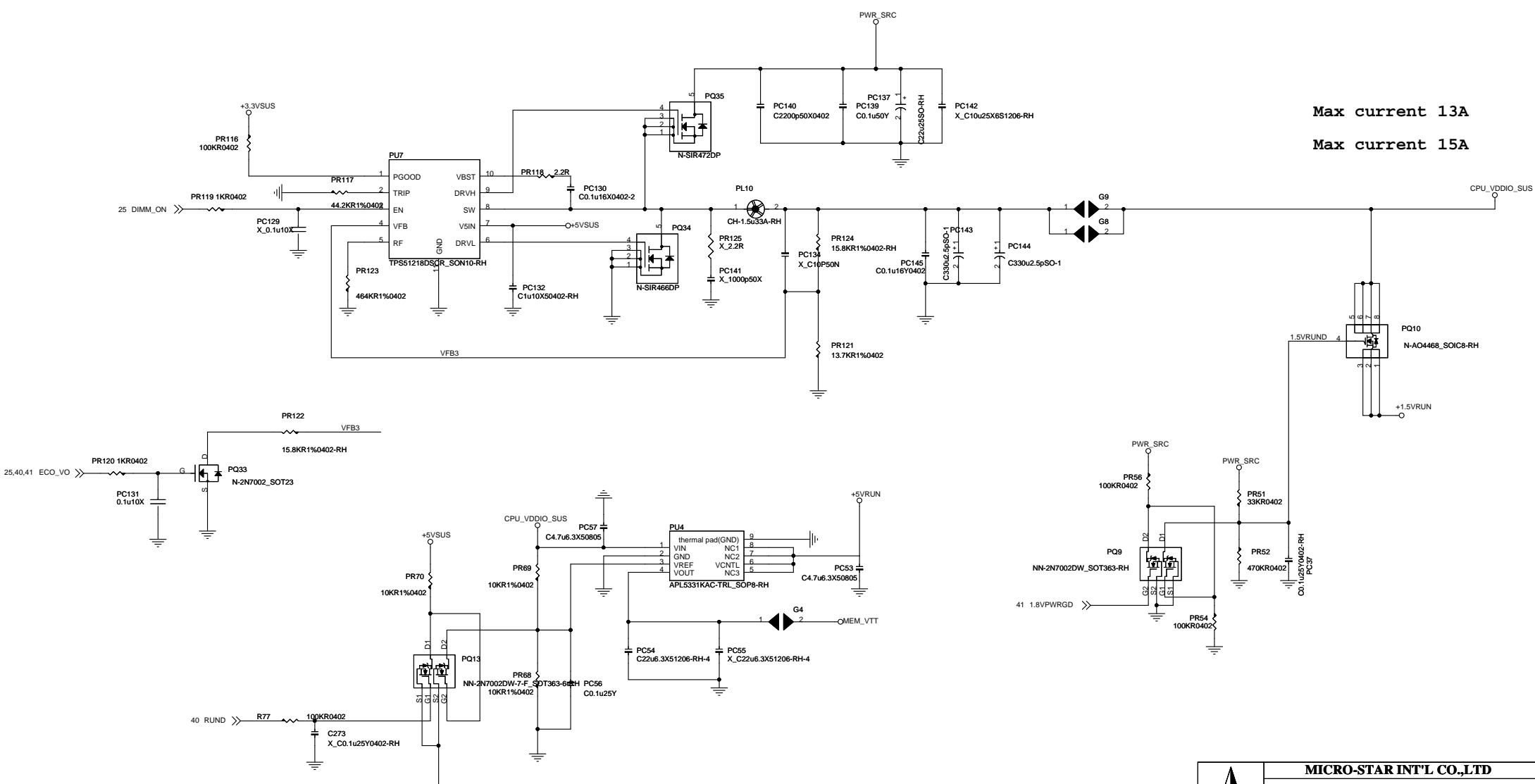


MICRO-STAR INT'L CO.,LTD

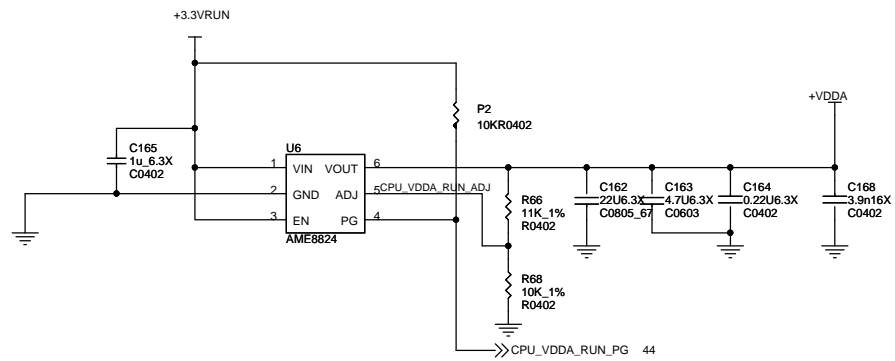
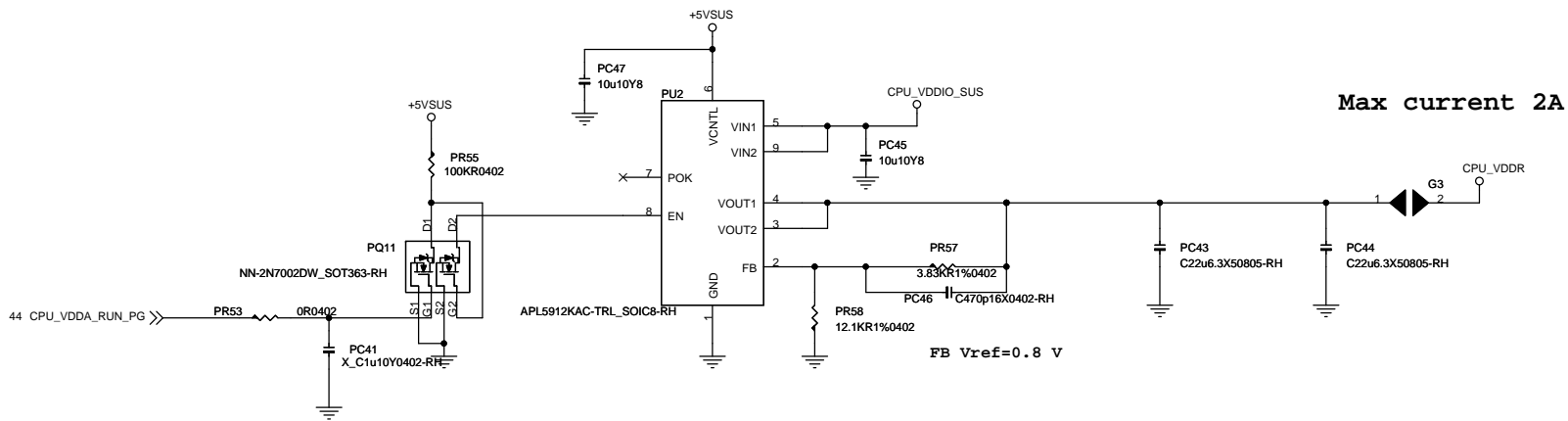
MS-168x

Size B	Document Description 1.5V 2.5V VLDT	Rev 0A
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Max current 13A  
Max current 15A



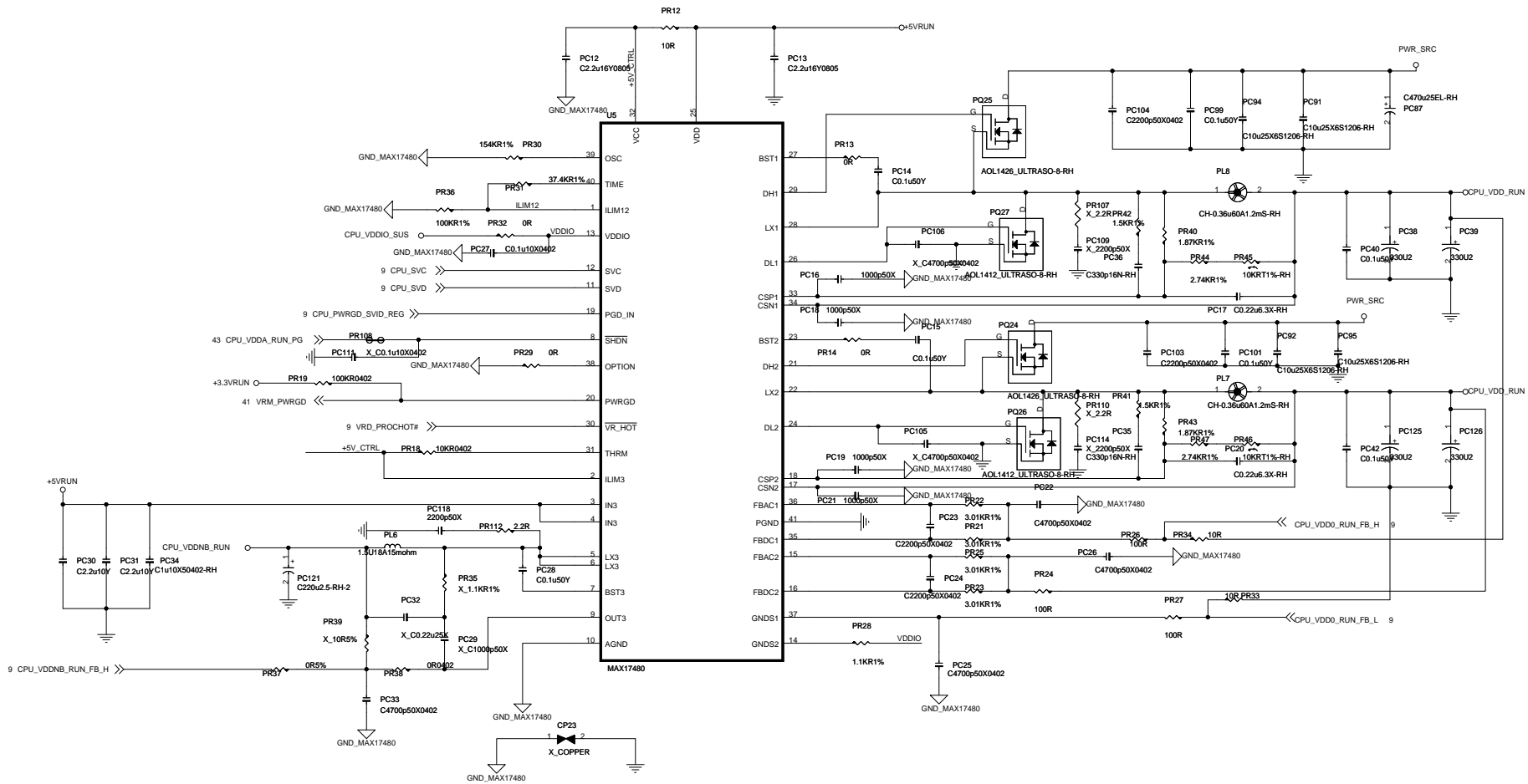
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-168x</b>		
Size Custom	Document Description <b>DDR POWER</b>	Rev 0A
Date: Monday, February 08, 2010		Sheet 42 of 50

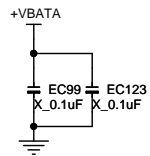
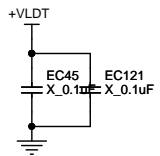
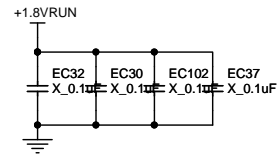
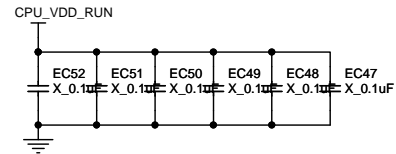
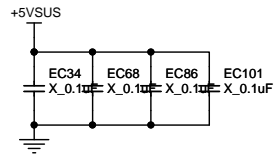
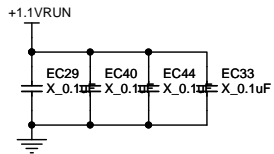
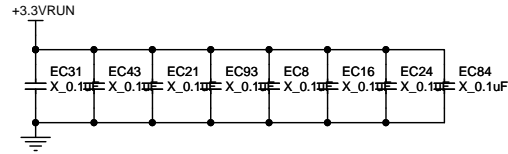
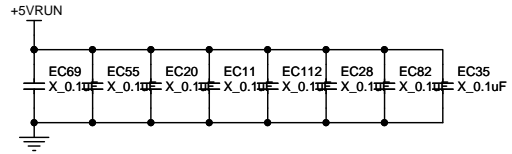
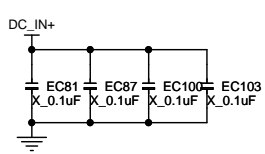
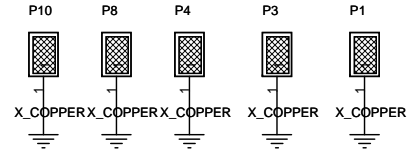
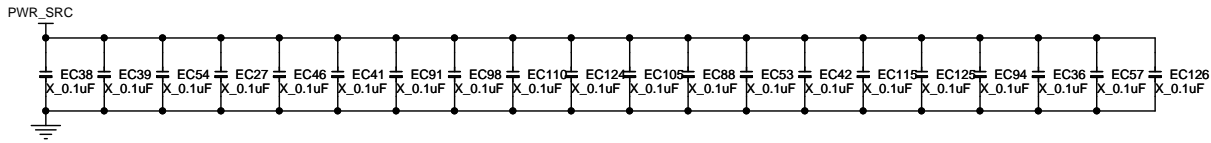
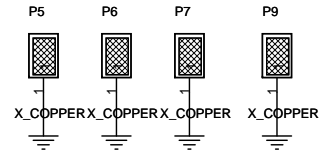
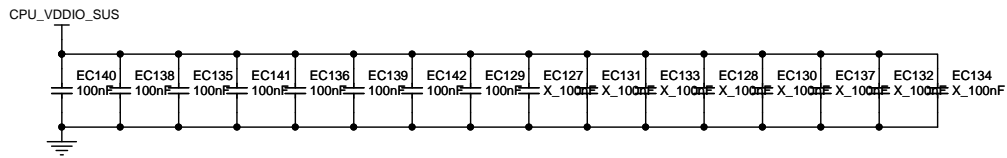



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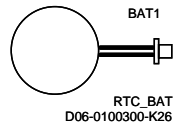
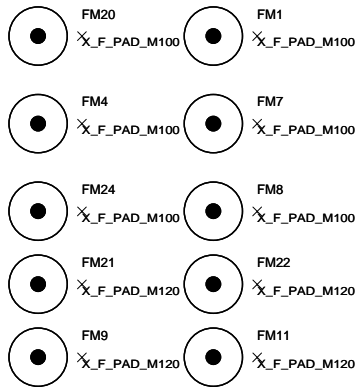
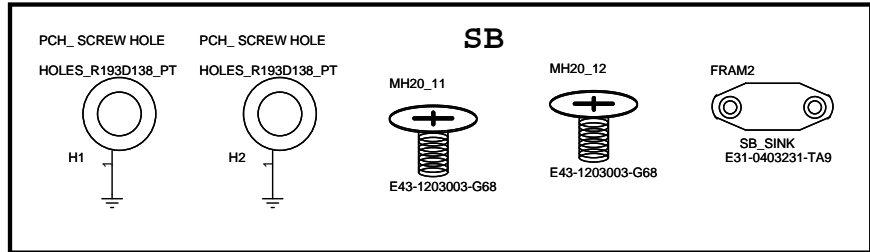
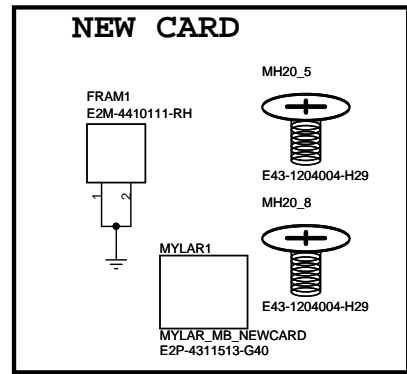
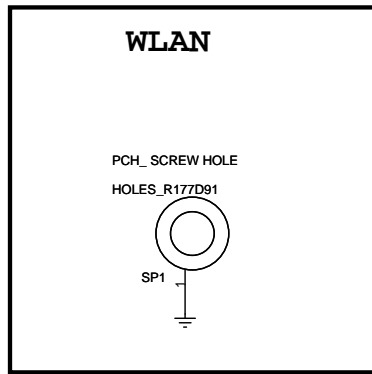
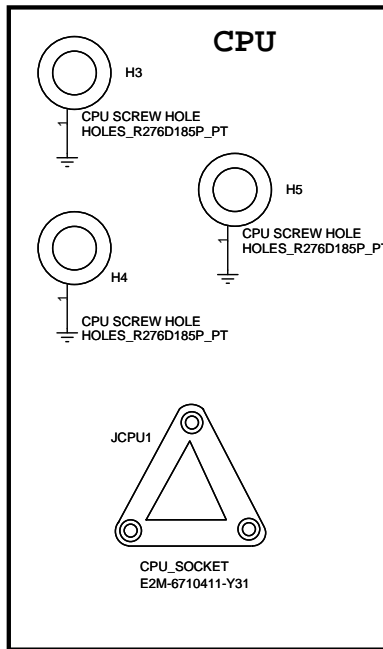
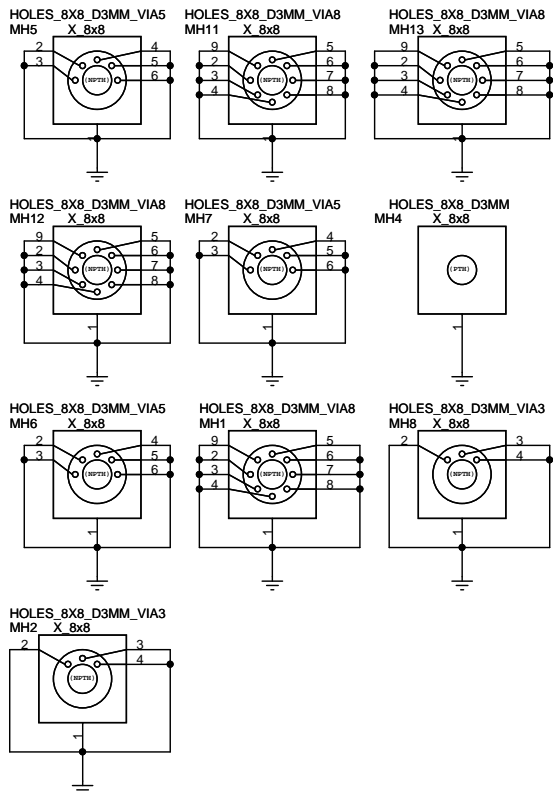
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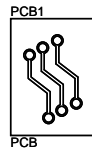
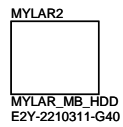





			<b>MICRO-STAR INT'L CO.,LTD</b>	
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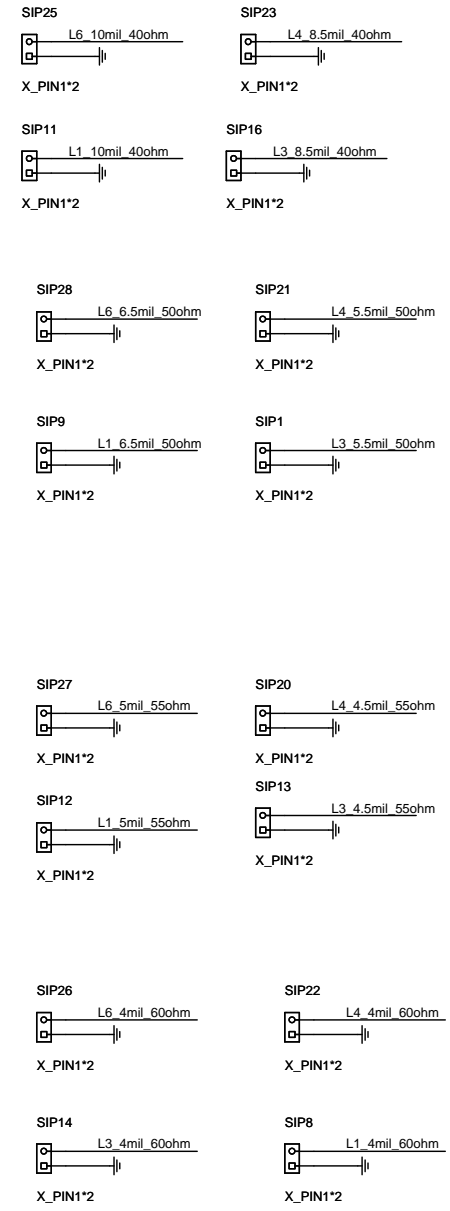


**FOR HDD**

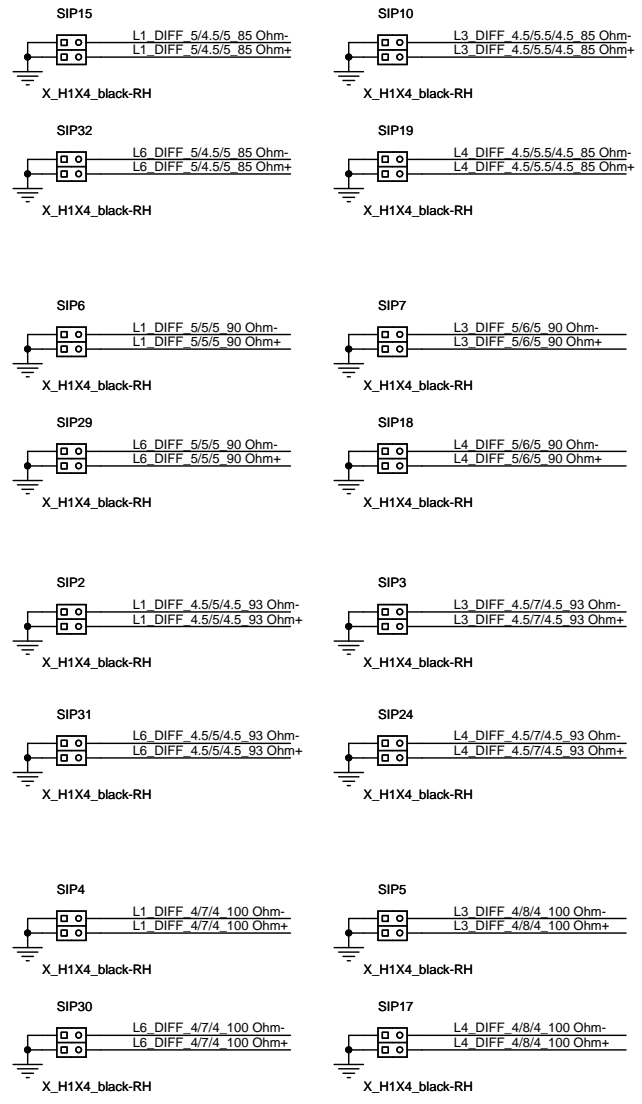


			<b>MICRO-STAR INT'L CO.,LTD</b>		
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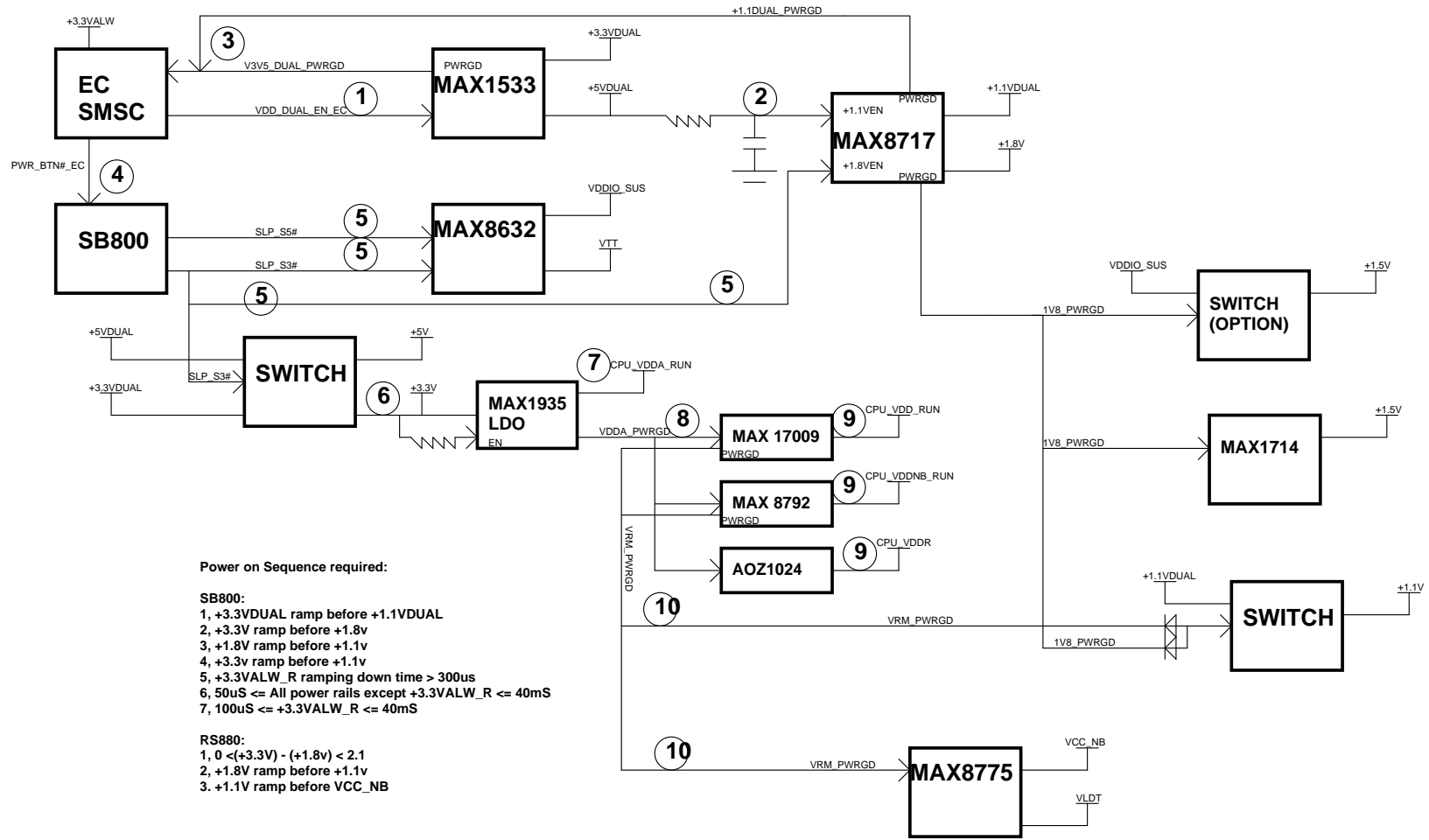
**Single ended**



**Differential signal**



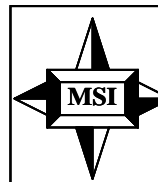
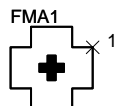
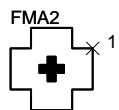
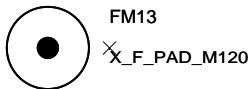
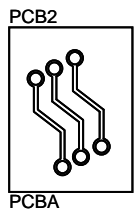
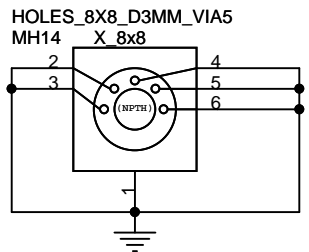
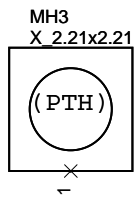
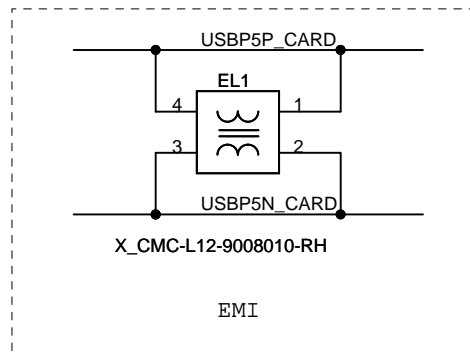
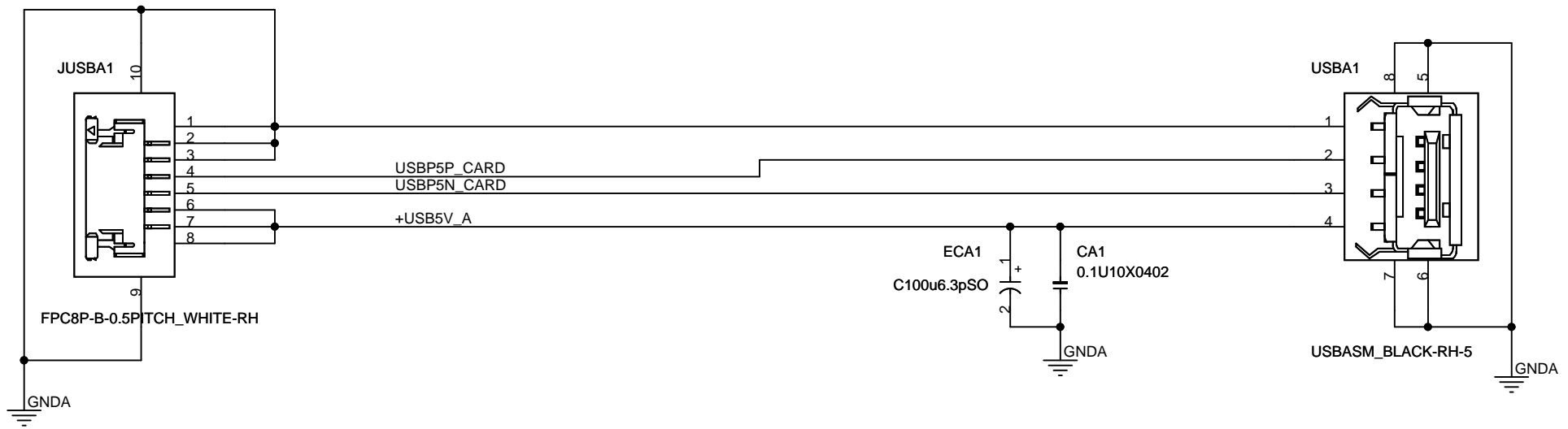
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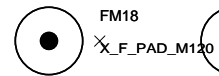
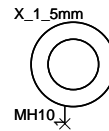
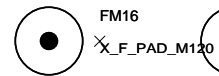
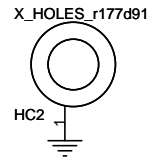
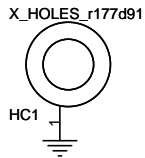
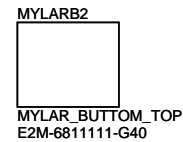
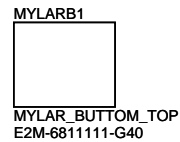
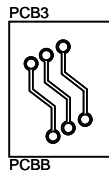
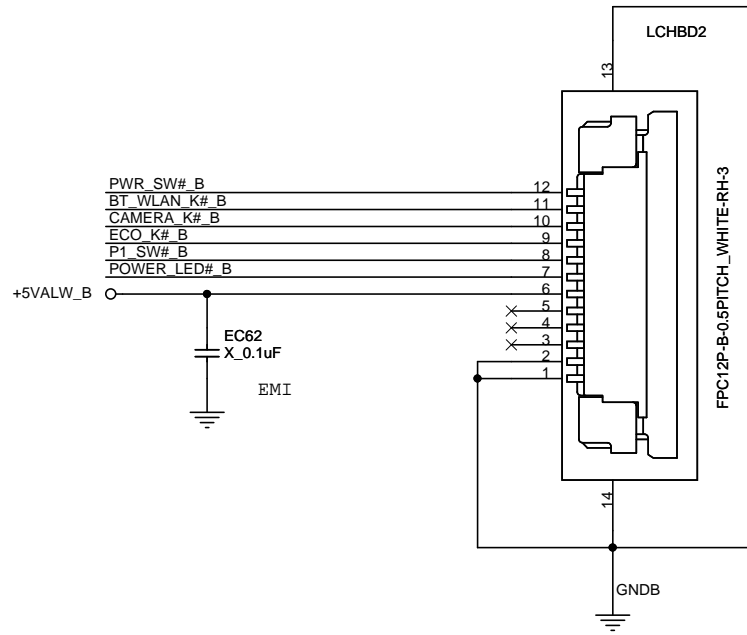
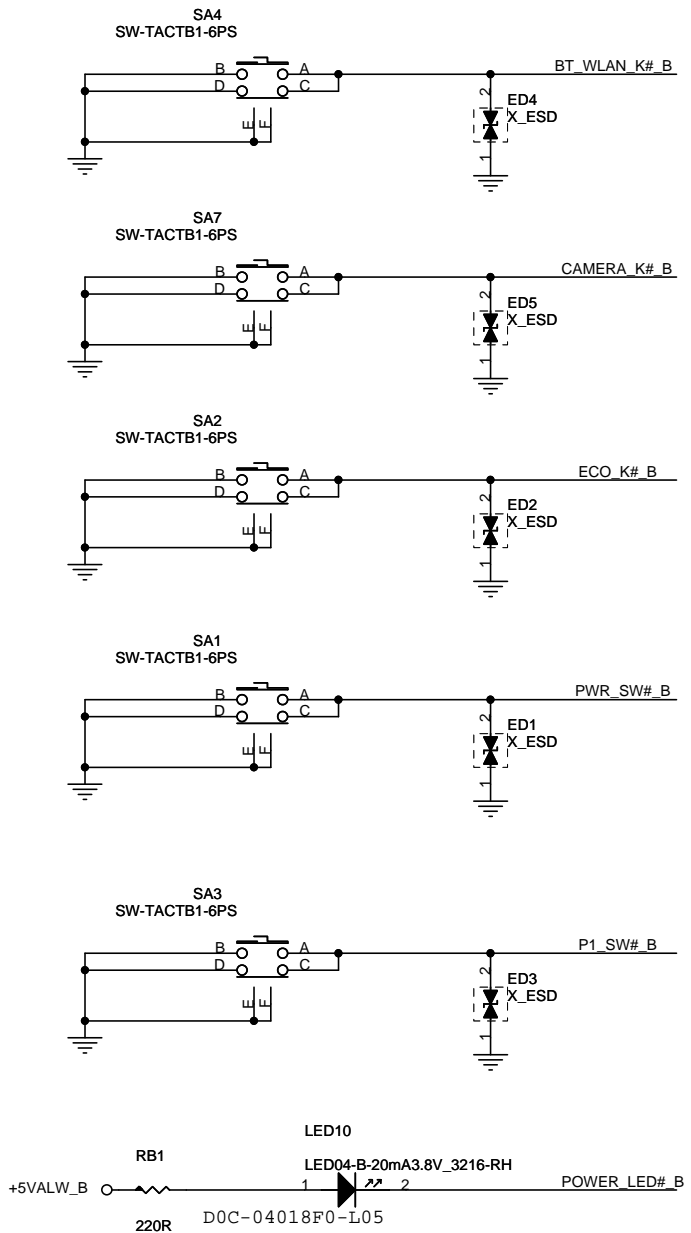
**Power on Sequence required:**

- SB800:**
- 1, +3.3VDUAL ramp before +1.1VDUAL
  - 2, +3.3V ramp before +1.8v
  - 3, +1.8V ramp before +1.1v
  - 4, +3.3v ramp before +1.1v
  - 5, +3.3VALW\_R ramping down time > 300us
  - 6, 50uS <= All power rails except +3.3VALW\_R <= 40mS
  - 7, 100uS <= +3.3VALW\_R <= 40mS
- RS880:**
- 1,  $0 < (+3.3V) - (+1.8v) < 2.1$
  - 2, +1.8V ramp before +1.1v
  - 3, +1.1V ramp before VCC\_NB





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