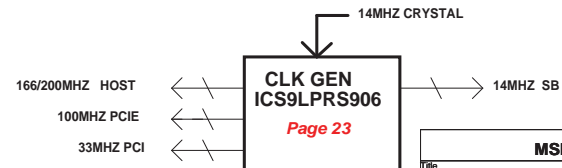
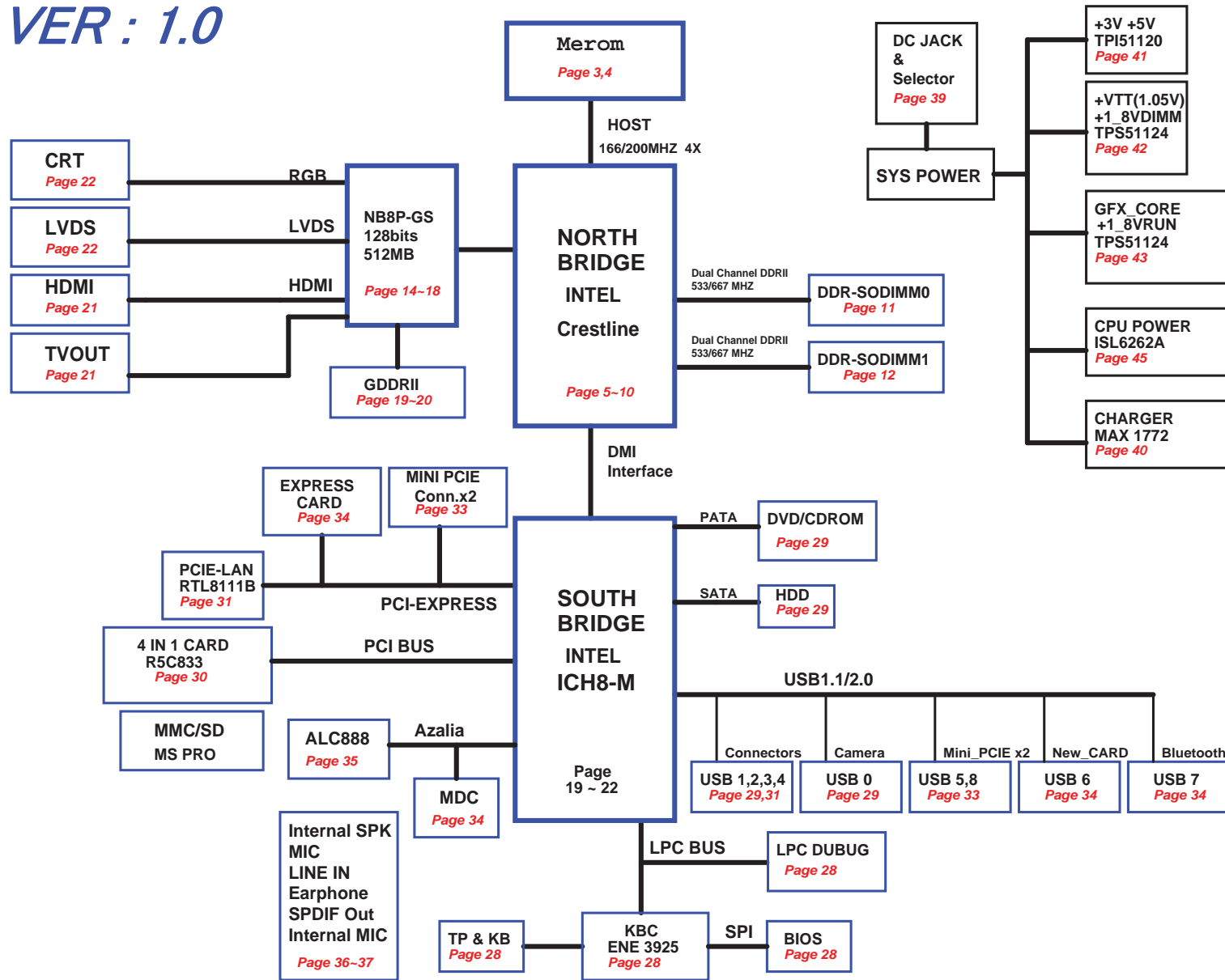


# MS-163A VER : 1.0

- 01 : BLOCK DIAGRAM
- 02 : PLATFORM
- 03 : Merom-1 (HOST BUS)
- 04 : Merom-2 (POWER/GND)
- 05 : CRESTLINE-1 (HOST BUS)
- 06 : CRESTLINE-2 (DMI/VGA)
- 07 : CRESTLINE-3 (DDR)
- 08 : CRESTLINE-4 (POWER-1)
- 09 : CRESTLINE-5 (POWER-2)
- 10 : CRESTLINE-6 (VSS)
- 11 : DDR2\_SODIMM0
- 12 : DDR2\_SODIMM1
- 13 : DDR2 Termination
- 14 : NB8P-1 (Host Interface)
- 15 : NB8P-2 (IO Interface)
- 16 : NB8P-3 (MEM Interface)
- 17 : NB8P-4 (STRAP)
- 18 : NB8P-5 (POWER/GND)
- 19 : GDDRII\_32Mx16\_BGA\_A
- 20 : GDDRII\_32Mx16\_BGA\_B
- 21 : [VIDEO] HDMI & TVOUT
- 22 : [VIDEO] CRT & LVDS & BL
- 23 : CLK GEN [ICS9LPRS514]
- 24 : ICH8M-1 (CPU/IDE/Azalia)
- 25 : ICH8M-2 (PCI/USB/PCIE/DMI)
- 26 : ICH8M-3 (SM BUS/GPIO)
- 27 : ICH8M-4 (POWER/GND)
- 28 : KBC/EC/uP [ENE3925-LFQP144]
- 29 : HDD, ODD, CAMERA & USB CONN
- 30 : CardReader (Ricoh-R5C833)
- 31 : PCIE LAN (RTL8111B)
- 32 : ESATA (SIL3531)
- 33 : Mini\_PCIEx2 & FAN
- 34 : NEWCARD & MDC & BT
- 35 : [AUDIO] CODEC ALC888
- 36 : [AUDIO] AMP & JACKS
- 37 : [AUDIO] Array Mic (FM2010)
- 38 : LED & FPC
- 39 : M\_Battery select
- 40 : M\_Battery Charger
- 41 : M\_System Power
- 42 : VTT(NB/SB), 1.8VDIMM, VTERM
- 43 : +G73M\_CORE, 1.8VRUN
- 44 : +1.2VGFX, +1.25VRUN, +1.5VRUN
- 45 : M\_CPU power
- 46 : Screw
- 47 : Manual Part
- 48 : EMI
- 49 : Power Sequence
- 50 : KBC\_CTR\_PWR
- 51 : AC/Battery timing 1
- 52 : AC/Battery timing 2
- 53 : AC/Battery timing 3
- 54 : AC/Battery timing 4



## Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
VHORE	Core Voltage for Processor	VR_ON
+VTT	1.05 rail for Processor & 965PM & ICH8M	PM_SLP_S3# ( RUN_ON )
+1_5VRUN	1.5V LDO power rail(off in S3-S5)	PM_SLP_S3# ( RUN_ON )
+1_25VRUN	1.25V powe rail NB PLL and PXE (off in S3-S5)	+1_5VRUN
+3VRUN	3.3V switched power rail(off in S3-S5)	RUND ( RUN_ON )
+5VRUN	5.0V switched power rail(off in S3-S5)	RUND (RUN_ON )
SMDDR_VTERM	0.9V DDR Termination voltage (off in S4-S5)	PM_SLP_S3# ( RUN_ON )
+1_8VDIMM	1.8V power rail DDR (off in S4-S5)	PM_SLP_S4# ( DIMM_ON )
+3VSUS	3.3V power rail (off in S4-S5)	SUS_ON
+5VSUS	5.0V power rail (off in S4-S5)	SUS_ON
+3VALW	3.3V always on power rail	PWR_SRC
+5VALW	5.0V always on power rail	PWR_SRC
+V5_AUDIO	5.0V Power rail Audio codec(off in S3-S5)	RUND

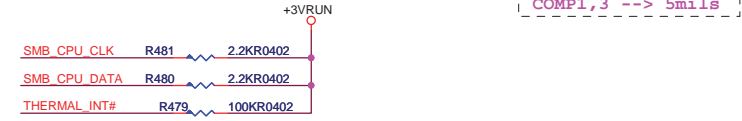
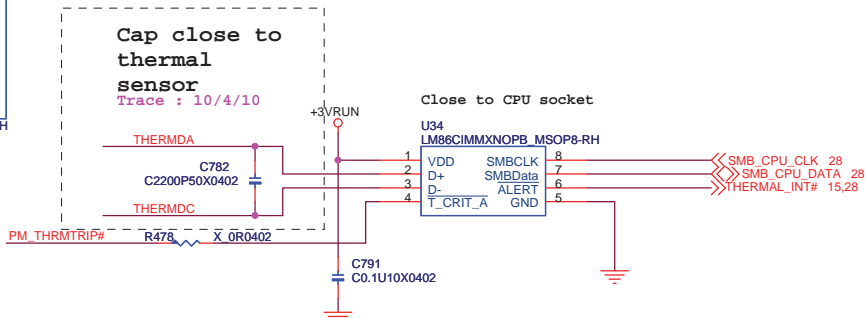
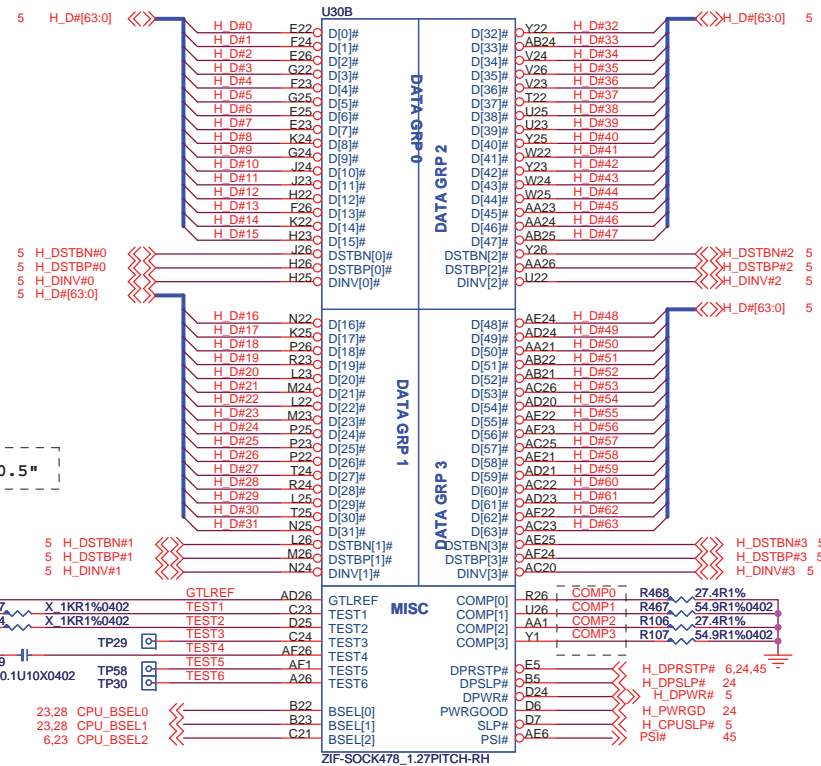
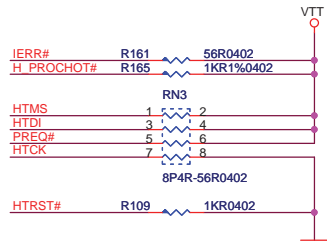
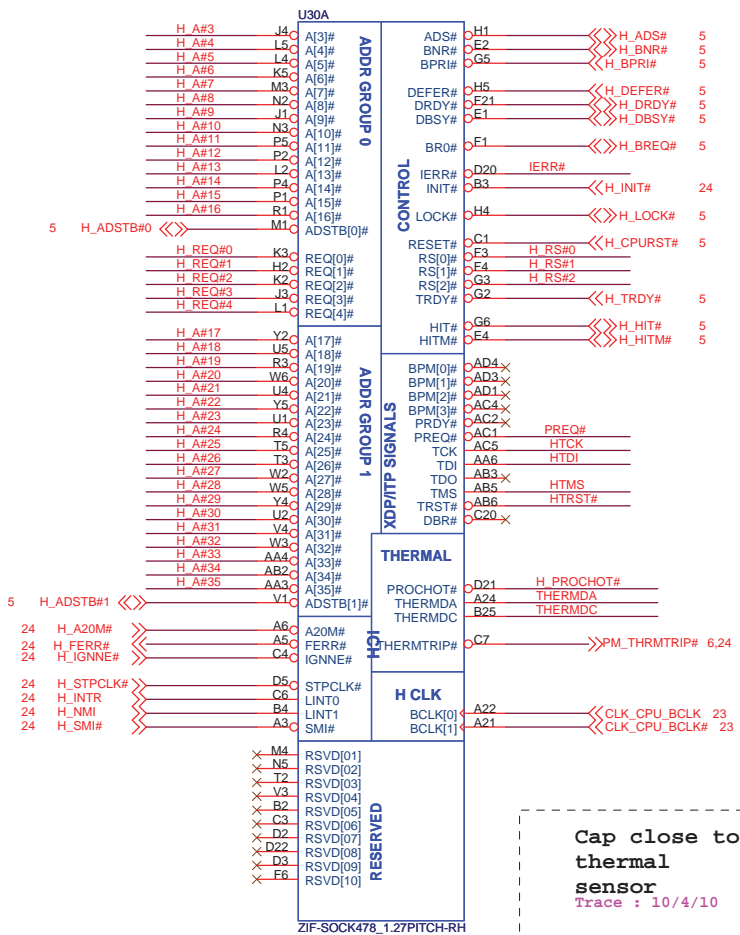
## POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+V*SUS	+V*RUN	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3( Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4( Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on then +V\*SUS will always keep high

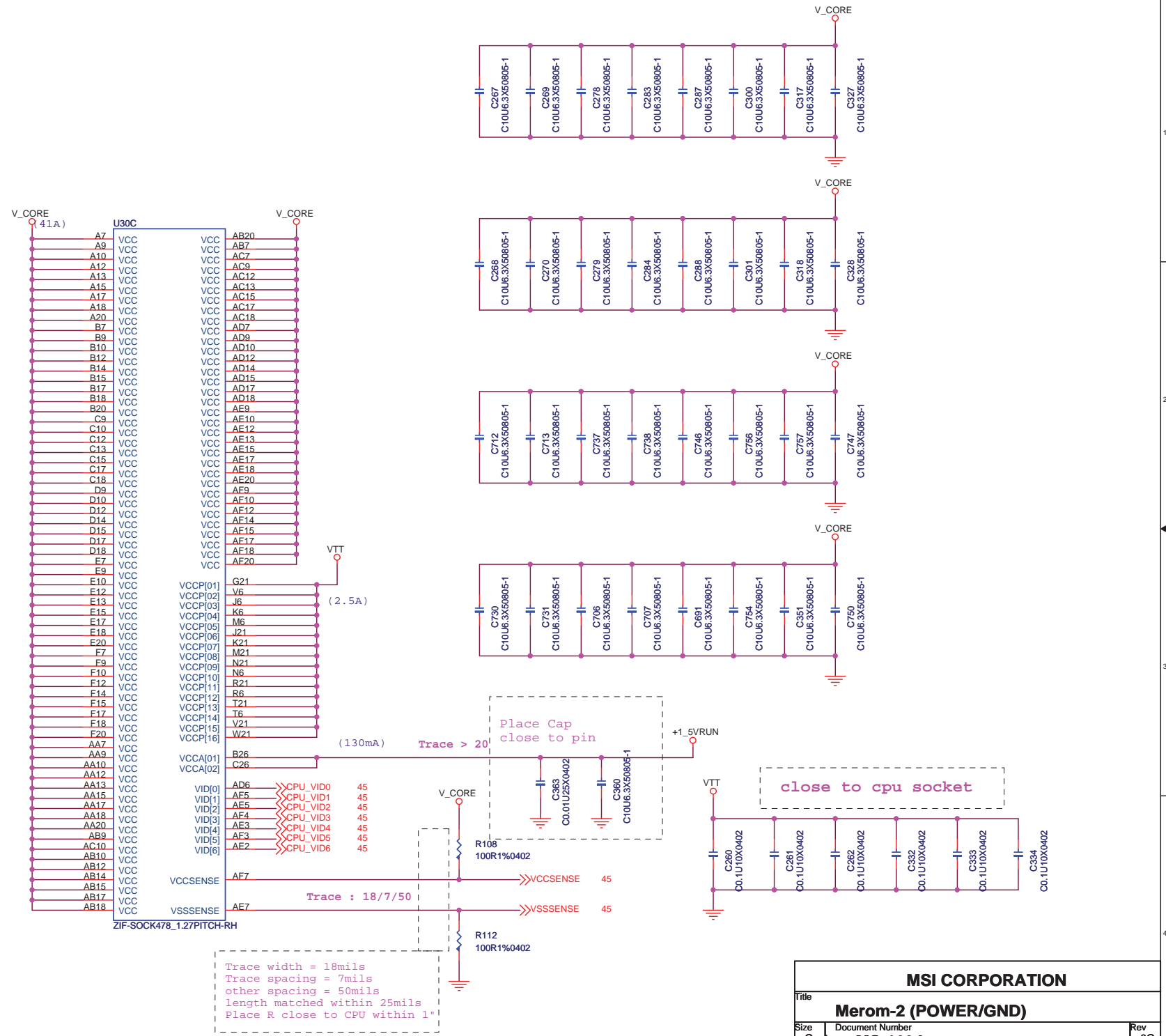
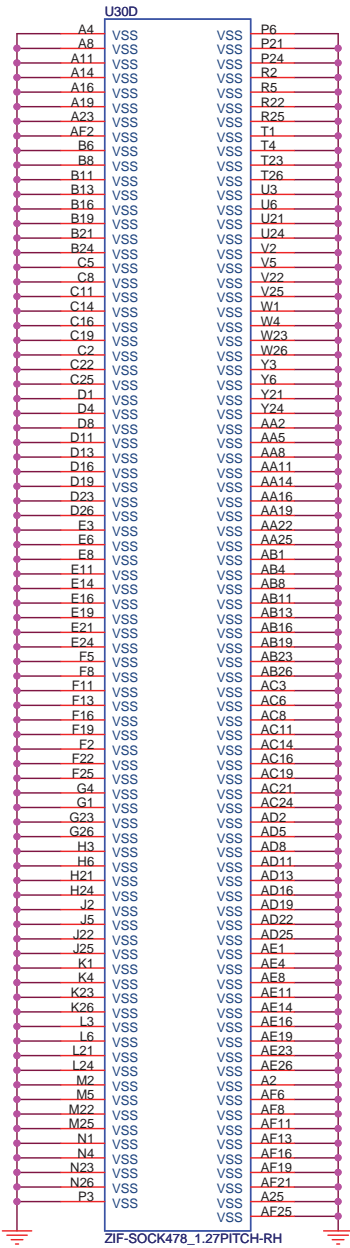
<b>MSI CORPORATION</b>		
Title <b>PLATFORM</b>		
Size Custom	Document Number <b>MS-163A</b>	Rev 0C
Date: Monday, May 07, 2007	Sheet 2 of 54	

5 H\_A#[35:3] <<> H\_A#[35:3]  
 5 H\_RS#[2:0] <> H\_RS#[2:0]  
 5 H\_REQ#[4:0] <<> H\_REQ#[4:0]



Within 0.5"  
 25mils Spacing  
 COMP0,2 --> 18mils  
 COMP1,3 --> 5mils

<b>MSI CORPORATION</b>			
Title <b>Merom-1 (HOST BUS)</b>			
Size	Document Number	Rev	
Custom	<b>MS-163A</b>	OC	
Date:	Thursday, July 05, 2007	Sheet	3 of 54

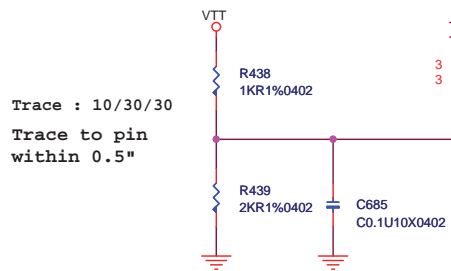
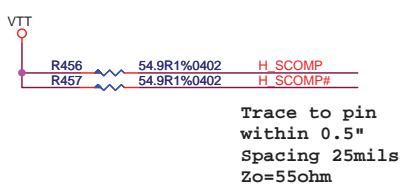
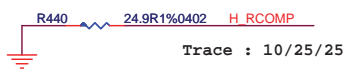
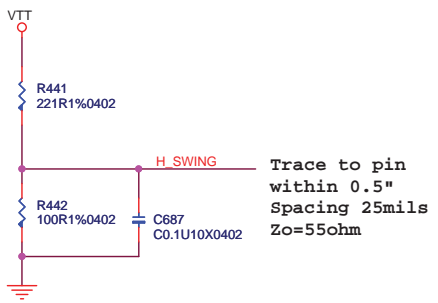


**MSI CORPORATION**

Title: **Merom-2 (POWER/GND)**

Size: Custom    Document Number: **MS-163A**    Rev: 0C

Date: Wednesday, July 04, 2007    Sheet: 4 of 54



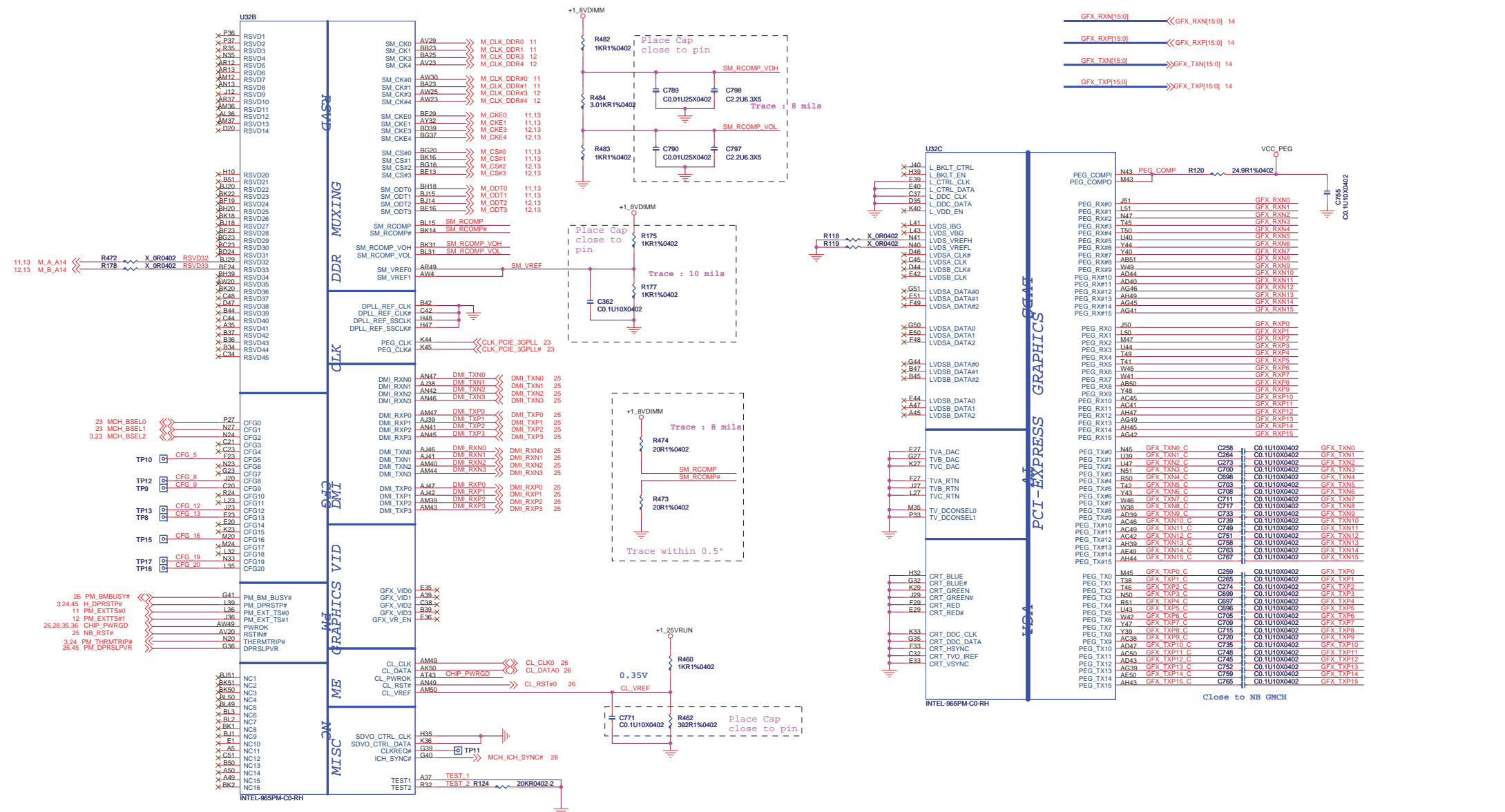
3 H_D#[63:0]	H_D#0	E2	H_D#0
	H_D#1	G2	H_D#1
	H_D#2	G7	H_D#2
	H_D#3	M6	H_D#3
	H_D#4	H7	H_D#4
	H_D#5	H3	H_D#5
	H_D#6	G4	H_D#6
	H_D#7	F3	H_D#7
	H_D#8	N8	H_D#8
	H_D#9	H2	H_D#9
	H_D#10	M10	H_D#10
	H_D#11	N12	H_D#11
	H_D#12	N9	H_D#12
	H_D#13	H5	H_D#13
	H_D#14	P13	H_D#14
	H_D#15	K9	H_D#15
	H_D#16	M2	H_D#16
	H_D#17	W10	H_D#17
	H_D#18	Y8	H_D#18
	H_D#19	V4	H_D#19
	H_D#20	M3	H_D#20
	H_D#21	J1	H_D#21
	H_D#22	N5	H_D#22
	H_D#23	N3	H_D#23
	H_D#24	W6	H_D#24
	H_D#25	W9	H_D#25
	H_D#26	N2	H_D#26
	H_D#27	Y7	H_D#27
	H_D#28	Y9	H_D#28
	H_D#29	P4	H_D#29
	H_D#30	W3	H_D#30
	H_D#31	N1	H_D#31
	H_D#32	AD12	H_D#32
	H_D#33	AE3	H_D#33
	H_D#34	AD9	H_D#34
	H_D#35	AC9	H_D#35
	H_D#36	AC7	H_D#36
	H_D#37	AC14	H_D#37
	H_D#38	AC11	H_D#38
	H_D#39	AC11	H_D#39
	H_D#40	AB2	H_D#40
	H_D#41	AD7	H_D#41
	H_D#42	AB1	H_D#42
	H_D#43	Y3	H_D#43
	H_D#44	AC6	H_D#44
	H_D#45	AE2	H_D#45
	H_D#46	AC5	H_D#46
	H_D#47	AG3	H_D#47
	H_D#48	AJ9	H_D#48
	H_D#49	AH8	H_D#49
	H_D#50	AJ14	H_D#50
	H_D#51	AE9	H_D#51
	H_D#52	AE11	H_D#52
	H_D#53	AH12	H_D#53
	H_D#54	AJ5	H_D#54
	H_D#55	AH5	H_D#55
	H_D#56	AJ6	H_D#56
	H_D#57	AE7	H_D#57
	H_D#58	AJ7	H_D#58
	H_D#59	AJ2	H_D#59
	H_D#60	AE5	H_D#60
	H_D#61	AJ3	H_D#61
	H_D#62	AH2	H_D#62
	H_D#63	AH13	H_D#63

U32A	H_SWING	B3	H_SWING
	H_RCOMP	C2	H_RCOMP
	H_SCOMP	W1	H_SCOMP
	H_SCOMP#	W2	H_SCOMP#
	3 H_CPURST#	B6	H_CPURST#
	3 H_CPUSLP#	E5	H_CPUSLP#
	MCHVREF	B9	H_AVREF
		A9	H_DVREF
			INTEL-965PM-C0-RH

HOST

H_A#3	J13	H_A#3	H_A#[35:3]	3
H_A#4	B11	H_A#4		
H_A#5	C11	H_A#5		
H_A#6	M11	H_A#6		
H_A#7	C15	H_A#7		
H_A#8	F16	H_A#8		
H_A#9	L13	H_A#9		
H_A#10	G17	H_A#10		
H_A#11	C14	H_A#11		
H_A#12	K16	H_A#12		
H_A#13	B13	H_A#13		
H_A#14	L16	H_A#14		
H_A#15	J17	H_A#15		
H_A#16	B14	H_A#16		
H_A#17	K19	H_A#17		
H_A#18	P15	H_A#18		
H_A#19	R17	H_A#19		
H_A#20	B16	H_A#20		
H_A#21	H20	H_A#21		
H_A#22	L19	H_A#22		
H_A#23	D17	H_A#23		
H_A#24	M17	H_A#24		
H_A#25	N16	H_A#25		
H_A#26	J19	H_A#26		
H_A#27	B18	H_A#27		
H_A#28	E19	H_A#28		
H_A#29	B17	H_A#29		
H_A#30	B15	H_A#30		
H_A#31	E17	H_A#31		
H_A#32	C18	H_A#32		
H_A#33	A19	H_A#33		
H_A#34	B19	H_A#34		
H_A#35	N19	H_A#35		
H_ADS#	G12	H_ADS#	H_ADS#	3
H_ADSTB#0	H17	H_ADSTB#0	H_ADSTB#0	3
H_ADSTB#1	G20	H_ADSTB#1	H_ADSTB#1	3
H_BNR#	C8	H_BNR#	H_BNR#	3
H_BPRI#	E8	H_BPRI#	H_BPRI#	3
H_BREQ#	F12	H_BREQ#	H_BREQ#	3
H_DEFER#	D6	H_DEFER#	H_DEFER#	3
H_DBSY#	C10	H_DBSY#	H_DBSY#	3
HPLL_CLK	AM5	CLK_MCH_BCLK	CLK_MCH_BCLK#	23
H_DPWR#	AM7	H_DPWR#	H_DPWR#	3
H_DRDY#	H8	H_DRDY#	H_DRDY#	3
H_HIT#	K7	H_HIT#	H_HIT#	3
H_HITM#	E4	H_HITM#	H_HITM#	3
H_LOCK#	C6	H_LOCK#	H_LOCK#	3
H_TRDY#	G10	H_TRDY#	H_TRDY#	3
H_DIN#0	K5	H_DIN#0	H_DIN#0	3
H_DIN#1	L2	H_DIN#1	H_DIN#1	3
H_DIN#2	AD13	H_DIN#2	H_DIN#2	3
H_DIN#3	AE13	H_DIN#3	H_DIN#3	3
H_DSTBN#0	M7	H_DSTBN#0	H_DSTBN#0	3
H_DSTBN#1	K3	H_DSTBN#1	H_DSTBN#1	3
H_DSTBN#2	AD2	H_DSTBN#2	H_DSTBN#2	3
H_DSTBN#3	AH11	H_DSTBN#3	H_DSTBN#3	3
H_DSTBP#0	L7	H_DSTBP#0	H_DSTBP#0	3
H_DSTBP#1	K2	H_DSTBP#1	H_DSTBP#1	3
H_DSTBP#2	AC2	H_DSTBP#2	H_DSTBP#2	3
H_DSTBP#3	AJ10	H_DSTBP#3	H_DSTBP#3	3
H_REQ#0	M14	H_REQ#0	H_REQ#[4:0]	3
H_REQ#1	E13	H_REQ#1		
H_REQ#2	A11	H_REQ#2		
H_REQ#3	H13	H_REQ#3		
H_REQ#4	B12	H_REQ#4		
H_RS#0	E12	H_RS#0	H_RS#[2:0]	3
H_RS#1	D7	H_RS#1		
H_RS#2	D8	H_RS#2		

<b>MSI CORPORATION</b>		
<b>CRESTLINE-1 (HOST BUS)</b>		
Title		
Size	Document Number	Rev
B	<b>MS-163A</b>	OC
Date:	Wednesday, July 04, 2007	Sheet 5 of 54



Strapping Configuration

CFG5 (Default=High)	CFG9 (Default=High)	CFG16 (Default=High)	CFG19 (Default=Low)	CFG20 (Default=Low)
0= DMI x2 1= DMI x4 (default)	0= Reverse Lanes 1= Normal (default) PCIE X16	0=Dynamic ODT Disabled 1=Dynamic ODT Enabled (default)	0= Normal (default) 1= Lanes Reversed DMI	Only SDVO or PCIE is operational

**MSI CORPORATION**

File: **CRESTLINE-2 (DMI/VGA)**

Size: Document Number  
 Custom **MS-163A** Rev: **0C**

Date: Wednesday, July 11, 2007 Sheet: 6 of 54



11 M\_A\_DQ[63:0]

12 M\_B\_DQ[63:0]

M A DQ0	AR43	SA_DQ0
M A DQ1	AW44	SA_DQ1
M A DQ2	BA45	SA_DQ2
M A DQ3	AY46	SA_DQ3
M A DQ4	AR41	SA_DQ4
M A DQ5	AR45	SA_DQ5
M A DQ6	AT42	SA_DQ6
M A DQ7	AW47	SA_DQ7
M A DQ8	BB45	SA_DQ8
M A DQ9	BF48	SA_DQ9
M A DQ10	BG47	SA_DQ10
M A DQ11	BJ45	SA_DQ11
M A DQ12	BB47	SA_DQ12
M A DQ13	BG50	SA_DQ13
M A DQ14	BH49	SA_DQ14
M A DQ15	BE45	SA_DQ15
M A DQ16	AW43	SA_DQ16
M A DQ17	BE44	SA_DQ17
M A DQ18	BG42	SA_DQ18
M A DQ19	BE40	SA_DQ19
M A DQ20	BF44	SA_DQ20
M A DQ21	BG47	SA_DQ21
M A DQ22	BF40	SA_DQ22
M A DQ23	BF40	SA_DQ23
M A DQ24	AR40	SA_DQ24
M A DQ25	AW40	SA_DQ25
M A DQ26	AT39	SA_DQ26
M A DQ27	AW36	SA_DQ27
M A DQ28	AW41	SA_DQ28
M A DQ29	AY41	SA_DQ29
M A DQ30	AV38	SA_DQ30
M A DQ31	AT38	SA_DQ31
M A DQ32	AV13	SA_DQ32
M A DQ33	AT13	SA_DQ33
M A DQ34	AW11	SA_DQ34
M A DQ35	AV11	SA_DQ35
M A DQ36	AU15	SA_DQ36
M A DQ37	AT11	SA_DQ37
M A DQ38	BA13	SA_DQ38
M A DQ39	BA11	SA_DQ39
M A DQ40	BE10	SA_DQ40
M A DQ41	BD10	SA_DQ41
M A DQ42	BD8	SA_DQ42
M A DQ43	AY9	SA_DQ43
M A DQ44	BG10	SA_DQ44
M A DQ45	AW9	SA_DQ45
M A DQ46	BD7	SA_DQ46
M A DQ47	BB9	SA_DQ47
M A DQ48	BB5	SA_DQ48
M A DQ49	AY7	SA_DQ49
M A DQ50	AT5	SA_DQ50
M A DQ51	AT7	SA_DQ51
M A DQ52	AY6	SA_DQ52
M A DQ53	BB7	SA_DQ53
M A DQ54	AR5	SA_DQ54
M A DQ55	AR8	SA_DQ55
M A DQ56	AR9	SA_DQ56
M A DQ57	AN3	SA_DQ57
M A DQ58	AM8	SA_DQ58
M A DQ59	AN10	SA_DQ59
M A DQ60	AT9	SA_DQ60
M A DQ61	AN9	SA_DQ61
M A DQ62	AN9	SA_DQ62
M A DQ63	AN11	SA_DQ63

INTEL-965PM-C0-RH

DDR SYSTEM MEMORY A

SA_BS0	BB19	M A BS0	11,13
SA_BS1	BK19	M A BS1	11,13
SA_BS2	BF29	M A BS2	11,13
SA_CAS#	BL17	M A CAS#	11,13
SA_DM0	AT45	M A DM0	M A_DM[7:0] 11
SA_DM1	BD44	M A DM1	
SA_DM2	BD42	M A DM2	
SA_DM3	AW38	M A DM3	
SA_DM4	AW13	M A DM4	
SA_DM5	BG8	M A DM5	
SA_DM6	AY5	M A DM6	
SA_DM7	AN6	M A DM7	
SA_DQS0	AT46	M A DQS0	M A_DQS[7:0] 11
SA_DQS1	BE48	M A DQS1	
SA_DQS2	BB43	M A DQS2	
SA_DQS3	BC37	M A DQS3	
SA_DQS4	BB16	M A DQS4	
SA_DQS5	BH6	M A DQS5	
SA_DQS6	BB2	M A DQS6	
SA_DQS7	AP3	M A DQS7	M A_DQS#[7:0] 11
SA_DQS#0	AT47	M A DQS#0	M A_DQS#[7:0] 11
SA_DQS#1	BD47	M A DQS#1	
SA_DQS#2	BC41	M A DQS#2	
SA_DQS#3	BA37	M A DQS#3	
SA_DQS#4	BA16	M A DQS#4	
SA_DQS#5	BH7	M A DQS#5	
SA_DQS#6	BC1	M A DQS#6	
SA_DQS#7	AP2	M A DQS#7	
SA_MA0	BJ19	M A A0	M A_A[13:0] 11,13
SA_MA1	BD20	M A A1	
SA_MA2	BK27	M A A2	
SA_MA3	BJ28	M A A3	
SA_MA4	BL24	M A A4	
SA_MA5	BK28	M A A5	
SA_MA6	BJ27	M A A6	
SA_MA7	BJ25	M A A7	
SA_MA8	BL28	M A A8	
SA_MA9	BA28	M A A9	
SA_MA10	BC19	M A A10	
SA_MA11	BE28	M A A11	
SA_MA12	BG30	M A A12	
SA_MA13	BJ16	M A A13	
SA_RAS#	BE18	M A_RAS#	11,13
SA_RCVEN#	AY20	SA_RCVEN#	TP33
SA_WE#	BA19	M A_WE#	11,13

M B DQ0	AP49	SB_DQ0
M B DQ1	AR51	SB_DQ1
M B DQ2	AW50	SB_DQ2
M B DQ3	AW51	SB_DQ3
M B DQ4	AN51	SB_DQ4
M B DQ5	AN50	SB_DQ5
M B DQ6	AV50	SB_DQ6
M B DQ7	AV49	SB_DQ7
M B DQ8	BA50	SB_DQ8
M B DQ9	BB50	SB_DQ9
M B DQ10	B449	SB_DQ10
M B DQ11	BE50	SB_DQ11
M B DQ12	BA51	SB_DQ12
M B DQ13	AY49	SB_DQ13
M B DQ14	BF50	SB_DQ14
M B DQ15	BF49	SB_DQ15
M B DQ16	BJ50	SB_DQ16
M B DQ17	BJ44	SB_DQ17
M B DQ18	BJ43	SB_DQ18
M B DQ19	BL43	SB_DQ19
M B DQ20	BK47	SB_DQ20
M B DQ21	BK49	SB_DQ21
M B DQ22	BK43	SB_DQ22
M B DQ23	BK42	SB_DQ23
M B DQ24	BL41	SB_DQ24
M B DQ25	BL41	SB_DQ25
M B DQ26	BJ37	SB_DQ26
M B DQ27	BJ36	SB_DQ27
M B DQ28	BK41	SB_DQ28
M B DQ29	BL40	SB_DQ29
M B DQ30	BL35	SB_DQ30
M B DQ31	BK37	SB_DQ31
M B DQ32	BK13	SB_DQ32
M B DQ33	BE11	SB_DQ33
M B DQ34	BK11	SB_DQ34
M B DQ35	BC11	SB_DQ35
M B DQ36	BC13	SB_DQ36
M B DQ37	BE12	SB_DQ37
M B DQ38	BC12	SB_DQ38
M B DQ39	BG12	SB_DQ39
M B DQ40	BL10	SB_DQ40
M B DQ41	BL9	SB_DQ41
M B DQ42	BK5	SB_DQ42
M B DQ43	BL5	SB_DQ43
M B DQ44	BK9	SB_DQ44
M B DQ45	BK10	SB_DQ45
M B DQ46	BJ8	SB_DQ46
M B DQ47	BJ6	SB_DQ47
M B DQ48	BF4	SB_DQ48
M B DQ49	BH5	SB_DQ49
M B DQ50	BG1	SB_DQ50
M B DQ51	BC2	SB_DQ51
M B DQ52	BK3	SB_DQ52
M B DQ53	BE4	SB_DQ53
M B DQ54	BD3	SB_DQ54
M B DQ55	BJ2	SB_DQ55
M B DQ56	BA3	SB_DQ56
M B DQ57	BB3	SB_DQ57
M B DQ58	AR1	SB_DQ58
M B DQ59	AT3	SB_DQ59
M B DQ60	AY2	SB_DQ60
M B DQ61	AY3	SB_DQ61
M B DQ62	AU2	SB_DQ62
M B DQ63	AT2	SB_DQ63

INTEL-965PM-C0-RH

DDR SYSTEM MEMORY B

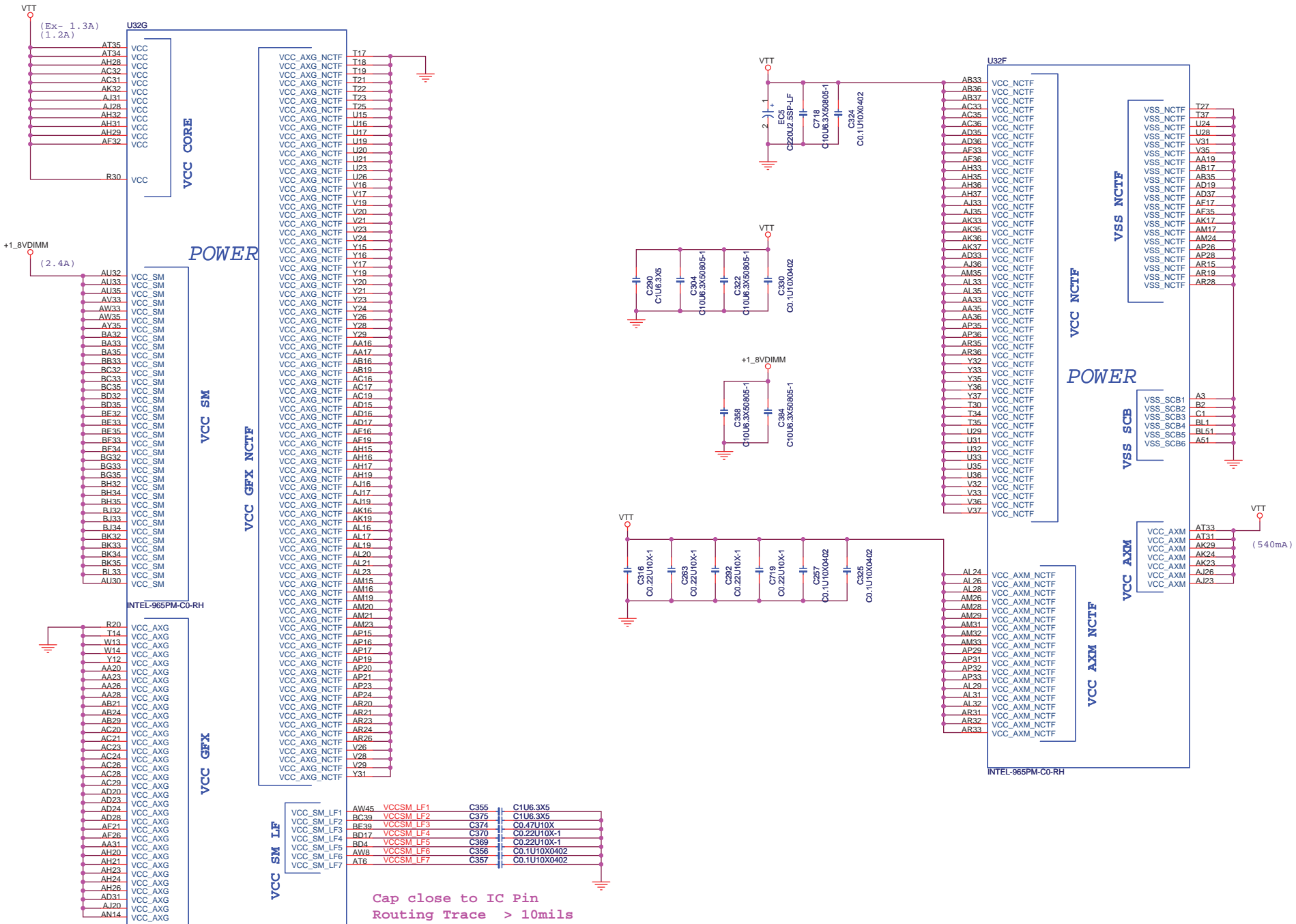
SB_BS0	AY17	M B BS0	12,13
SB_BS1	BG18	M B BS1	12,13
SB_BS2	BG36	M B BS2	12,13
SB_CAS#	BE17	M B CAS#	12,13
SB_DM0	AR50	M B DM0	M B_DM[7:0] 12
SB_DM1	BD49	M B DM1	
SB_DM2	BK45	M B DM2	
SB_DM3	BL39	M B DM3	
SB_DM4	BH12	M B DM4	
SB_DM5	BJ7	M B DM5	
SB_DM6	BF3	M B DM6	
SB_DM7	AW2	M B DM7	
SB_DQS0	AT50	M B DQS0	M B_DQS[7:0] 12
SB_DQS1	BD50	M B DQS1	
SB_DQS2	BK46	M B DQS2	
SB_DQS3	BK39	M B DQS3	
SB_DQS4	BL12	M B DQS4	
SB_DQS5	BE2	M B DQS5	
SB_DQS6	BF2	M B DQS6	
SB_DQS7	AV2	M B DQS7	M B_DQS#[7:0] 12
SB_DQS#0	AU50	M B DQS#0	M B_DQS#[7:0] 12
SB_DQS#1	BC50	M B DQS#1	
SB_DQS#2	BL45	M B DQS#2	
SB_DQS#3	BK38	M B DQS#3	
SB_DQS#4	BK12	M B DQS#4	
SB_DQS#5	BK7	M B DQS#5	
SB_DQS#6	BF2	M B DQS#6	
SB_DQS#7	AV3	M B DQS#7	
SB_MA0	BC18	M B A0	M B_A[13:0] 12,13
SB_MA1	BG28	M B A1	
SB_MA2	BG25	M B A2	
SB_MA3	AW17	M B A3	
SB_MA4	BF25	M B A4	
SB_MA5	BE25	M B A5	
SB_MA6	BA29	M B A6	
SB_MA7	BK28	M B A7	
SB_MA8	AY28	M B A8	
SB_MA9	BD37	M B A9	
SB_MA10	BG17	M B A10	
SB_MA11	BE37	M B A11	
SB_MA12	BA39	M B A12	
SB_MA13	BG13	M B A13	
SB_RAS#	AV16	M B_RAS#	12,13
SB_RCVEN#	AY18	SB_RCVEN#	TP33
SB_WE#	BC17	M B_WE#	12,13

**MSI CORPORATION**

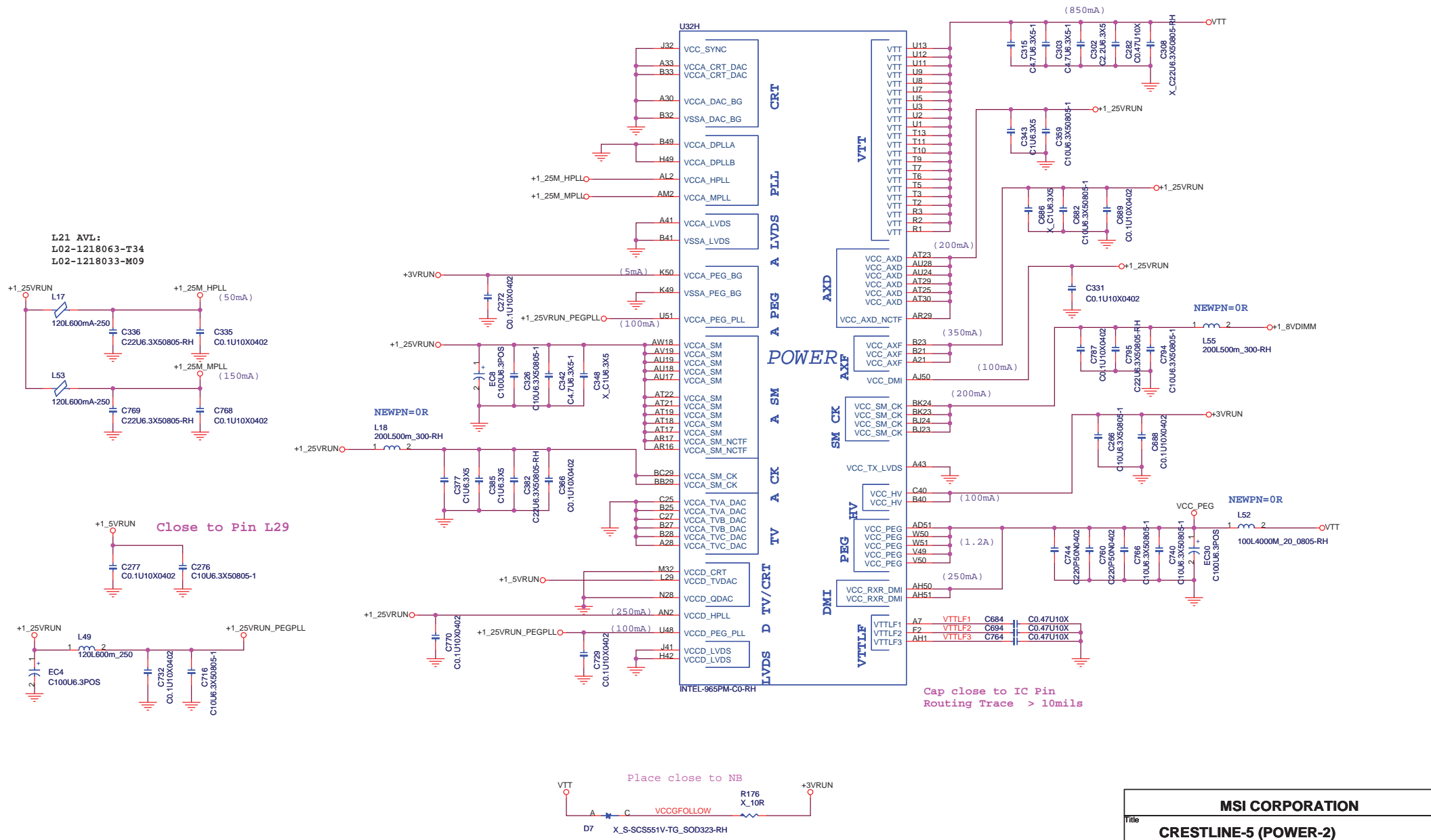
Title: **CRESTLINE-3 (DDR)**

Size	Document Number	Rev
Custom	<b>MS-163A</b>	0C

Date: Wednesday, July 04, 2007 Sheet 7 of 54







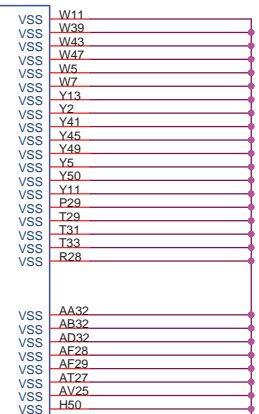
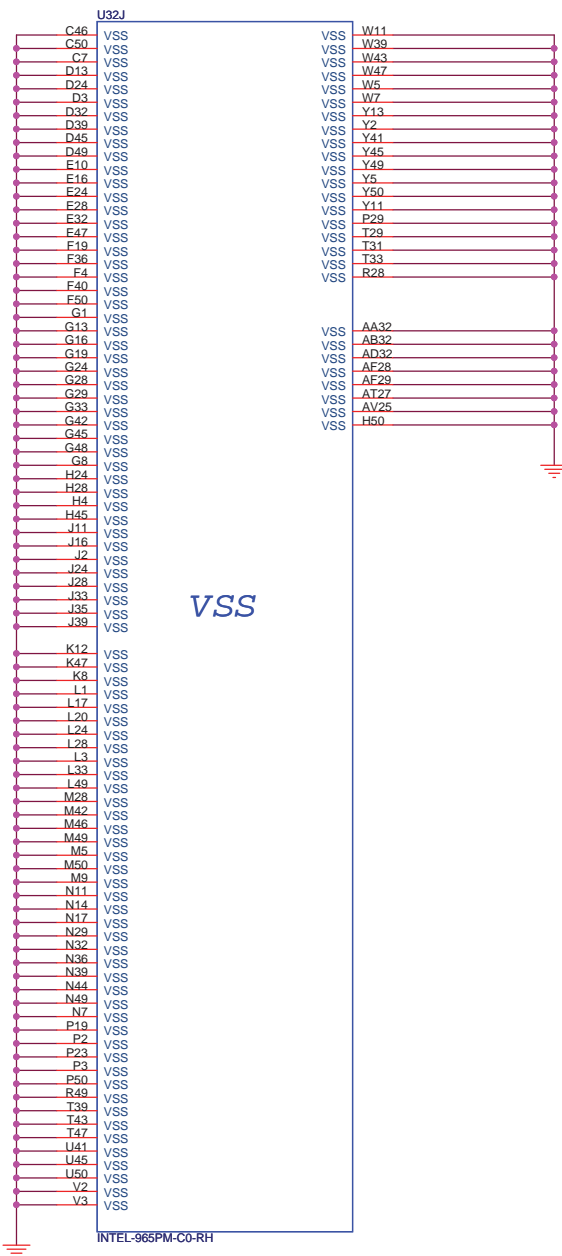
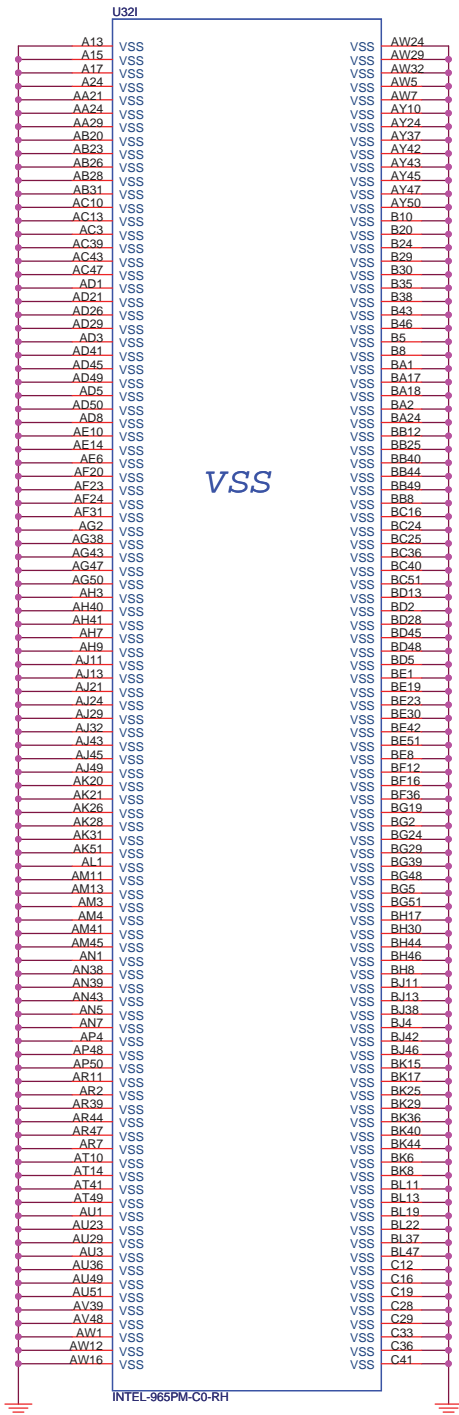
L21 AVL:  
 L02-1218063-T34  
 L02-1218033-M09

Close to Pin L29

Place close to NB

Cap close to IC Pin  
 Routing Trace > 10mils

<b>MSI CORPORATION</b>		
Title		
<b>CRESTLINE-5 (POWER-2)</b>		
Size	Document Number	Rev
Custom	<b>MS-163A</b>	0C
Date:	Tuesday, May 29, 2007	Sheet 9 of 54

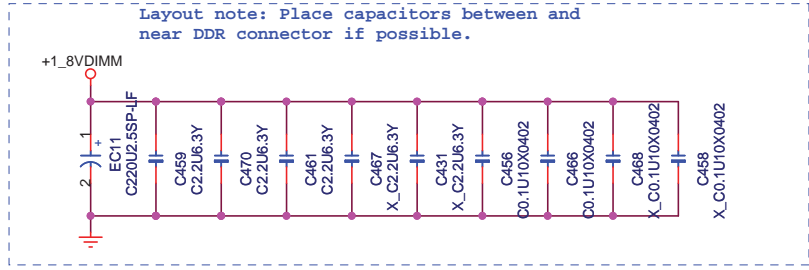
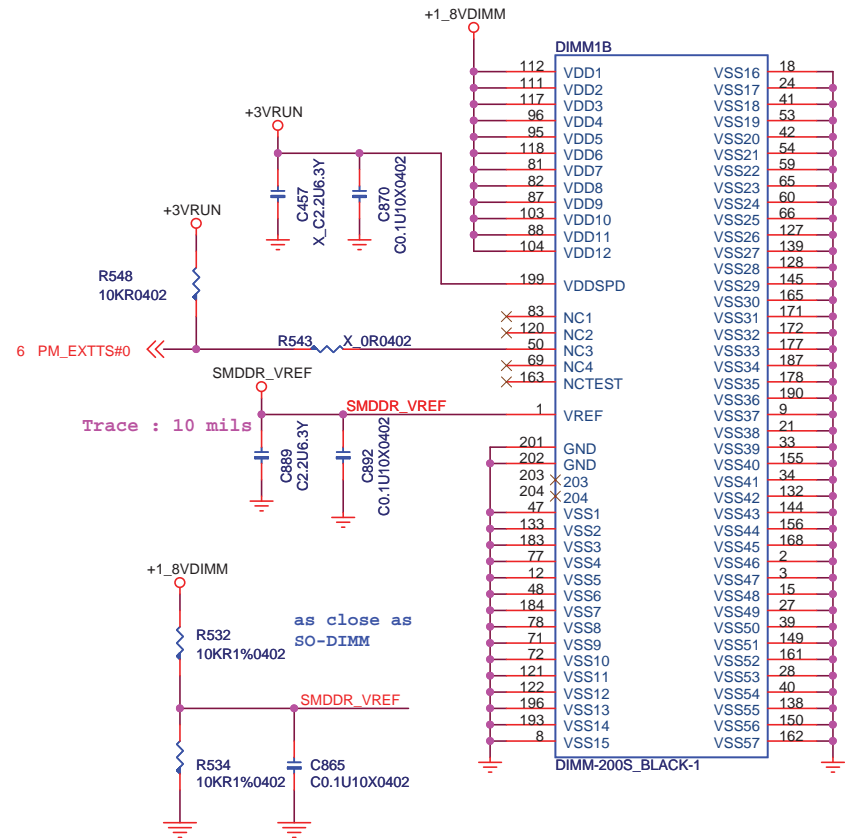
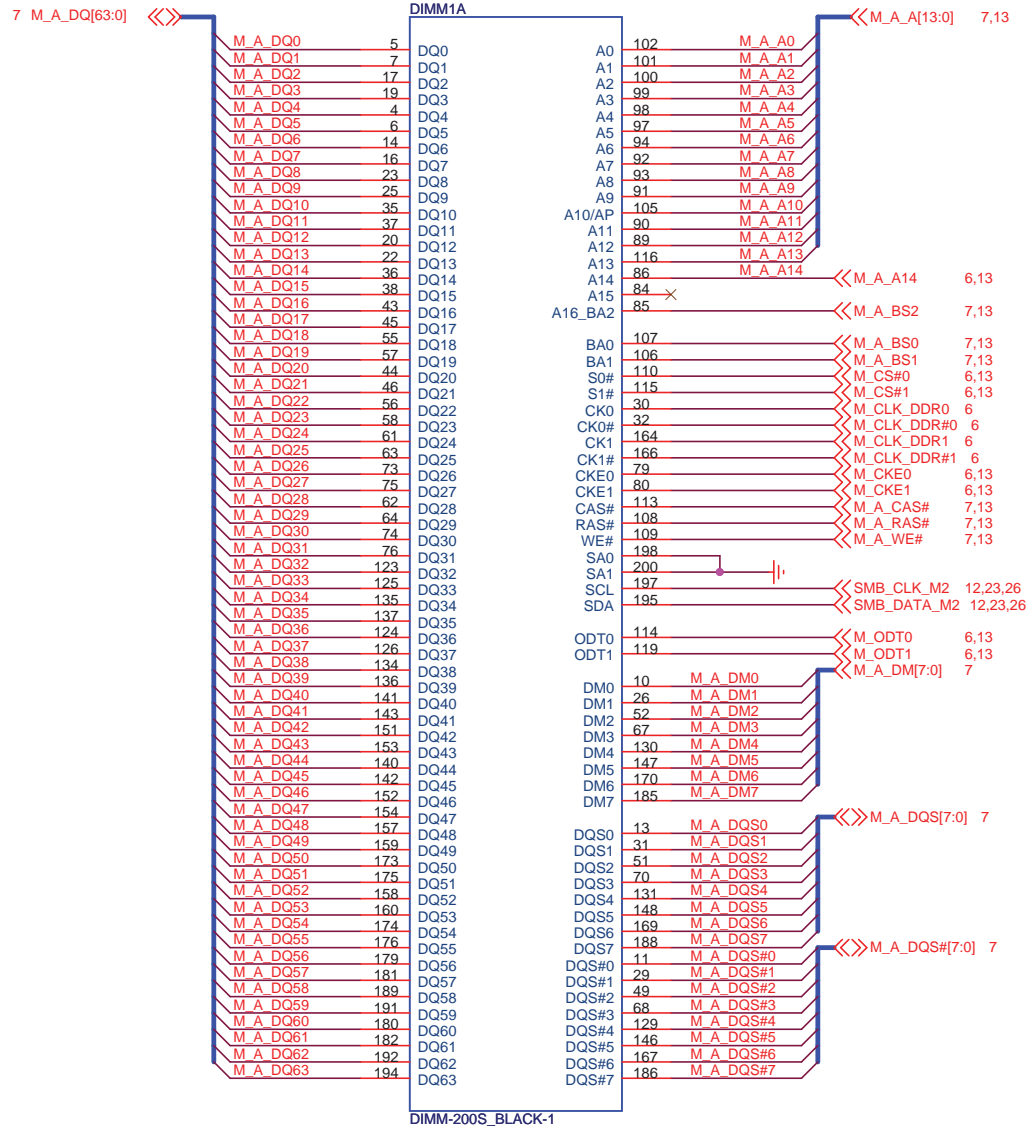


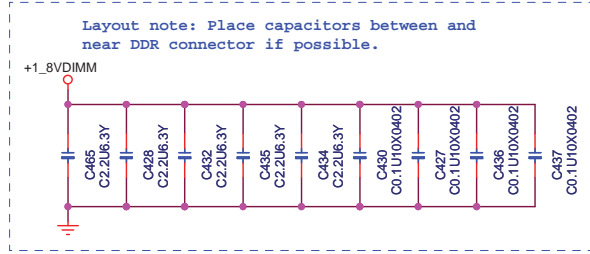
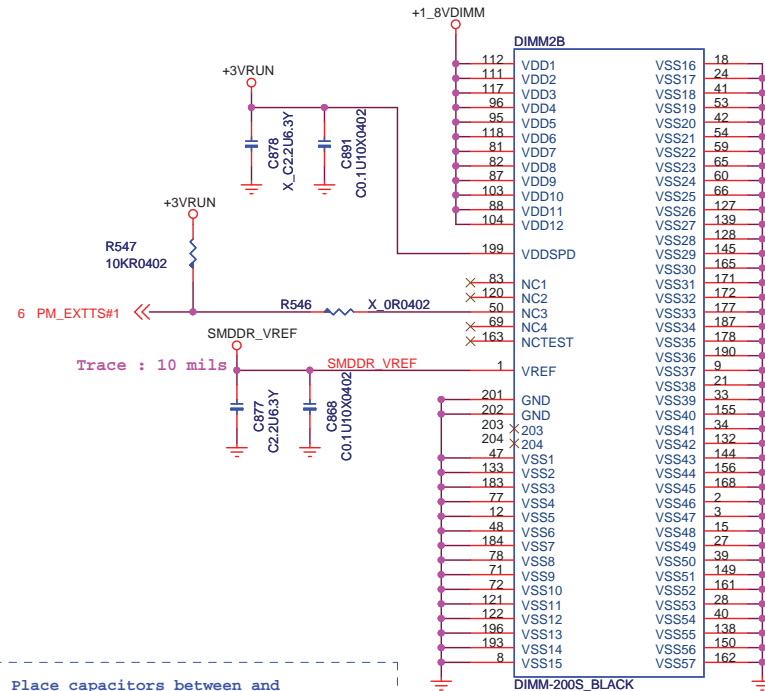
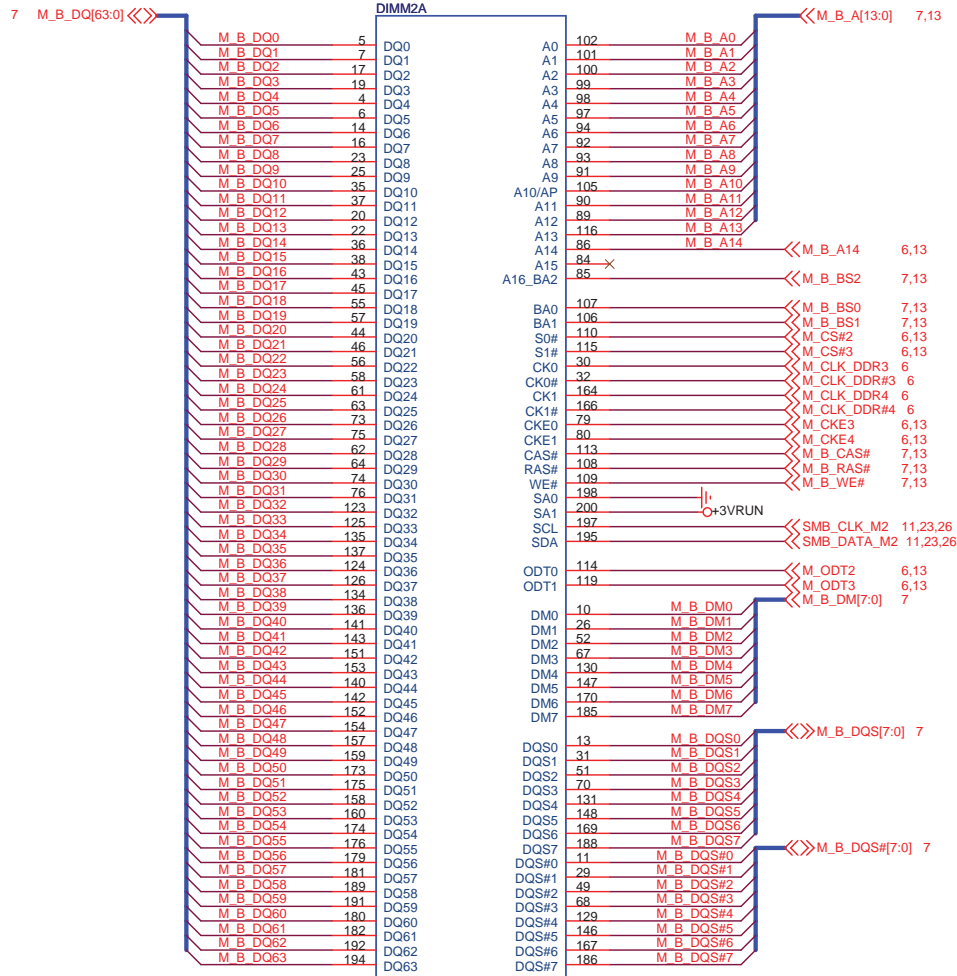
**MSI CORPORATION**

Title: **CRESTLINE-6 (VSS)**

Size	Document Number	Rev
Custom	<b>MS-163A</b>	0C

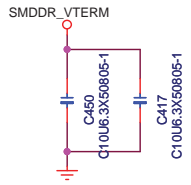
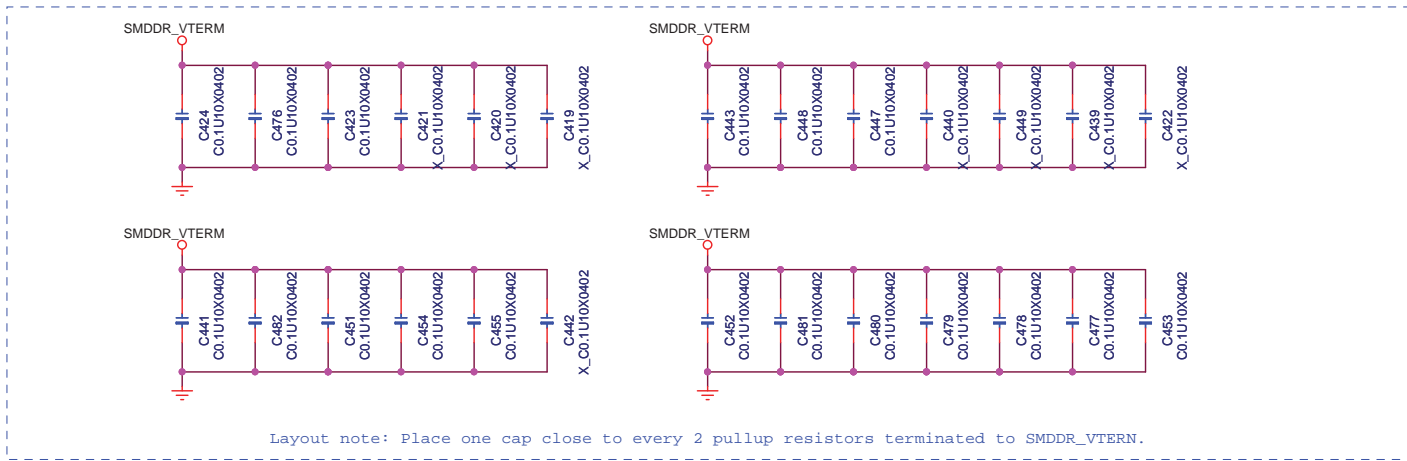
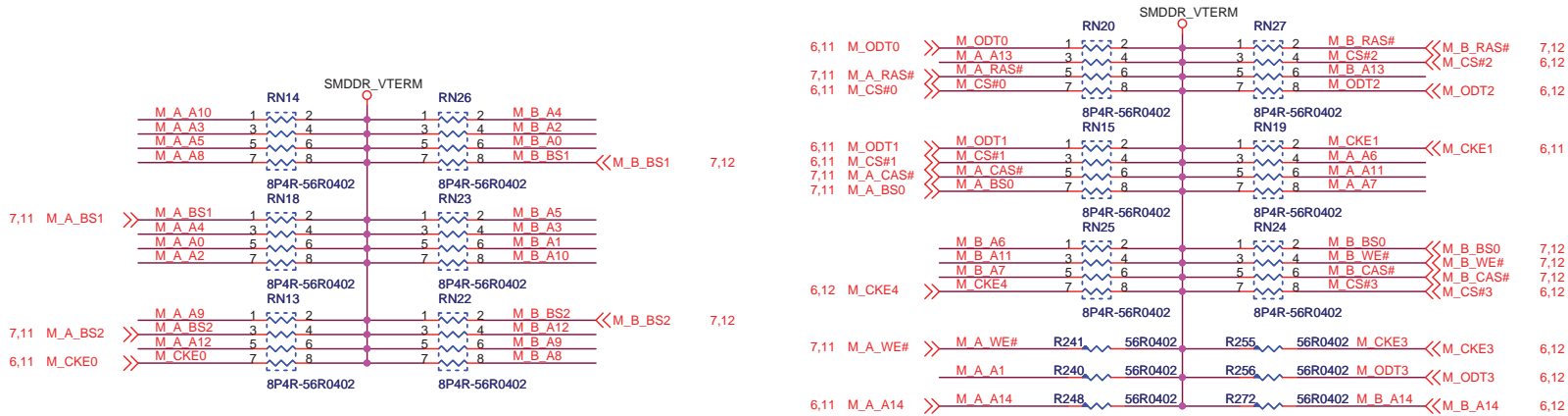
Date: Monday, May 28, 2007 Sheet 10 of 54



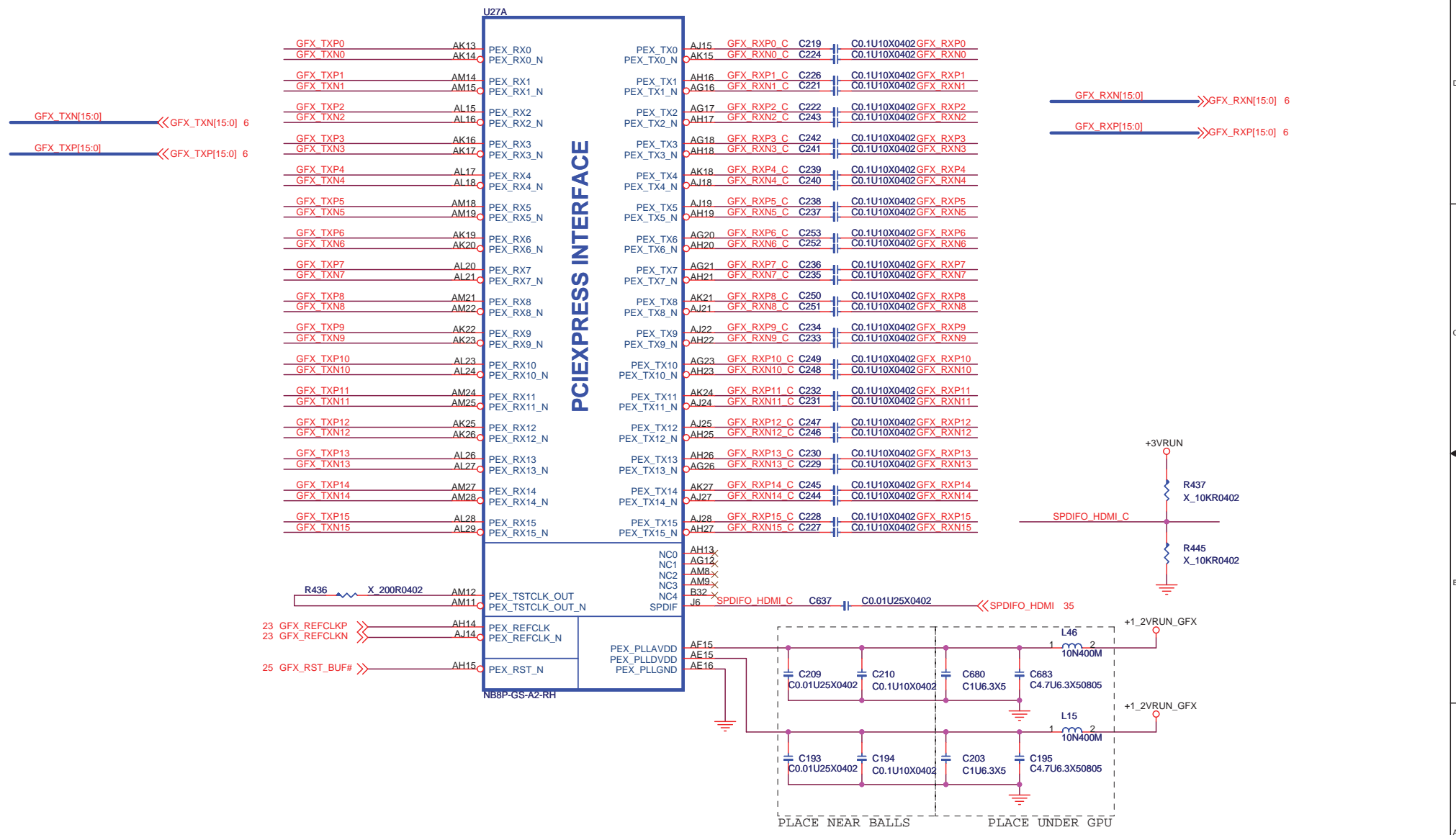


MSI CORPORATION		
Title		
DDR2 SODIMM 1		
Size	Document Number	Rev
Custom	MS-163A	0C
Date:	Tuesday, July 10, 2007	Sheet 12 of 54

M\_A\_A[13:0] << M\_A\_A[13:0] 7,11  
 M\_B\_A[13:0] << M\_B\_A[13:0] 7,12

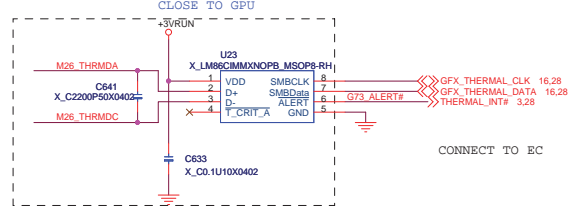
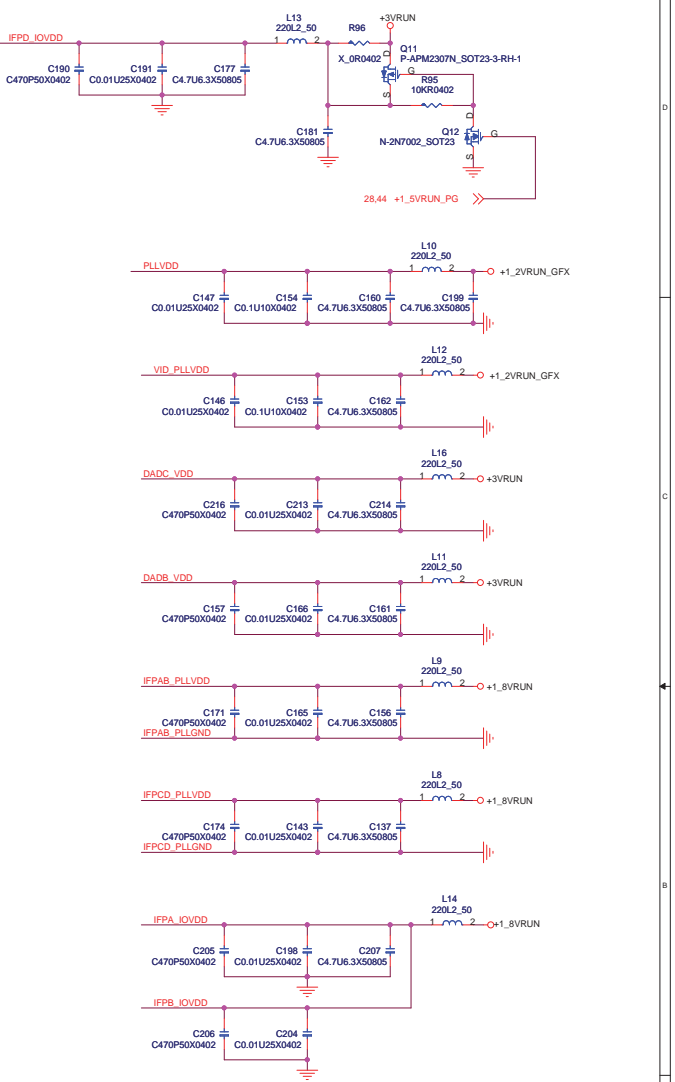
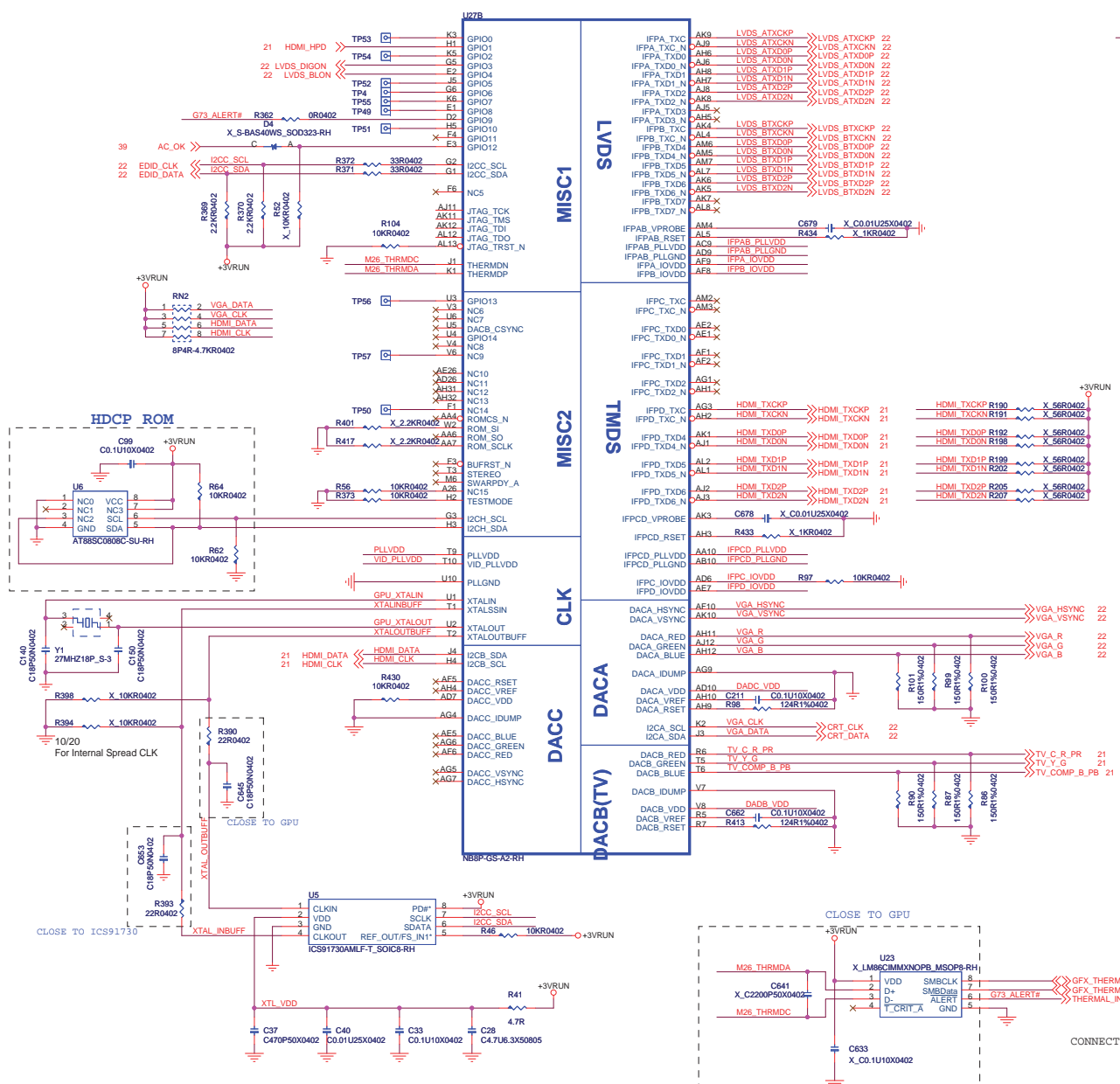


<b>MSI CORPORATION</b>		
Title		
<b>DDR2 TREMINATION</b>		
Size	Document Number	Rev
B	<b>MS-163A</b>	OC
Date:	Wednesday, July 04, 2007	Sheet 13 of 54



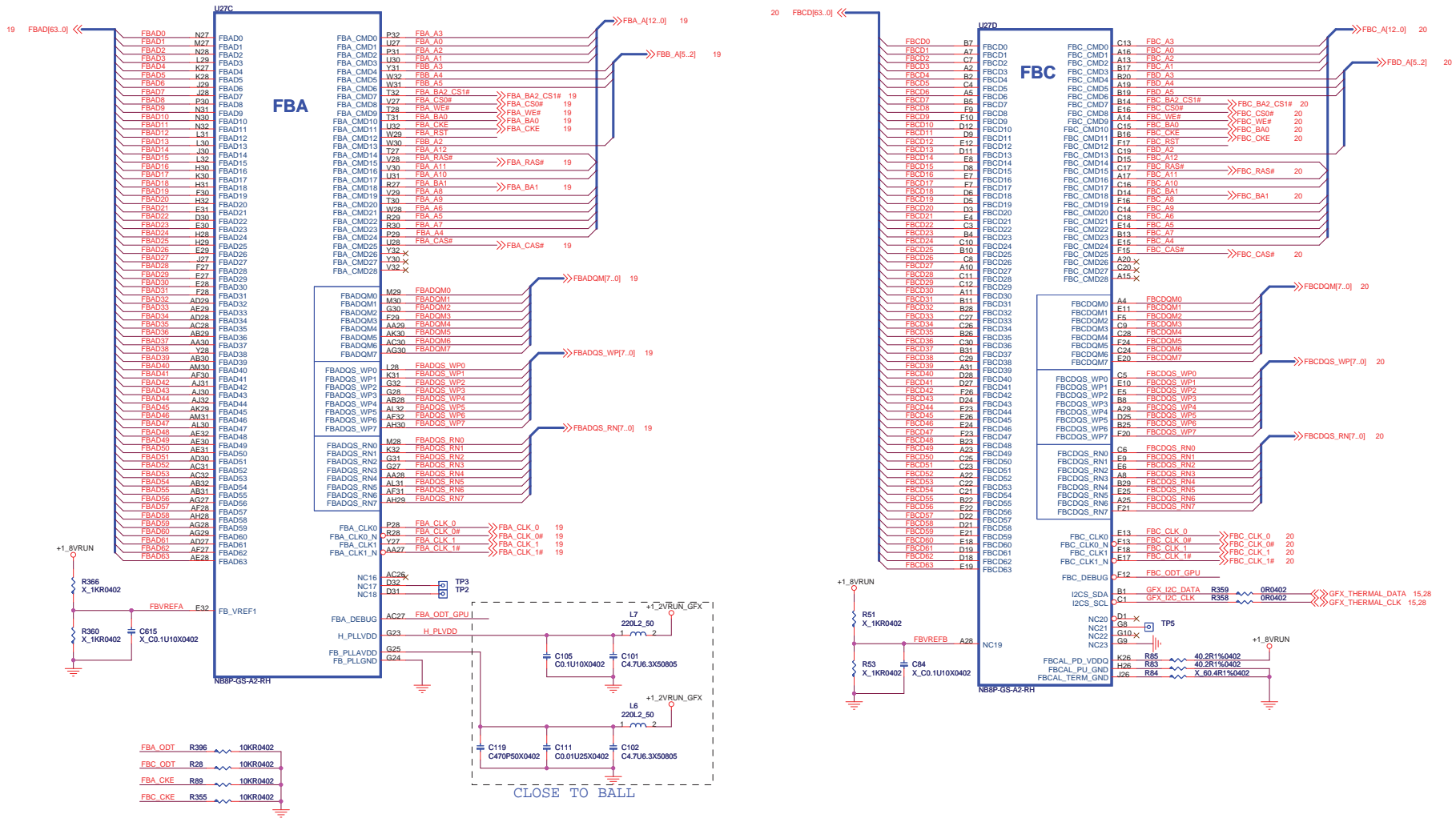
MSI CORPORATION		
Title		
NB8P: Host Interface		
Size	Document Number	Rev
B	MS-163A	OC
Date:	Tuesday, July 10, 2007	Sheet 14 of 54





**MSI CORPORATION**

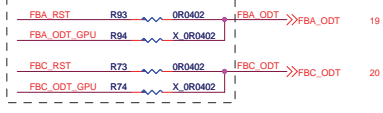
File <b>NB8P: IO Interface</b>		
Size <b>C</b>	Document Number <b>MS-163A</b>	Rev <b>0A</b>
Date: Friday, July 06, 2007	Sheet 15	of 54



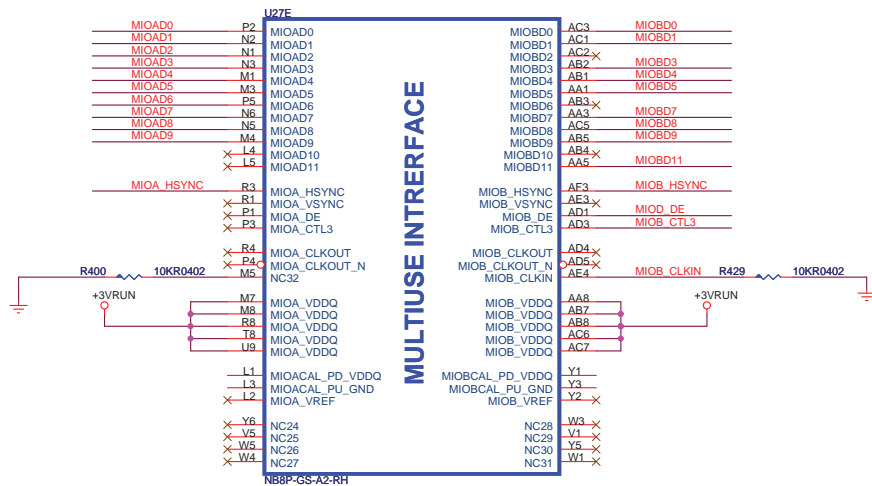
- FBA\_ODT R396 10KR0402
- FBC\_ODT R28 10KR0402
- FBA\_CKE R99 10KR0402
- FBC\_CKE R355 10KR0402

CLOSE TO BALL

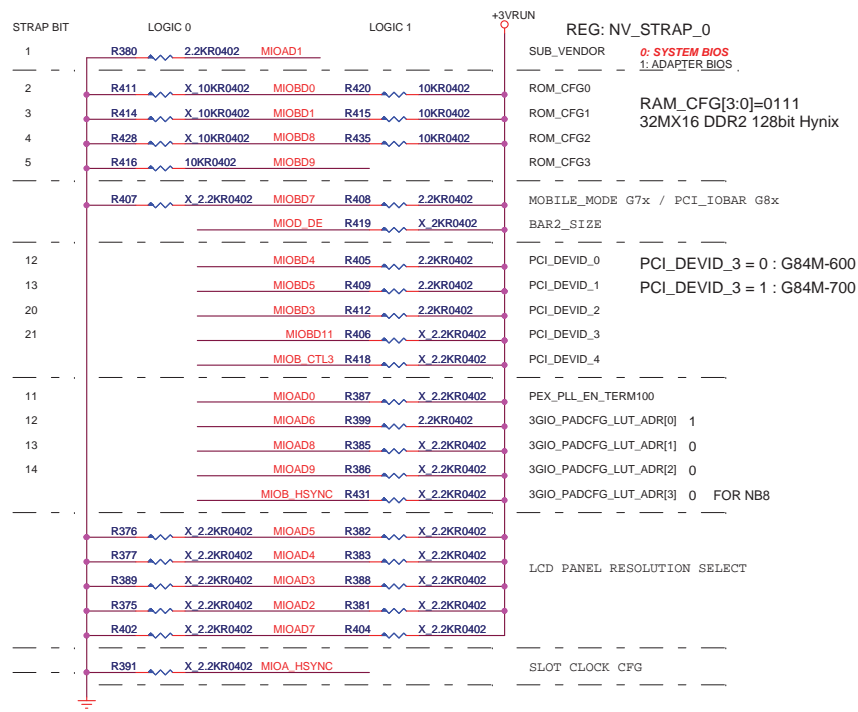
CLOSE TO GPU



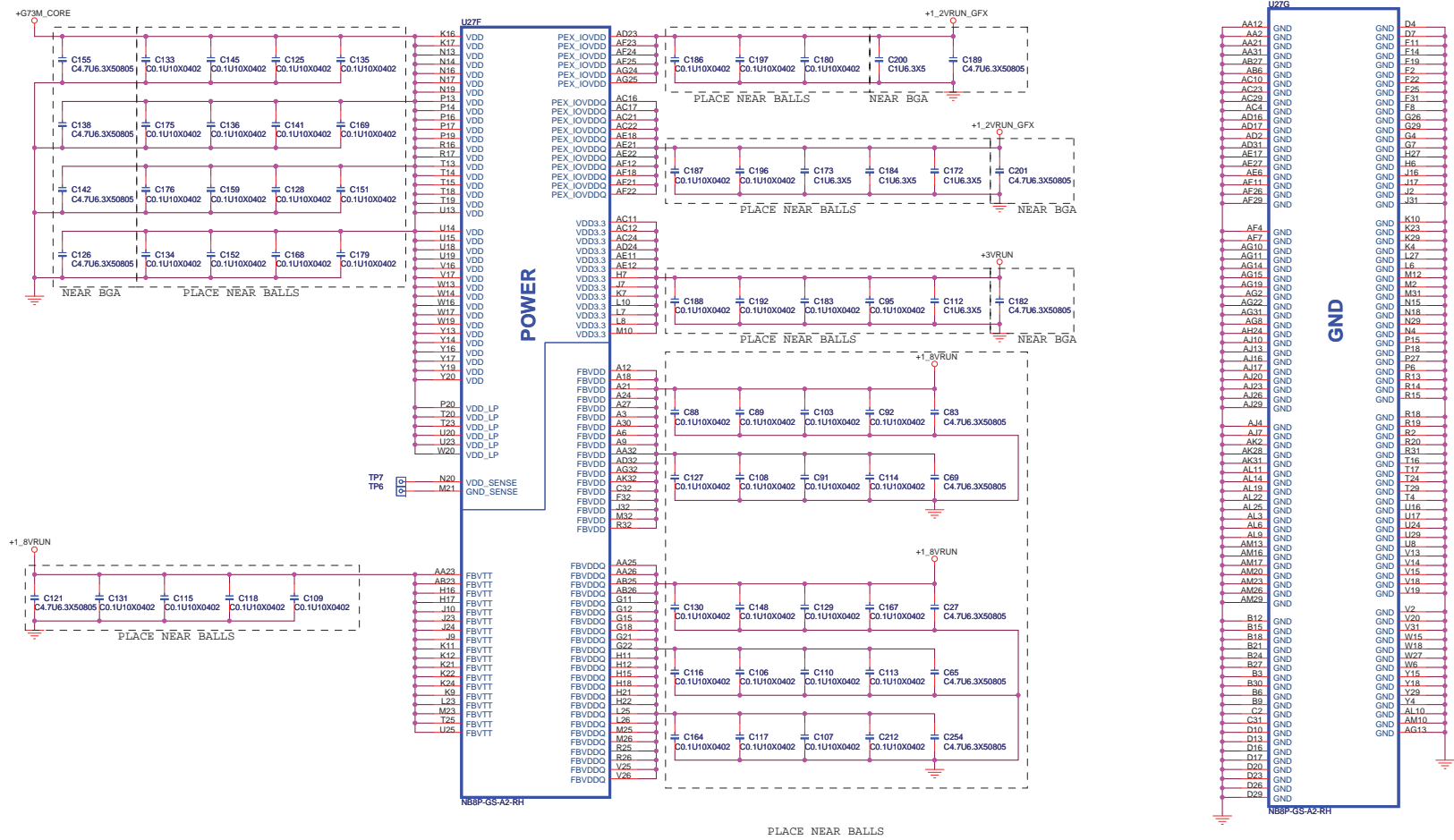
MSI CORPORATION		
File	<b>NB8P: MEM Interface</b>	
Size	Document Number	Rev
C	<b>MS-163A</b>	0C
Date:	Wednesday, July 04, 2007	Sheet 16 of 54



PIN NAME	G8X FUNCTION	DEFAULT	VBIOS ROM NOT PRESENT	NB8
MIOBD2	CRYSTAL	0	NOT REQUIRED	0
MIOAD7	TVMODE0	1	NOT REQUIRED	X
MIOAD10	TVMODE1	0	NOT REQUIRED	0
MIOBD6	TVMODE2	0	NOT REQUIRED	0
MIOBD4	PCI_DEVID_0	0	2K PULL-UP RECOMMENDED	X
MIOBD5	PCI_DEVID_1	0	2K PULL-UP RECOMMENDED	X
MIOBD3	PCI_DEVID_2	0	2K PULL-UP RECOMMENDED	X
MIOBD11	PCI_DEVID_3	0	2K PULL-UP RECOMMENDED	X
MIOB_CTL3	PCI_DEVID_4	0	2K PULL-UP RECOMMENDED	X
MIOAD6	3GIO_PADCFG0	0	2K PULL-UP RECOMMENDED	1
MIOAD8	3GIO_PADCFG1	0	2K PULL-UP RECOMMENDED	0
MIOAD9	3GIO_PADCFG2	0	2K PULL-UP RECOMMENDED	0
MIOB_HSYNC	3GIO_PADCFG3	0	2K PULL-UP RECOMMENDED	0
MIOBD7	PCI_IOPAR	1	NOT REQUIRED	1
MIOB_DE	BAR2_SIZE	0	NOT REQUIRED	0

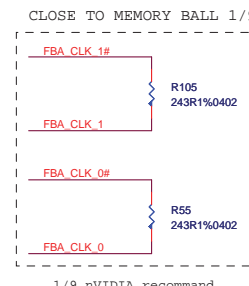
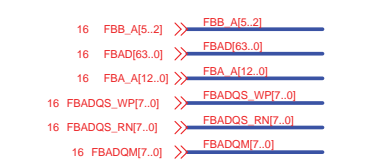
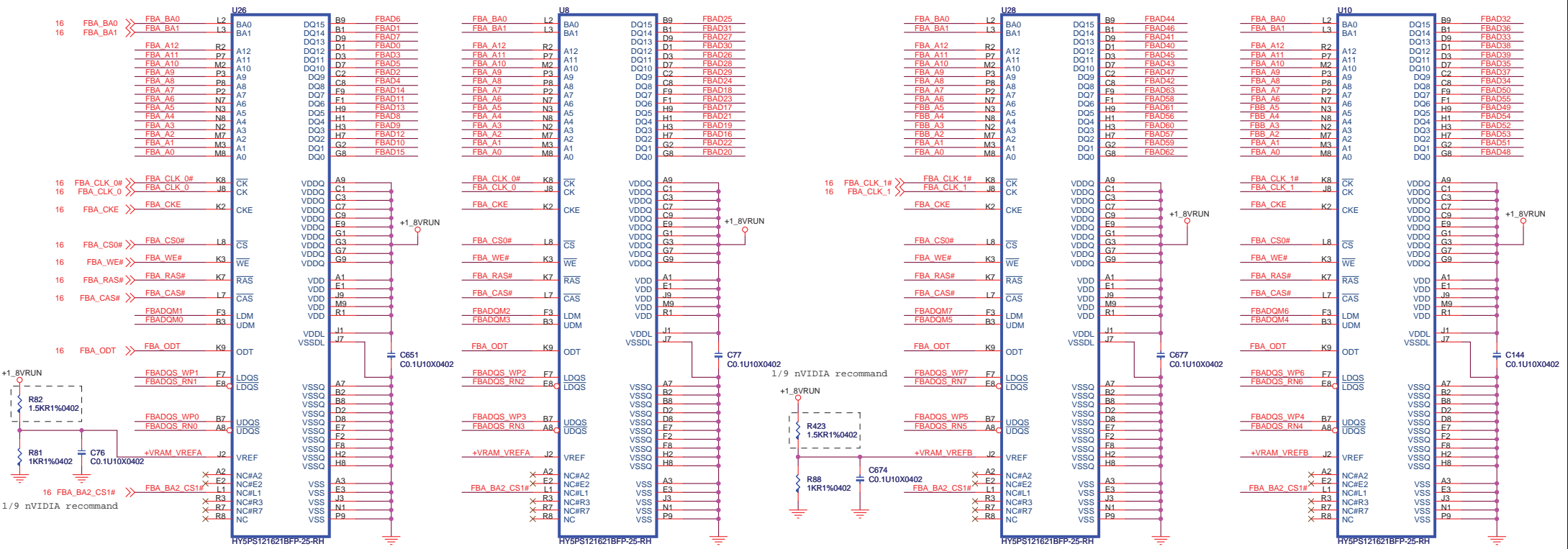


<b>MSI CORPORATION</b>		
Title <b>NB8P: STRAP</b>		
Size Custom	Document Number <b>MS-163A</b>	Rev <b>0C</b>
Date: Friday, July 06, 2007	Sheet 17	of 54

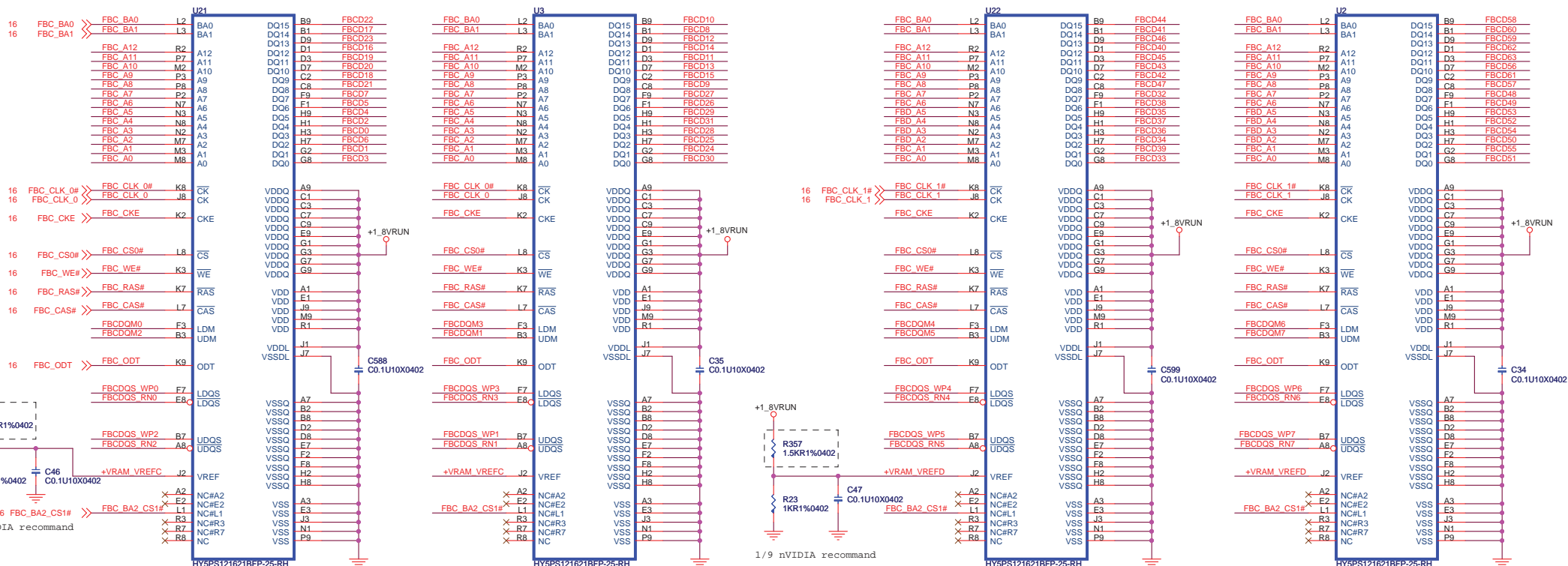


U27G		U27G	
AA12	GND	D4	GND
AA2	GND	D7	GND
AA3	GND	F11	GND
AA4	GND	F14	GND
AA5	GND	E19	GND
AA6	GND	F2	GND
AA7	GND	F22	GND
AA8	GND	E25	GND
AA9	GND	F31	GND
AA10	GND	F8	GND
AA11	GND	G26	GND
AA12	GND	G29	GND
AA13	GND	G4	GND
AA14	GND	G7	GND
AA15	GND	H6	GND
AA16	GND	H27	GND
AA17	GND	H6	GND
AA18	GND	J16	GND
AA19	GND	J17	GND
AA20	GND	J2	GND
AA21	GND	J31	GND
AA22	GND	K10	GND
AA23	GND	K23	GND
AA24	GND	K29	GND
AA25	GND	K4	GND
AA26	GND	L27	GND
AA27	GND	L6	GND
AA28	GND	M12	GND
AA29	GND	M2	GND
AA30	GND	M11	GND
AA31	GND	N15	GND
AA32	GND	N18	GND
AA33	GND	N29	GND
AA34	GND	N4	GND
AA35	GND	P15	GND
AA36	GND	P18	GND
AA37	GND	P27	GND
AA38	GND	P6	GND
AA39	GND	R13	GND
AA40	GND	R14	GND
AA41	GND	R15	GND
AA42	GND	R18	GND
AA43	GND	R19	GND
AA44	GND	R2	GND
AA45	GND	R20	GND
AA46	GND	R31	GND
AA47	GND	T16	GND
AA48	GND	T17	GND
AA49	GND	T24	GND
AA50	GND	T29	GND
AA51	GND	T4	GND
AA52	GND	U16	GND
AA53	GND	U17	GND
AA54	GND	U24	GND
AA55	GND	U29	GND
AA56	GND	U8	GND
AA57	GND	V13	GND
AA58	GND	V14	GND
AA59	GND	V15	GND
AA60	GND	V18	GND
AA61	GND	V19	GND
AA62	GND	V2	GND
AA63	GND	V20	GND
AA64	GND	V31	GND
AA65	GND	W15	GND
AA66	GND	W18	GND
AA67	GND	W27	GND
AA68	GND	W6	GND
AA69	GND	Y15	GND
AA70	GND	Y18	GND
AA71	GND	Y29	GND
AA72	GND	Y4	GND
AA73	GND	Y4	GND
AA74	GND	Y10	GND
AA75	GND	Y11	GND
AA76	GND	Y12	GND
AA77	GND	Y13	GND
AA78	GND	Y14	GND
AA79	GND	Y19	GND
AA80	GND	Y20	GND
AA81	GND	Y21	GND
AA82	GND	Y22	GND
AA83	GND	Y23	GND
AA84	GND	Y24	GND
AA85	GND	Y25	GND
AA86	GND	Y26	GND
AA87	GND	Y27	GND
AA88	GND	Y28	GND
AA89	GND	Y29	GND
AA90	GND	Y30	GND
AA91	GND	Y31	GND
AA92	GND	Y32	GND
AA93	GND	Y33	GND
AA94	GND	Y34	GND
AA95	GND	Y35	GND
AA96	GND	Y36	GND
AA97	GND	Y37	GND
AA98	GND	Y38	GND
AA99	GND	Y39	GND
AA100	GND	Y40	GND
AA101	GND	Y41	GND
AA102	GND	Y42	GND
AA103	GND	Y43	GND
AA104	GND	Y44	GND
AA105	GND	Y45	GND
AA106	GND	Y46	GND
AA107	GND	Y47	GND
AA108	GND	Y48	GND
AA109	GND	Y49	GND
AA110	GND	Y50	GND
AA111	GND	Y51	GND
AA112	GND	Y52	GND
AA113	GND	Y53	GND
AA114	GND	Y54	GND
AA115	GND	Y55	GND
AA116	GND	Y56	GND
AA117	GND	Y57	GND
AA118	GND	Y58	GND
AA119	GND	Y59	GND
AA120	GND	Y60	GND
AA121	GND	Y61	GND
AA122	GND	Y62	GND
AA123	GND	Y63	GND
AA124	GND	Y64	GND
AA125	GND	Y65	GND
AA126	GND	Y66	GND
AA127	GND	Y67	GND
AA128	GND	Y68	GND
AA129	GND	Y69	GND
AA130	GND	Y70	GND
AA131	GND	Y71	GND
AA132	GND	Y72	GND
AA133	GND	Y73	GND
AA134	GND	Y74	GND
AA135	GND	Y75	GND
AA136	GND	Y76	GND
AA137	GND	Y77	GND
AA138	GND	Y78	GND
AA139	GND	Y79	GND
AA140	GND	Y80	GND
AA141	GND	Y81	GND
AA142	GND	Y82	GND
AA143	GND	Y83	GND
AA144	GND	Y84	GND
AA145	GND	Y85	GND
AA146	GND	Y86	GND
AA147	GND	Y87	GND
AA148	GND	Y88	GND
AA149	GND	Y89	GND
AA150	GND	Y90	GND
AA151	GND	Y91	GND
AA152	GND	Y92	GND
AA153	GND	Y93	GND
AA154	GND	Y94	GND
AA155	GND	Y95	GND
AA156	GND	Y96	GND
AA157	GND	Y97	GND
AA158	GND	Y98	GND
AA159	GND	Y99	GND
AA160	GND	Y100	GND

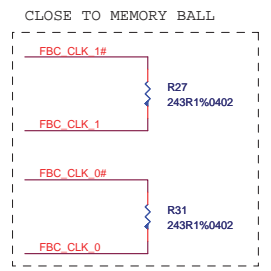
# 512 M GDDRII Channels A



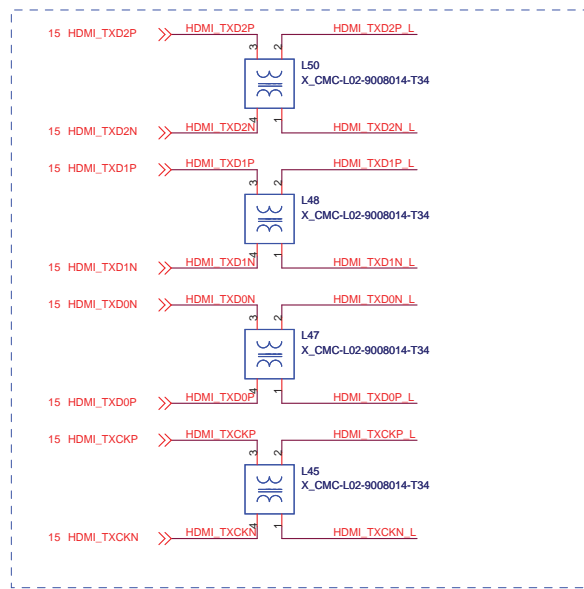
# 512 M GDDRII Channels B



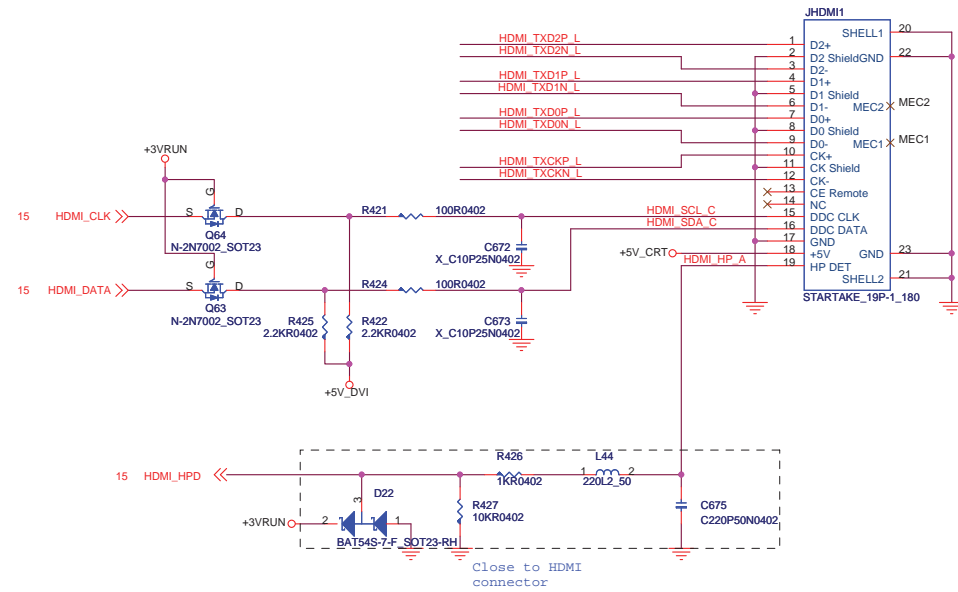
- 16 FBD\_A[5..2] >> FBD\_A[5..2]
- 16 FBCD[63..0] >> FBCD[63..0]
- 16 FBC\_A[12..0] >> FBC\_A[12..0]
- 16 FBCDQS\_WP[7..0] >> FBCDQS\_WP[7..0]
- 16 FBCDQS\_RN[7..0] >> FBCDQS\_RN[7..0]
- 16 FBCDQM[7..0] >> FBCDQM[7..0]





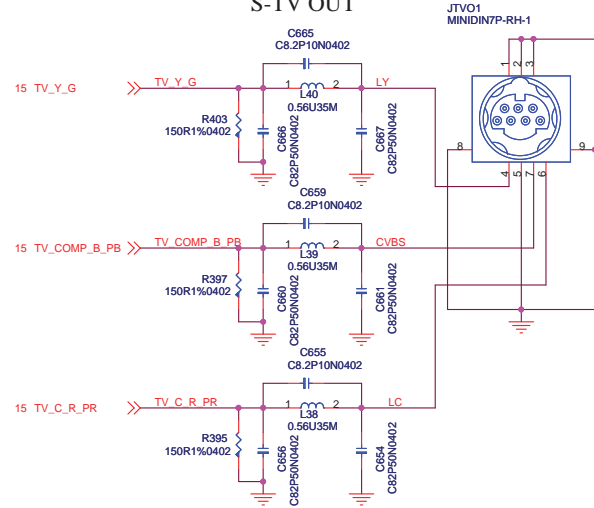


CLOSE TO CONNECTOR

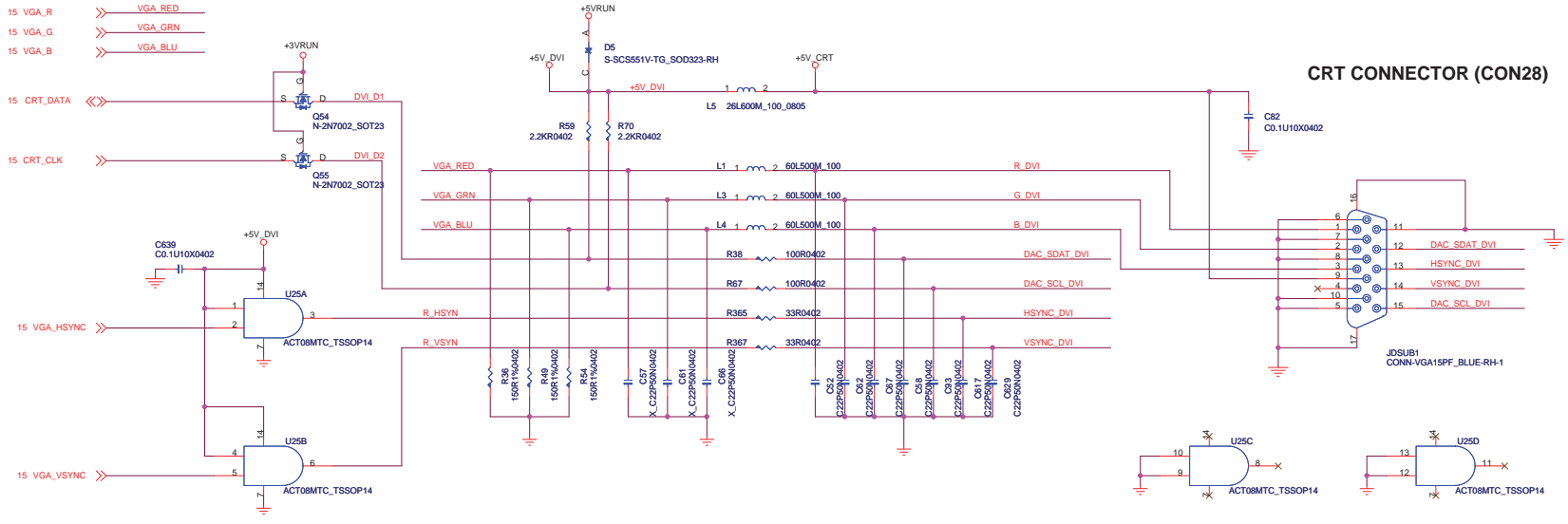


Close to HDMI connector

### S-TV OUT

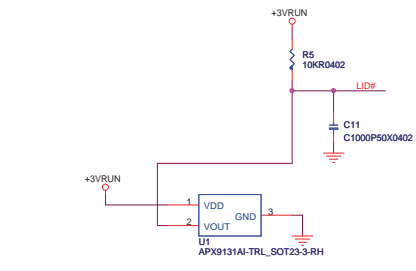
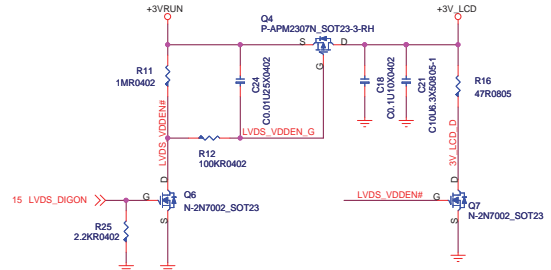


<b>MSI CORPORATION</b>		
Title	<b>HDMI &amp; TV connector</b>	
Size	Document Number	Rev
Custom	<b>MS-163A</b>	<b>0A</b>
Date:	Wednesday, July 04, 2007	Sheet 21 of 54

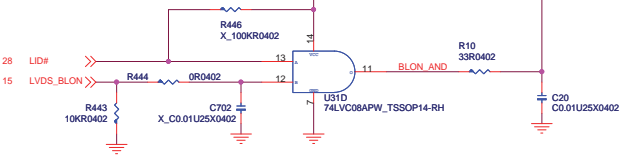


**CRT CONNECTOR (CON28)**

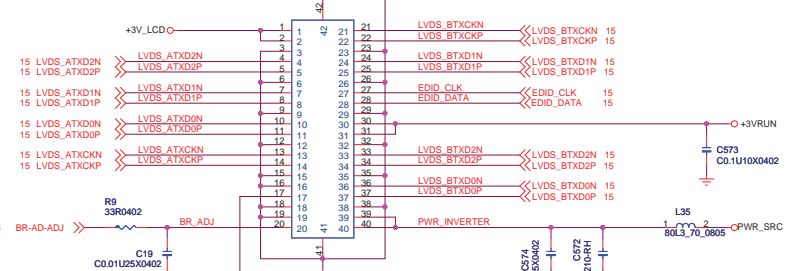
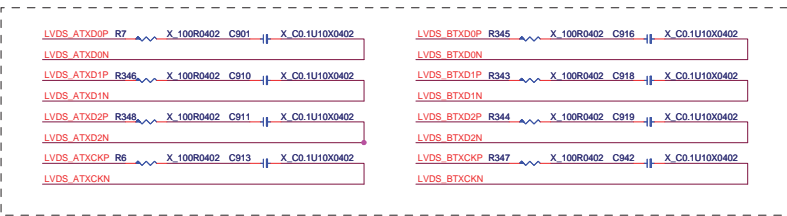
JDSUB1  
CONN-VGA15PF\_BLUE-RH-1

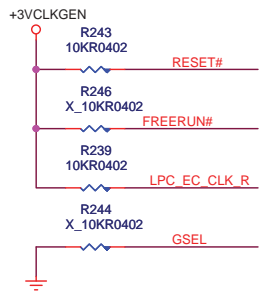


**R406 have to be NC after EVT**



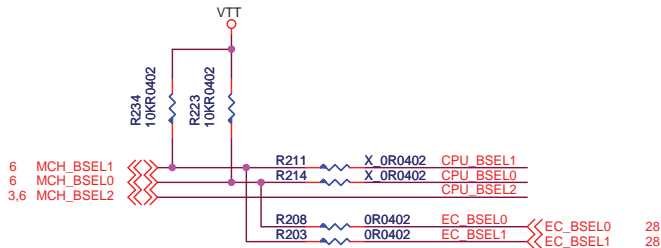
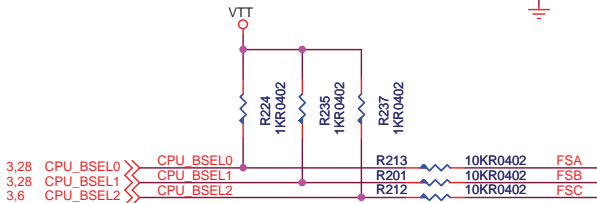
For EMI



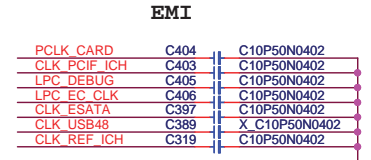
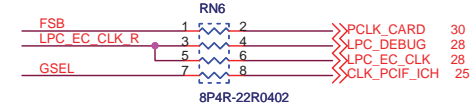
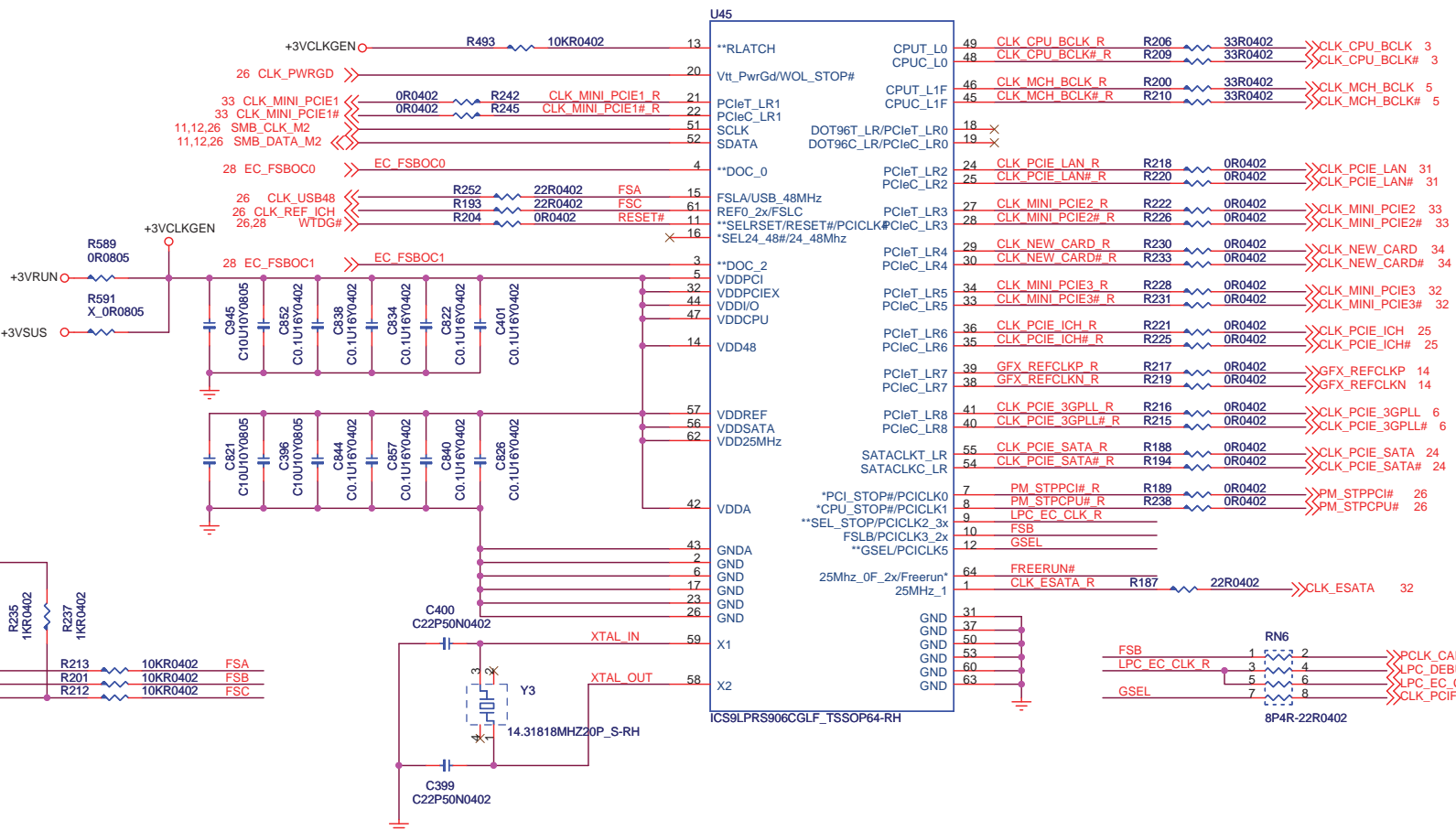


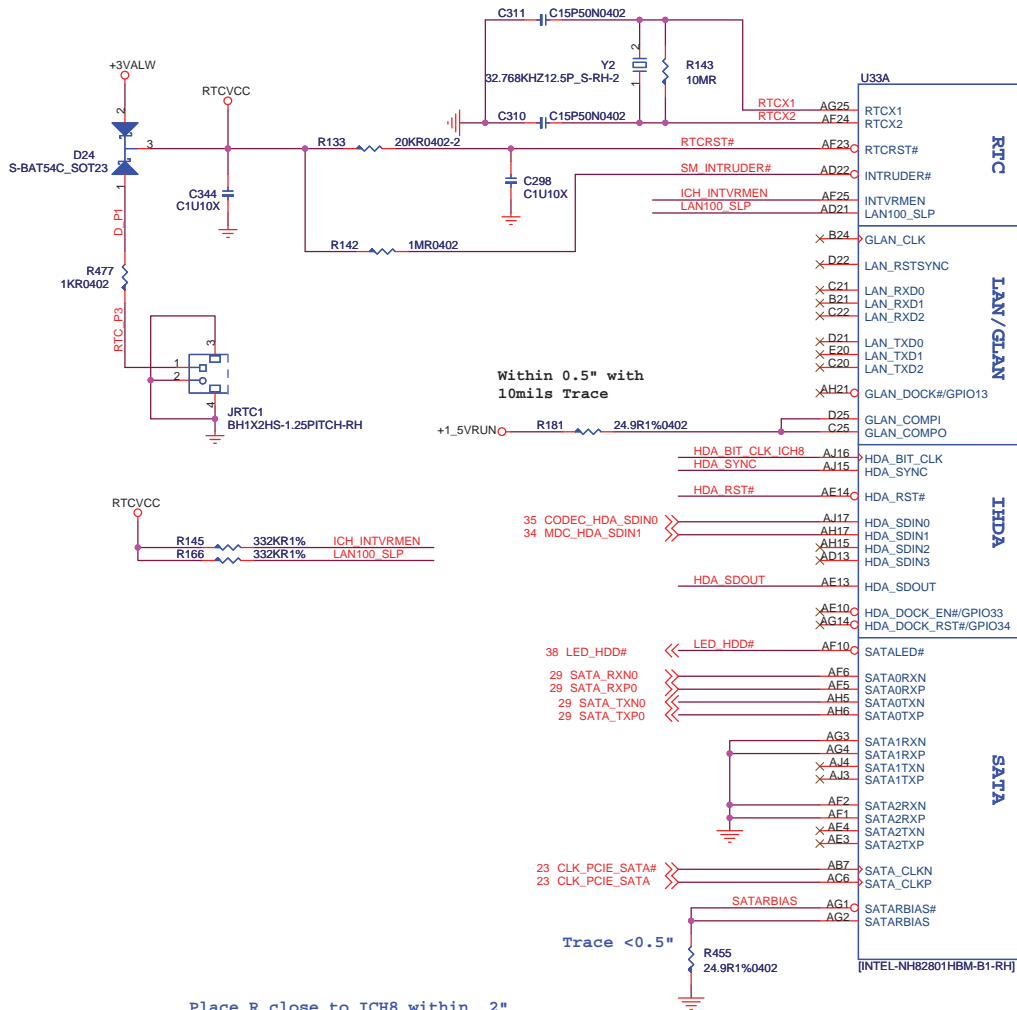
PIN 7,8 FUNCTION	PIN 9 STRAP
CPU/PCI STOP	1
PCICLK	0

PIN 18,19 FUNCTION	PIN 12 STRAP
96M	1
PCIe	0



CPU Table			FSB Freq (MHz)
BSEL[2]	BSEL[1]	BSEL[0]	
L	H	H	667 MHz
L	H	L	800 MHz

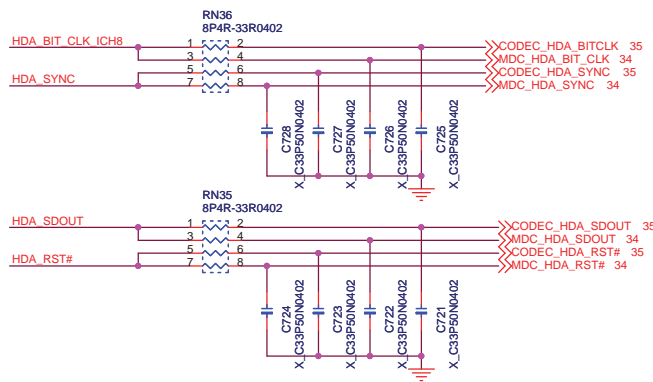
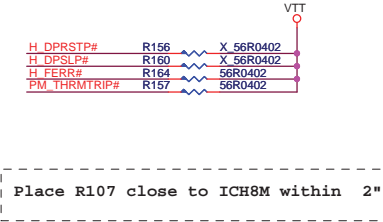




Within 0.5" with 10mils Trace

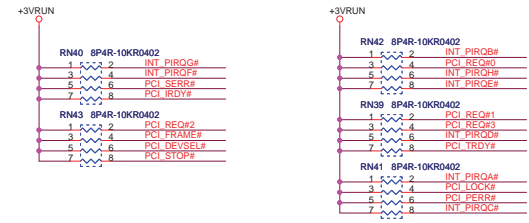
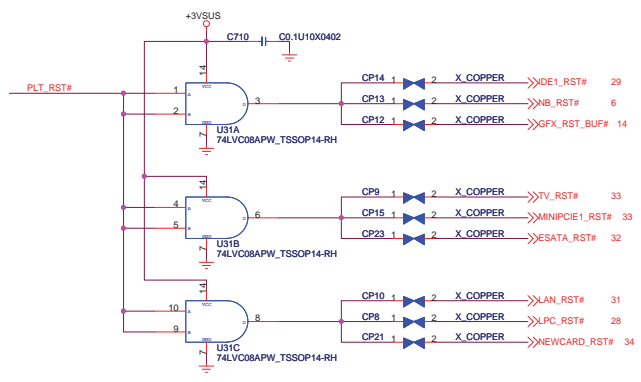
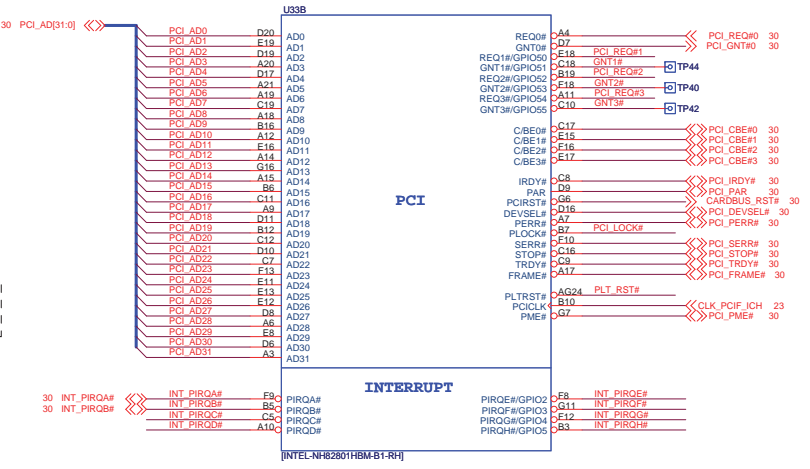
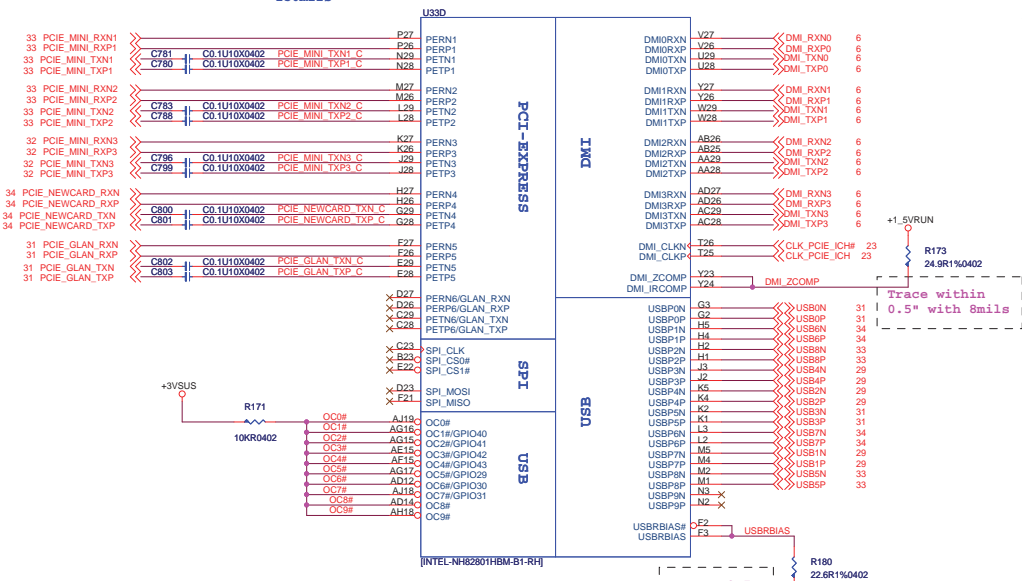
Place R close to ICH8 within 2"

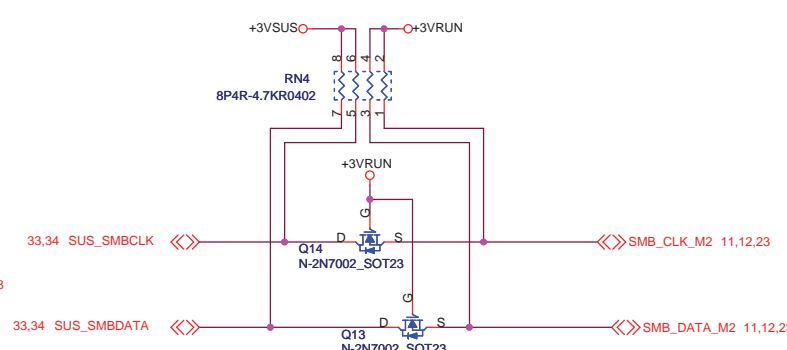
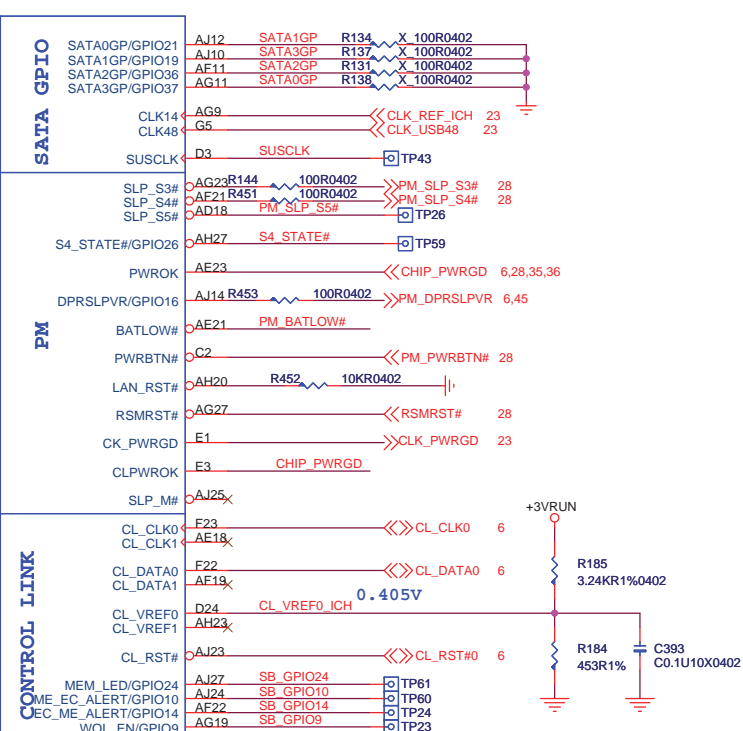
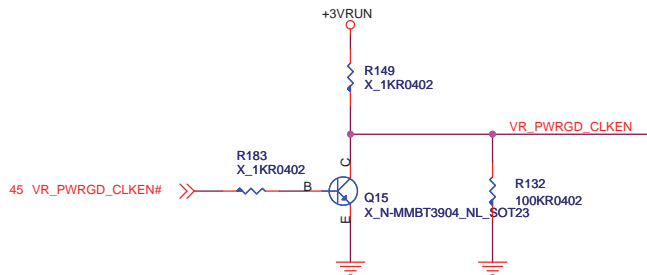
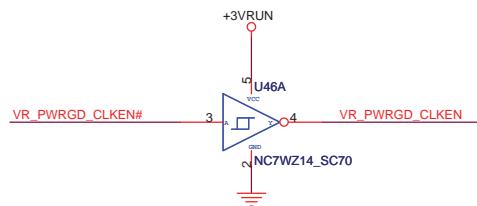
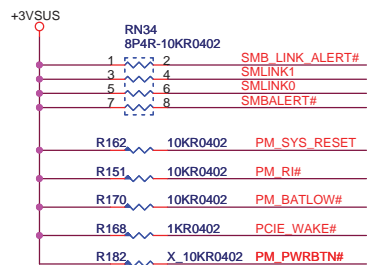
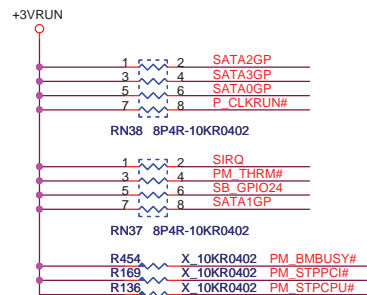
Trace <0.5"



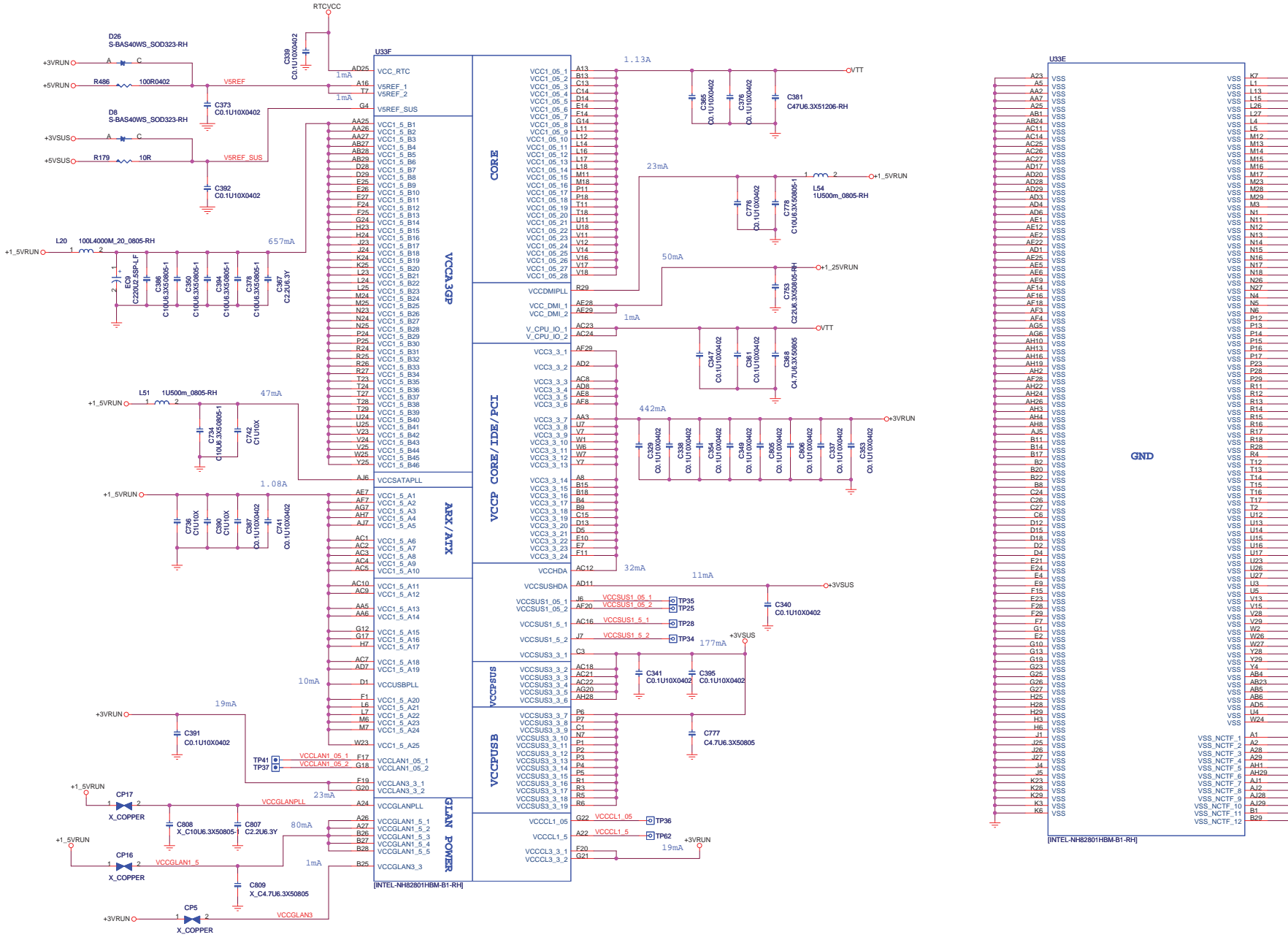
<b>MSI CORPORATION</b>		
<b>ICH8M-1 (CPU/IDE/Azalia)</b>		
Size	Document Number	Rev
Custom	<b>MS-163A</b>	0A
Date:	Wednesday, July 04, 2007	Sheet 24 of 54

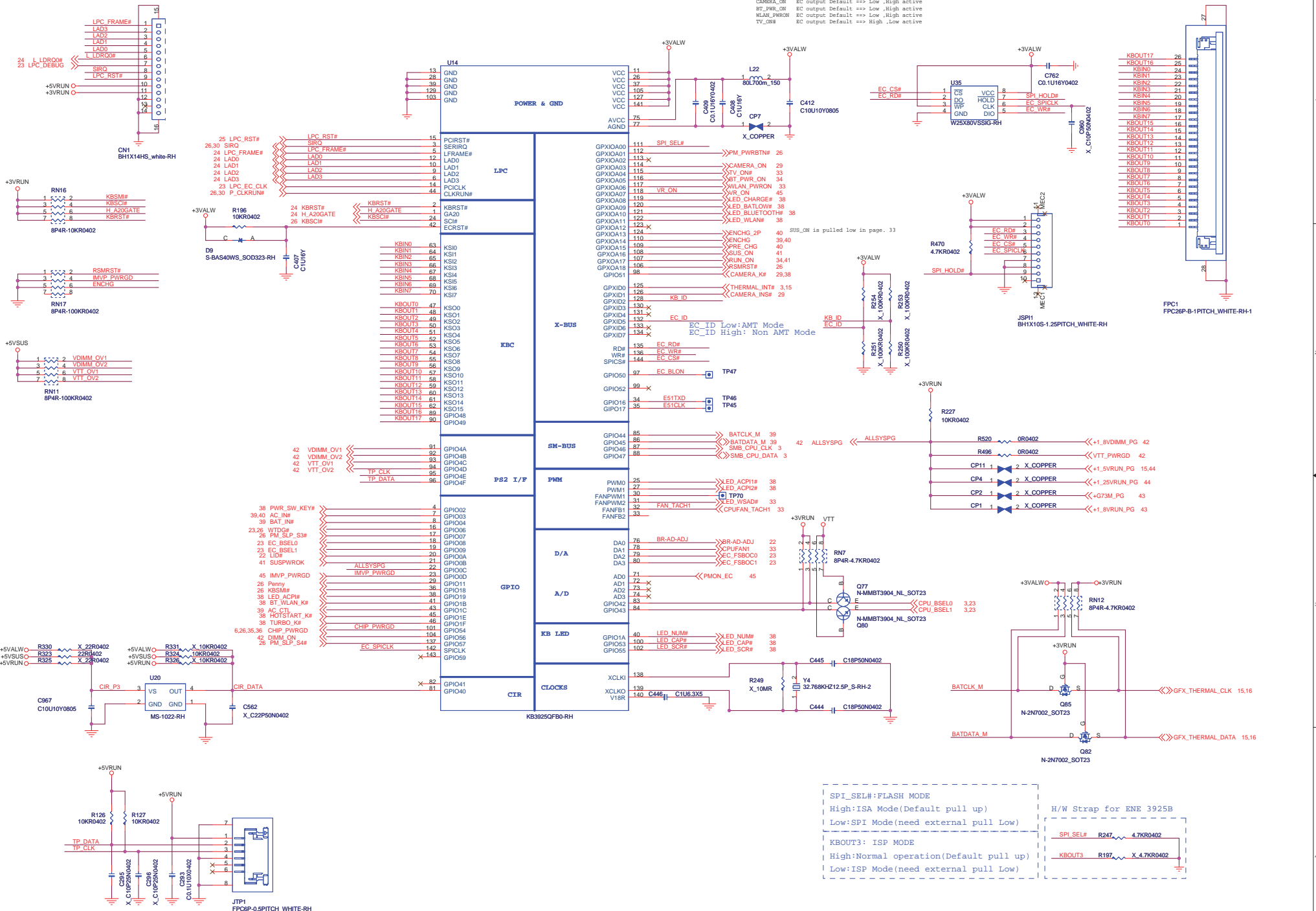
place Cap  
close to  
IC8 within  
250mils







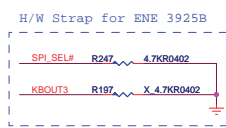




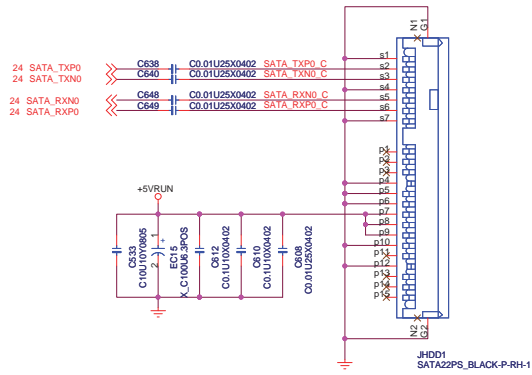
CAMERA\_ON EC output Default ==> Low ,High active  
 BT\_PWR\_ON EC output Default ==> Low ,High active  
 WLAN\_PWR\_ON EC output Default ==> Low ,High active  
 TV\_ON# EC output Default ==> High ,Low active

SPI\_SEL#: FLASH MODE  
 High: ISA Mode(Default pull up)  
 Low: SPI Mode(need external pull Low)

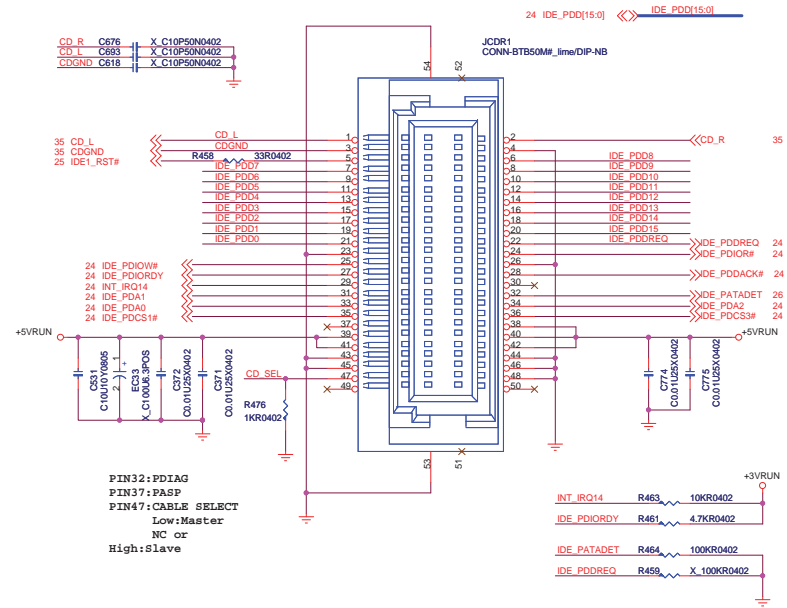
KBOUT3: ISP MODE  
 High: Normal operation(Default pull up)  
 Low: ISP Mode(need external pull Low)



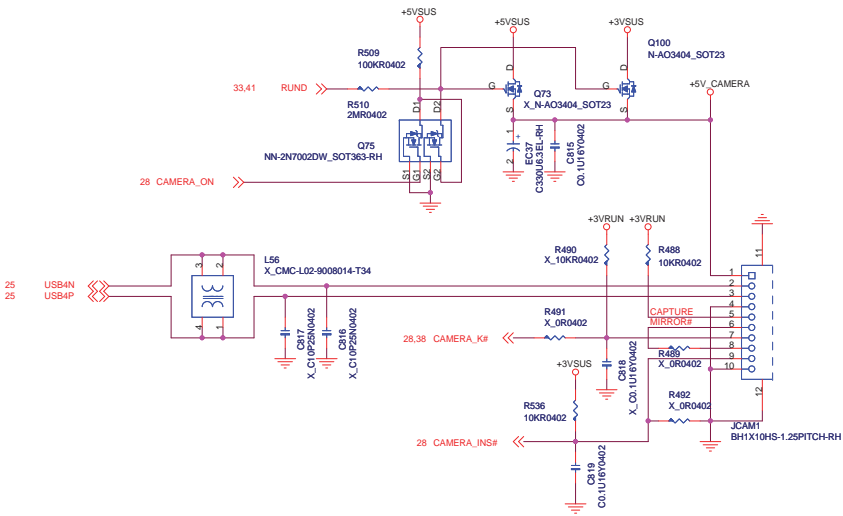
### HDD CONN



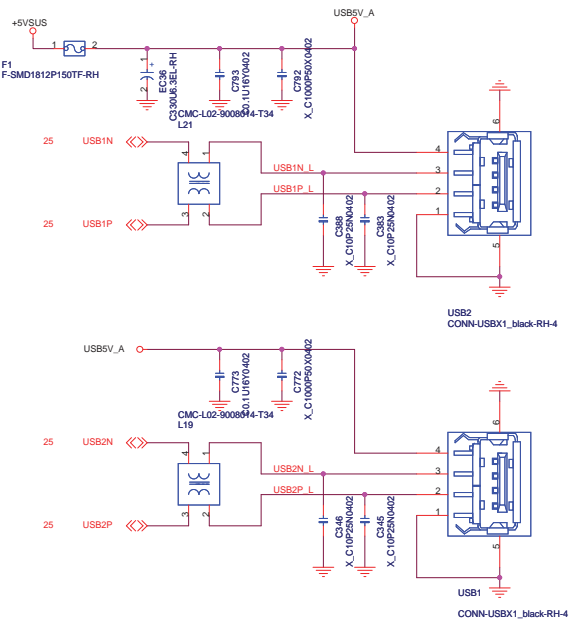
### ODD CONN

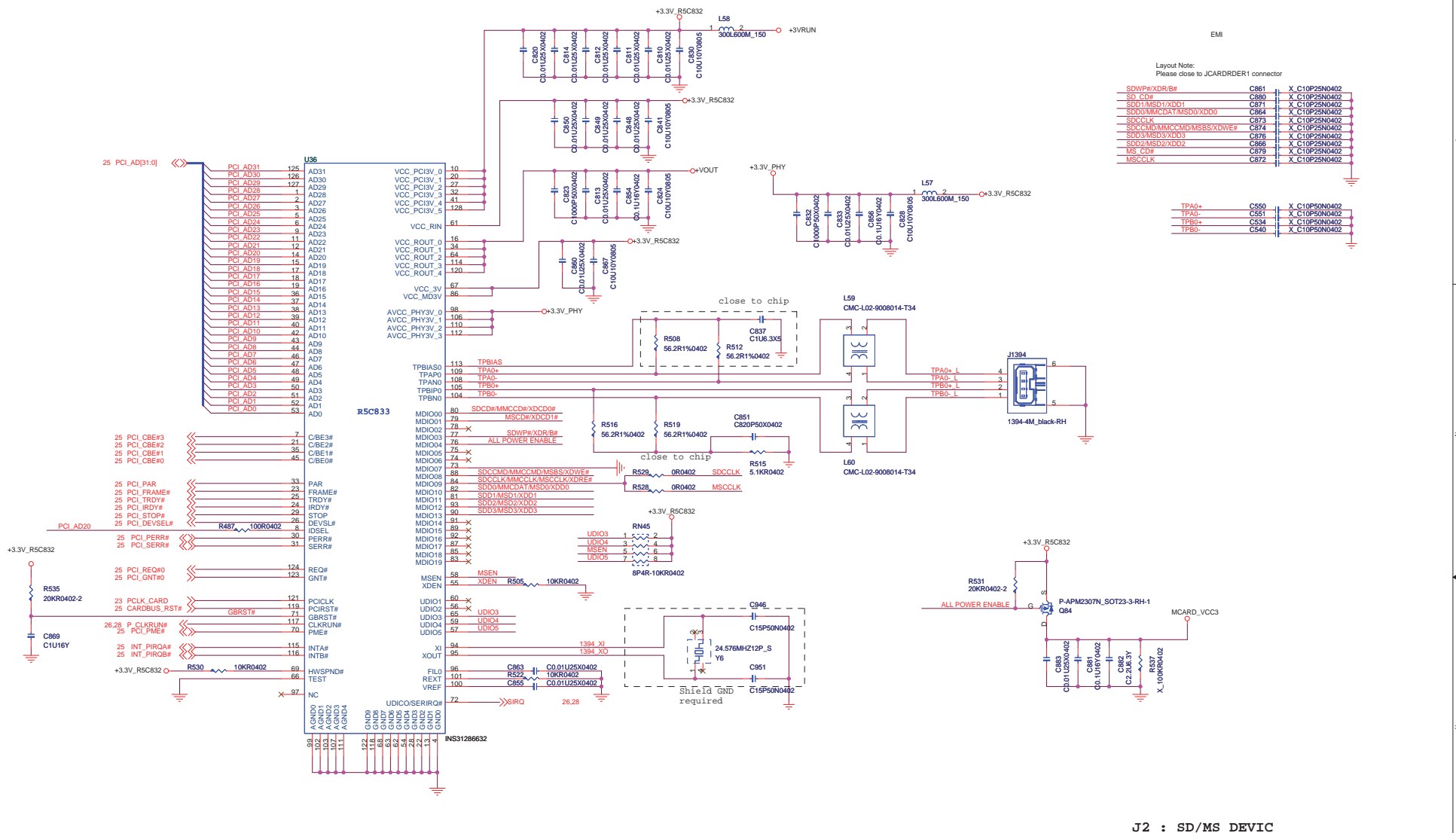


### CAMERA CONN



### USB CONN





Layout Note:  
Please close to JCARDRDR1 connector

SDWP#XDR/B#	C861	X	C10P25N0402
SD_CD#	C880	X	C10P25N0402
SD01/MSD1/XDD1	C871	X	C10P25N0402
SD00/MC/DAT/MSD0/XDD0	C864	X	C10P25N0402
SDCLK	C873	X	C10P25N0402
SDCCM/MMCC/MID/MSBS/XDWE#	C874	X	C10P25N0402
SD03/MSD3/XDD3	C866	X	C10P25N0402
SD02/MSD2/XDD2	C868	X	C10P25N0402
MS_CD#	C879	X	C10P25N0402
MSCCLK	C872	X	C10P25N0402

TPA0+	C550	X	C10P50N0402
TPA0-	C551	X	C10P50N0402
TPB0+	C554	X	C10P50N0402
TPB0-	C540	X	C10P50N0402

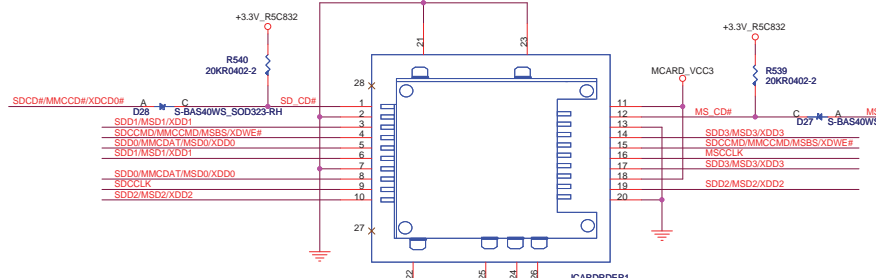
J2 : SD/MS DEVIC

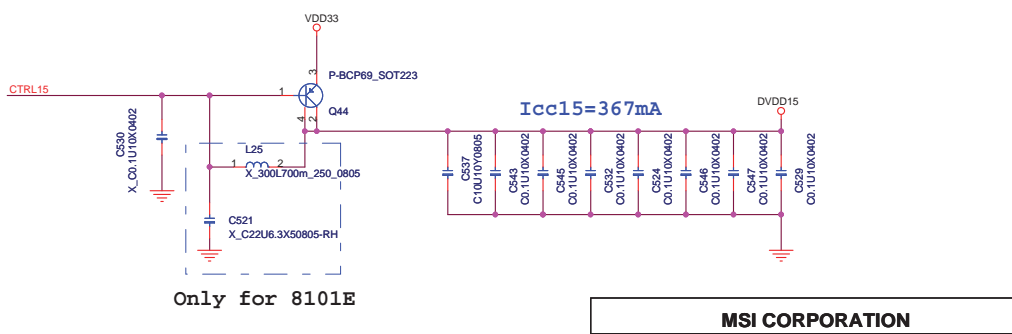
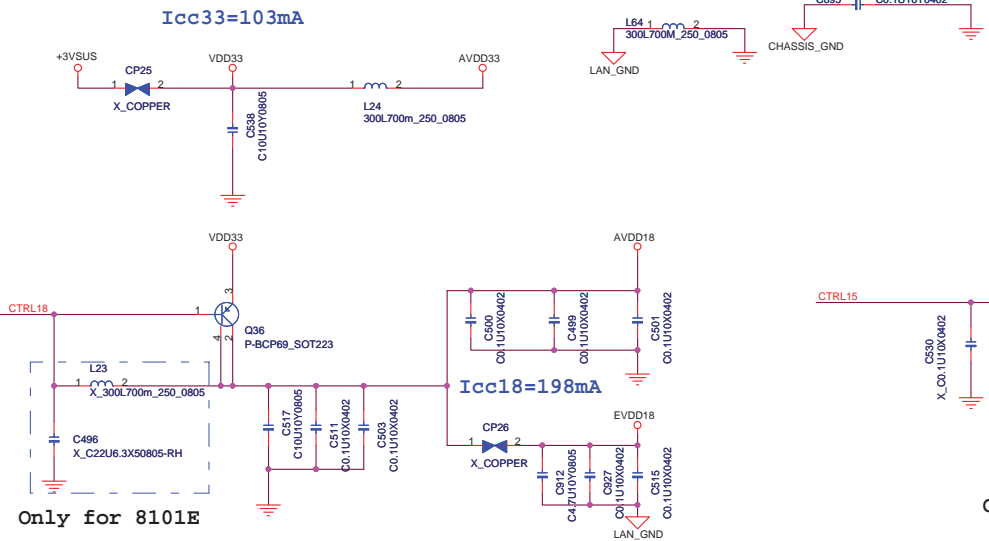
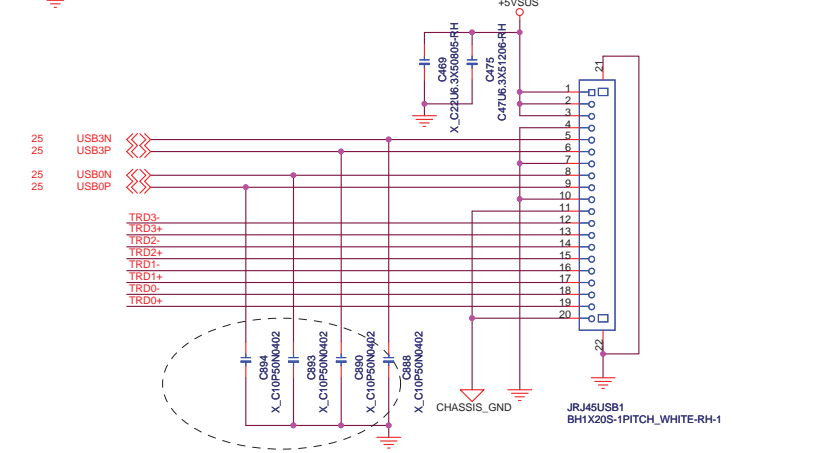
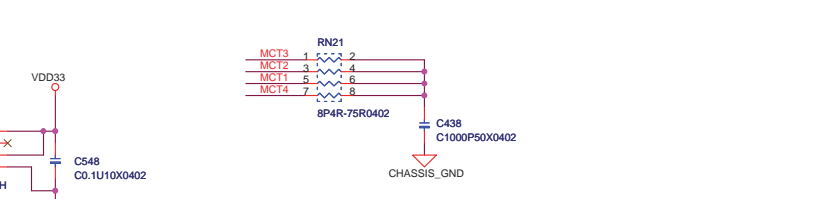
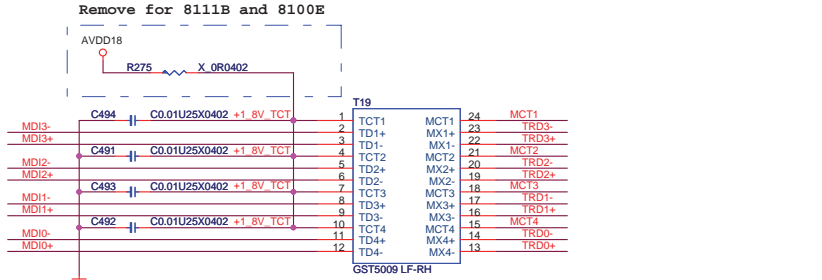
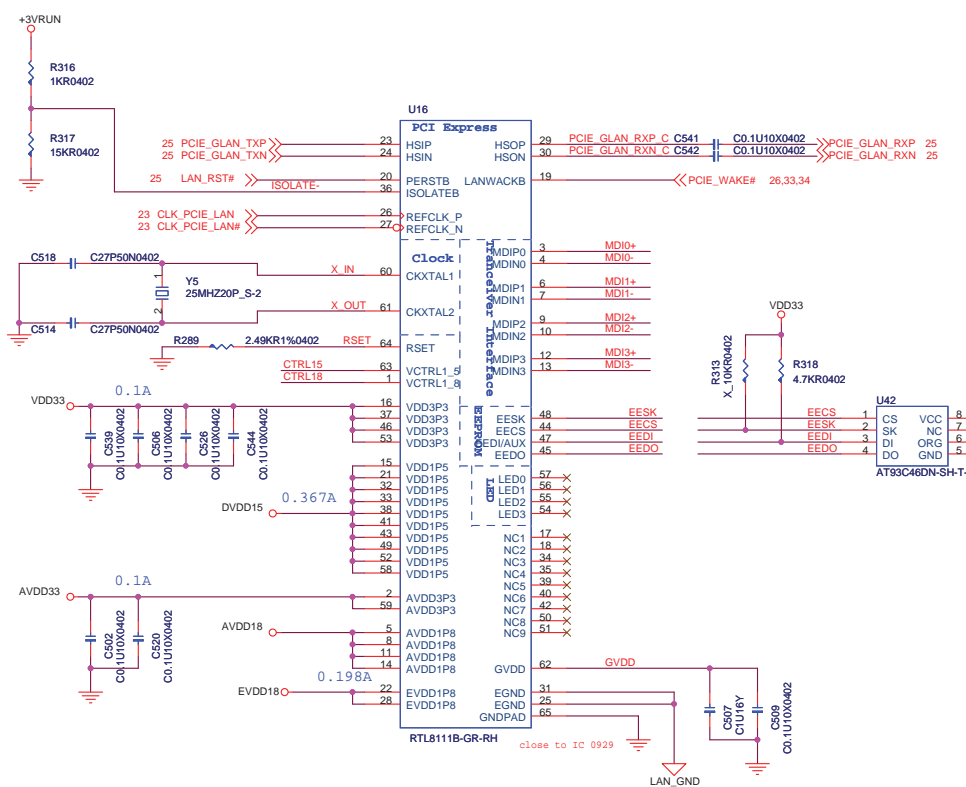
Pin	Description	Pin	Description
1	Card Detect SW	2	MS VSS
3	SD Data1	4	MS BS
5	SD Data0	6	MS Data1
7	SD VSS	8	MS Data0
9	SD CLK	10	MS Data2
11	SD VDD	12	MS INS
13	SD VSS	14	MS Data3
15	SD CMD	16	MS CLK
17	SD Data3	18	MS VDD
19	SD Data2	20	MS VSS
		26	SD_WP

MSD1A	SD	MMC	MS	MS
MDIO0	SDCD#	MMCDD#	MSCD#	XDCD#
MDIO1	SDCD#	MMCDD#	MSCD#	XDCD#
MDIO2	SDWP#	MMCWP#	MSWP#	XDWP#
MDIO3	SDWP#	MMCWP#	MSWP#	XDWP#
MDIO4	SDWP#	MMCWP#	MSWP#	XDWP#
MDIO5	SDWP#	MMCWP#	MSWP#	XDWP#
MDIO6	SDWP#	MMCWP#	MSWP#	XDWP#
MDIO7	SDWP#	MMCWP#	MSWP#	XDWP#
MDIO8	SDWP#	MMCWP#	MSWP#	XDWP#
MDIO9	SDWP#	MMCWP#	MSWP#	XDWP#
MDIO10	SDWP#	MMCWP#	MSWP#	XDWP#
MDIO11	SDWP#	MMCWP#	MSWP#	XDWP#
MDIO12	SDWP#	MMCWP#	MSWP#	XDWP#
MDIO13	SDWP#	MMCWP#	MSWP#	XDWP#
MDIO14	SDWP#	MMCWP#	MSWP#	XDWP#
MDIO15	SDWP#	MMCWP#	MSWP#	XDWP#
MDIO16	SDWP#	MMCWP#	MSWP#	XDWP#
MDIO17	SDWP#	MMCWP#	MSWP#	XDWP#
MDIO18	SDWP#	MMCWP#	MSWP#	XDWP#
MDIO19	SDWP#	MMCWP#	MSWP#	XDWP#

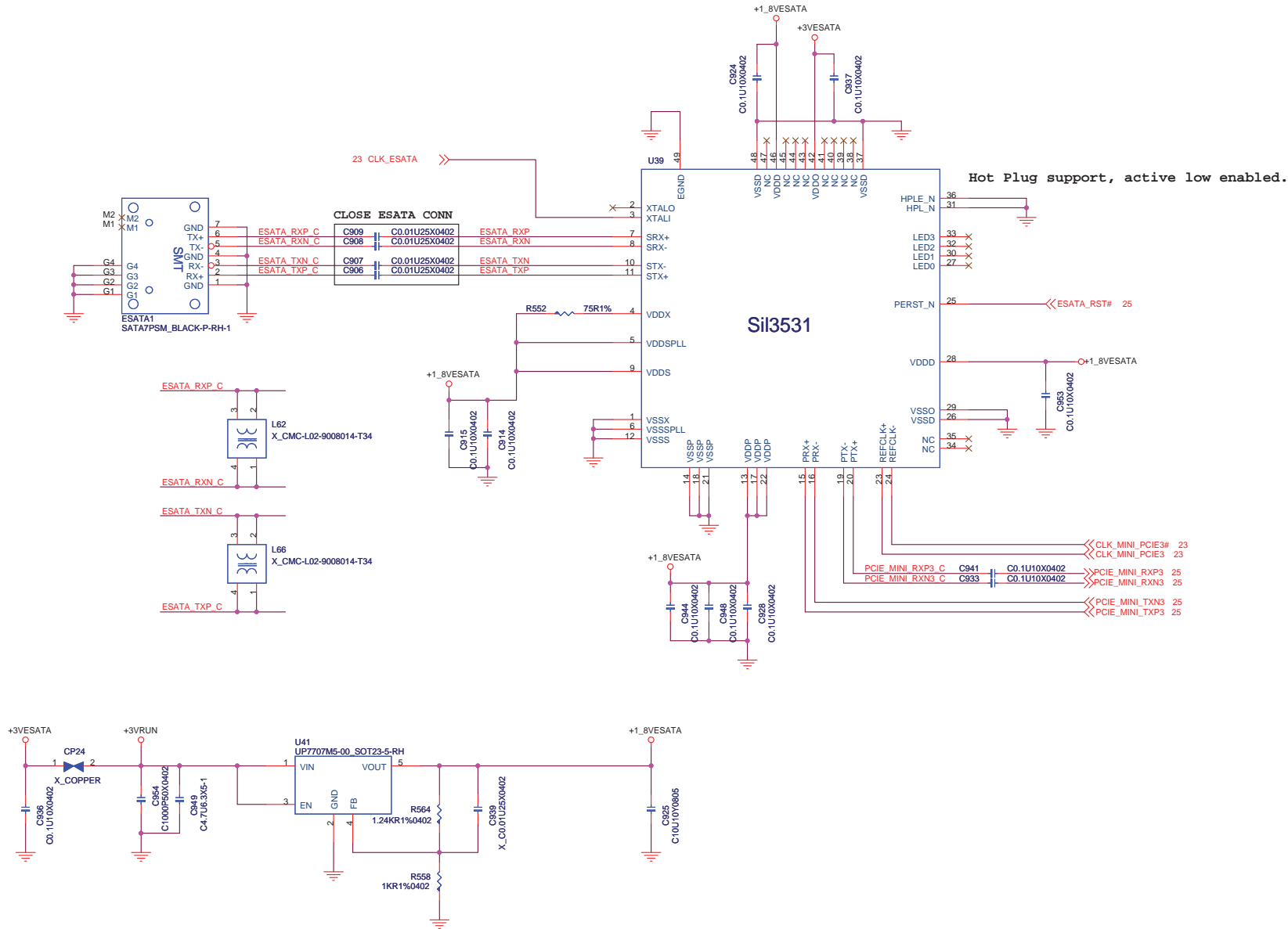
UDIO3	UDIO4	MSEN	XDEN	FUNCTION (ENABLE)
HIGH	HIGH	HIGH	LOW	SD, MMC, MSCARD

<b>MSI CORPORATION</b>			
<b>CardReader (Ricoch-R5C833)</b>			
File	Document Number	Rev	
C	<b>MS-163A</b>	0A	
Date:	Wednesday, July 04, 2007	Sheet	30 of 54



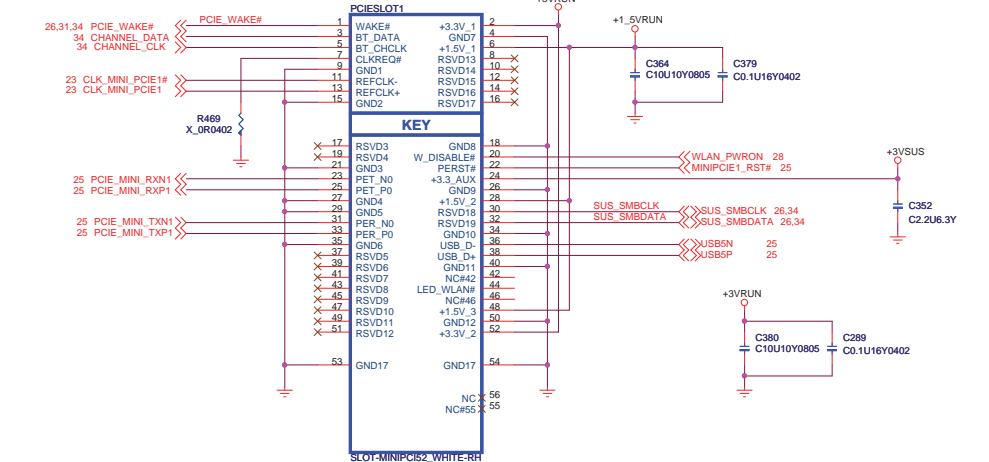


MSI CORPORATION		
Title	PCIE LAN (RTL 8111B)	
Size	Document Number	Rev
Custom	MS-163A	0A
Date:	Wednesday, July 04, 2007	Sheet 31 of 54

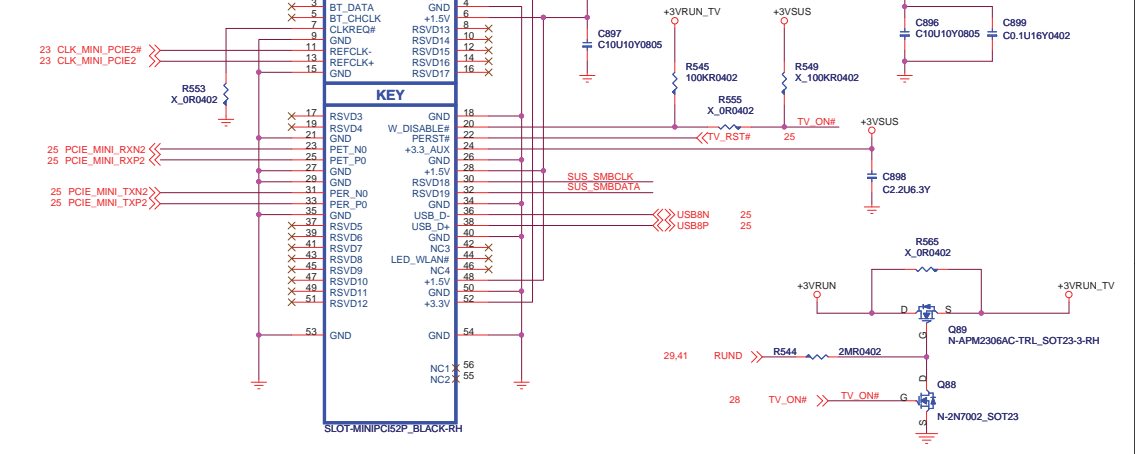


<b>MSI CORPORATION</b>		
Title <b>ESATA (SIL3531)</b>		
Size <b>Custom</b>	Document Number <b>MS-163A</b>	Rev <b>0A</b>
Date: <b>Wednesday, July 04, 2007</b>	Sheet <b>32</b> of <b>54</b>	

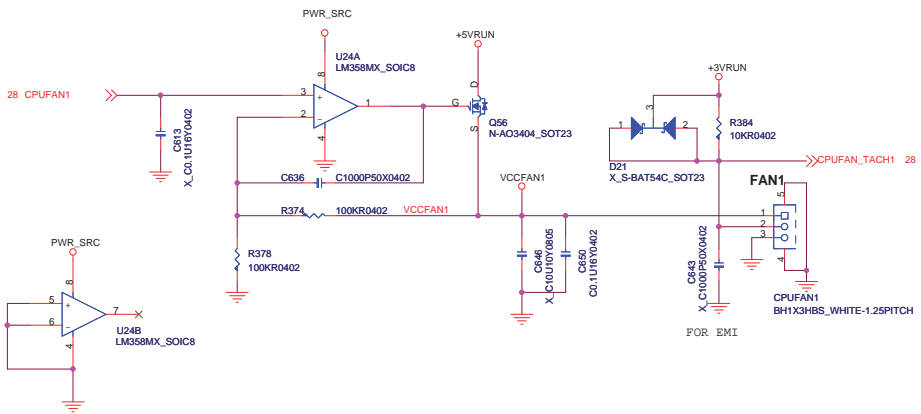
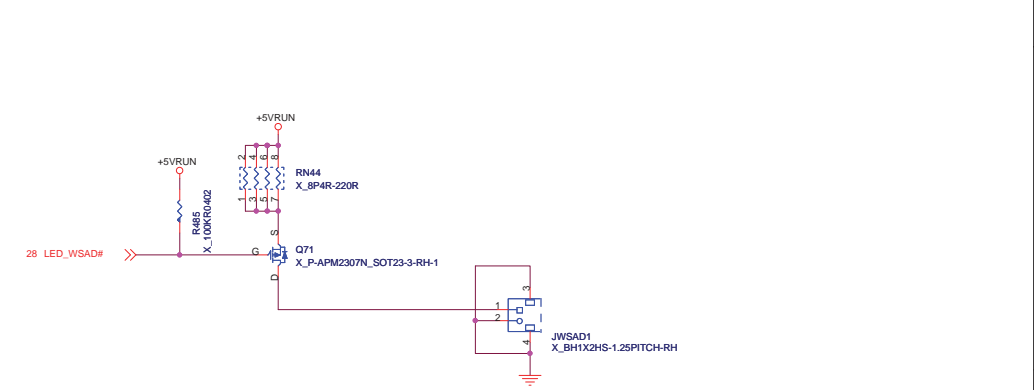
# Wireless LAN



# TV

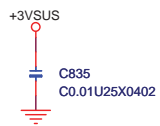
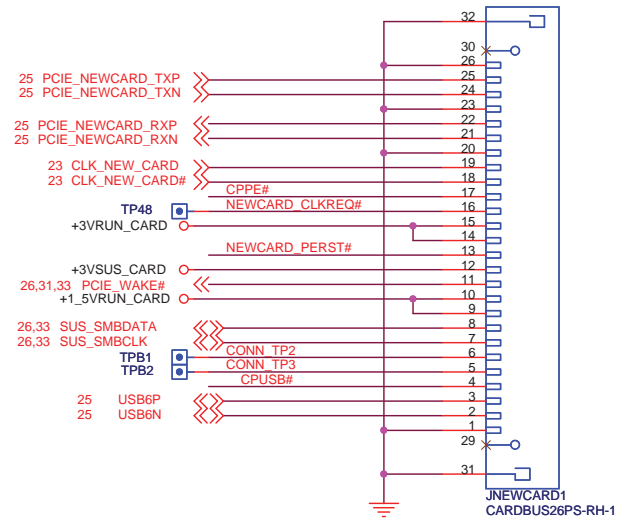
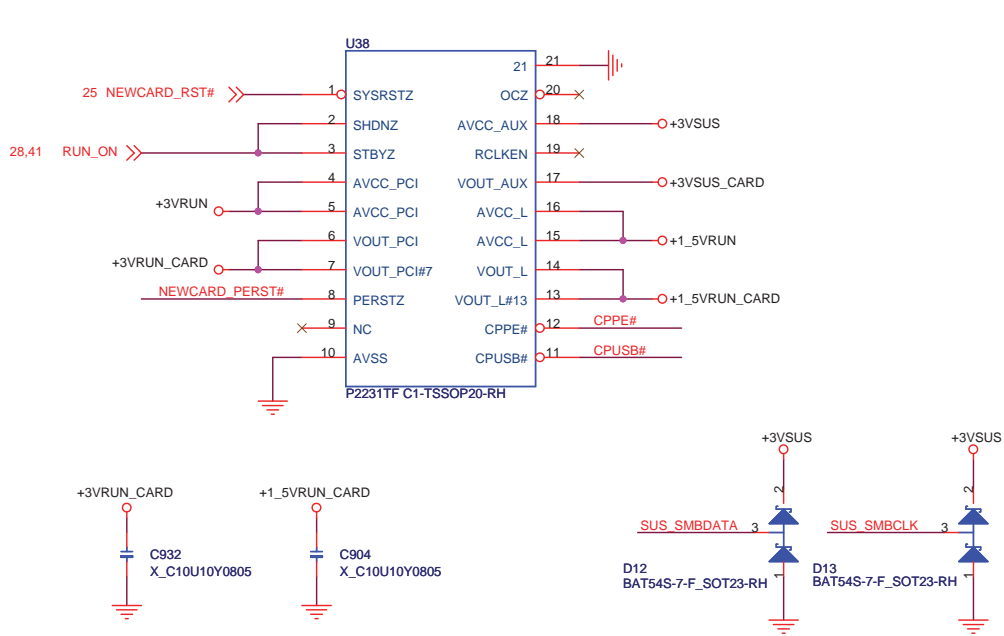


# KB-LED

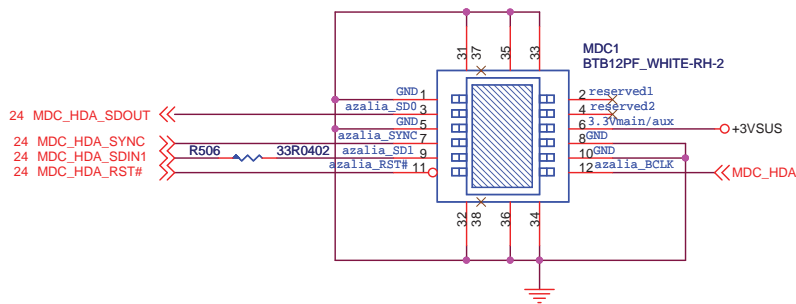


<b>MSI CORPORATION</b>			
File			
<b>MINI_PCIE / CPUFAN / KB_LED</b>			
Size	Document Number	Rev	
Custom	<b>MS-163A</b>	0A	
Date:	Wednesday, July 04, 2007	Sheet	33 of 54

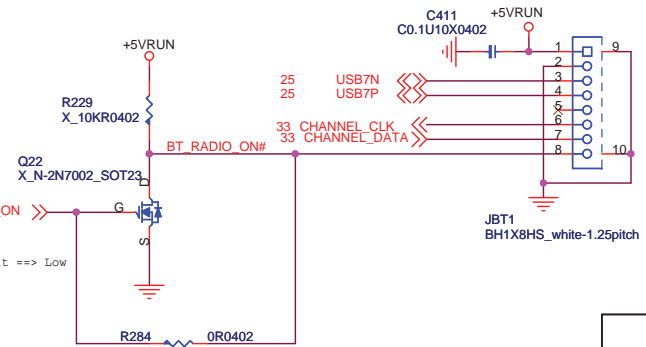




### MDC Connector Ver 1.5



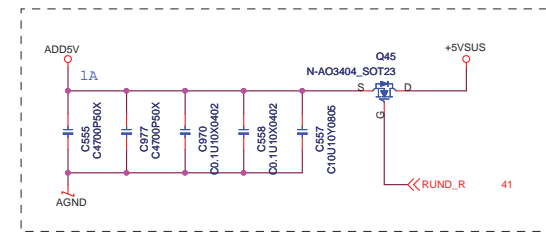
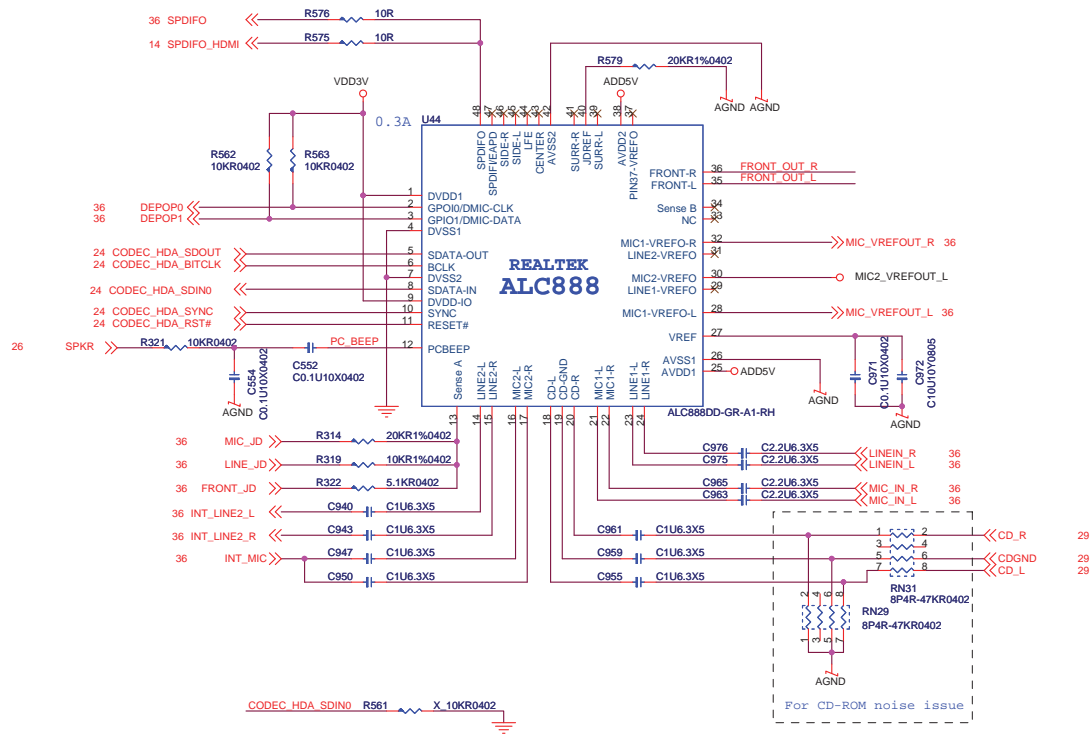
EC output Default ==> Low  
,High active



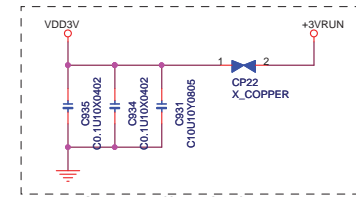
### BLUETOOTH

**MSI CORPORATION**

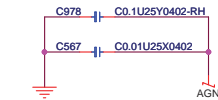
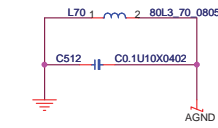
Title <b>NEWCARD &amp; MDC &amp; BT</b>		
Size Custom	Document Number <b>MS-163A</b>	Rev 0A
Date: Friday, July 06, 2007	Sheet 34	of 54



POWER ISOLATION (ANALOG 5V)

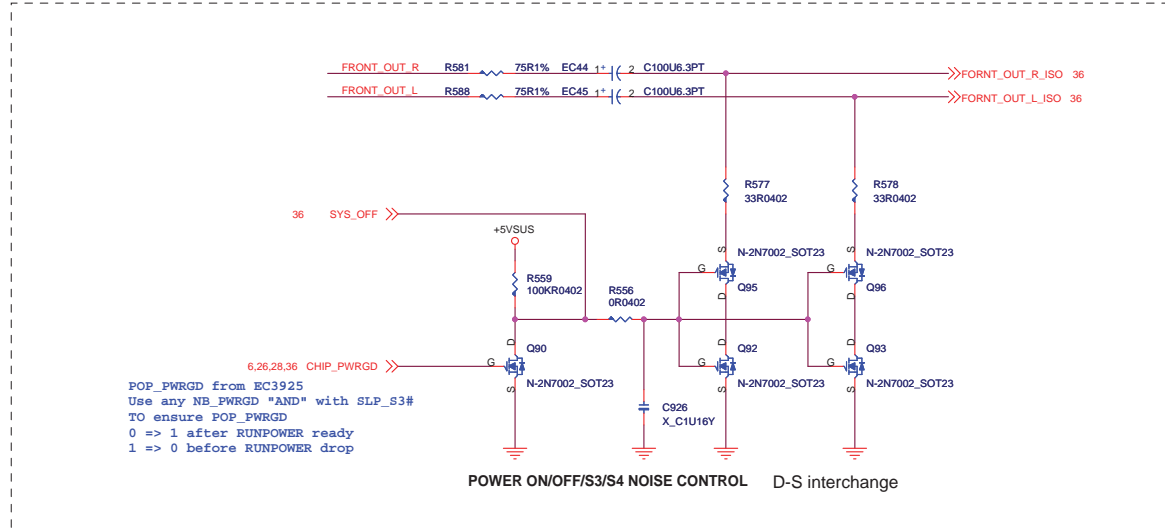


POWER ISOLATION (CODEC 3V)

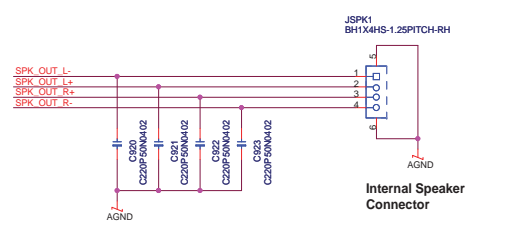
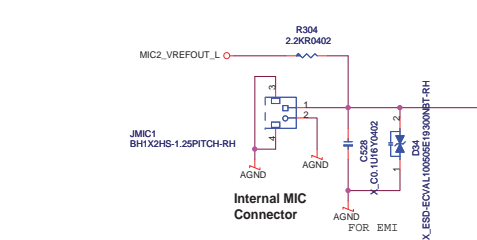
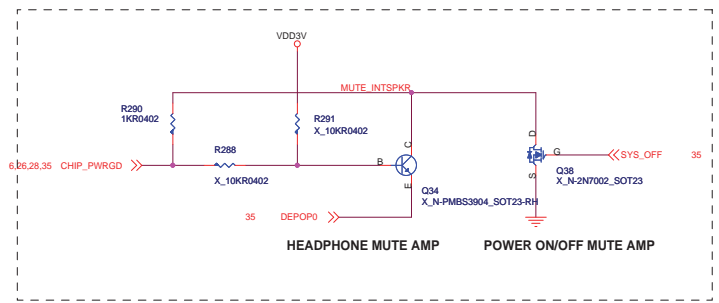
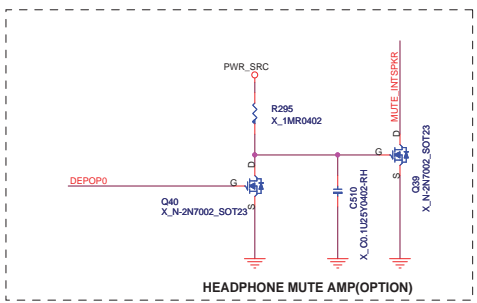
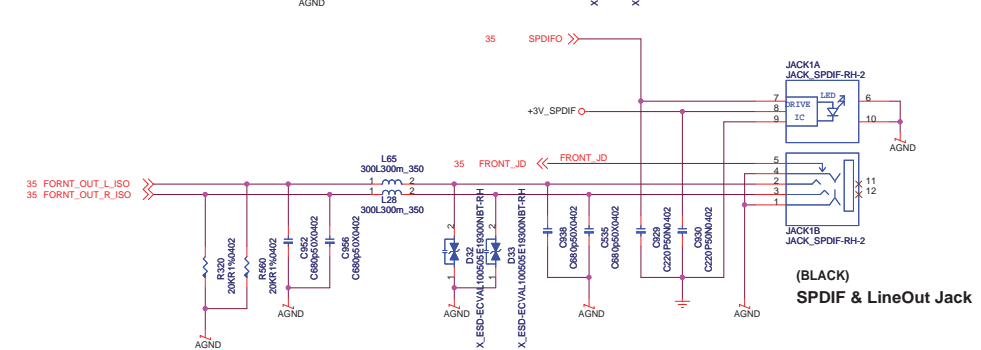
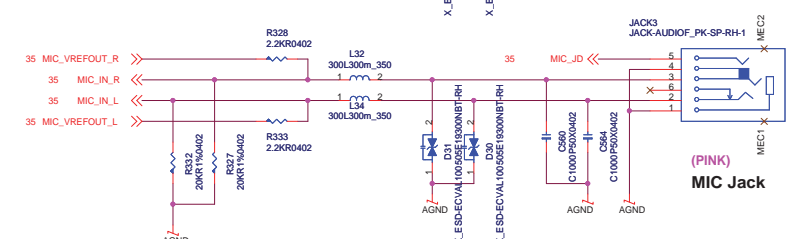
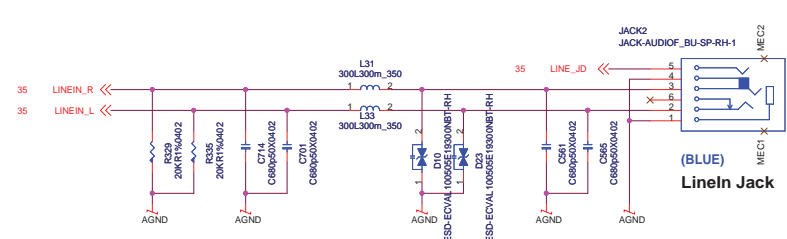
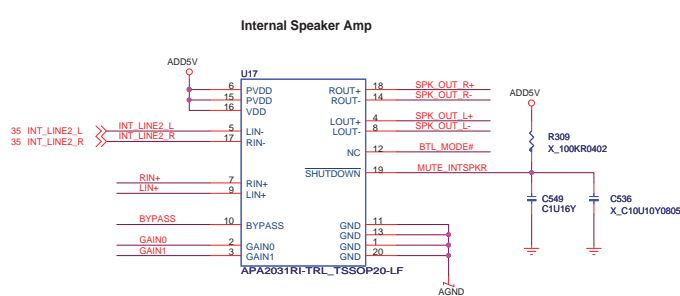
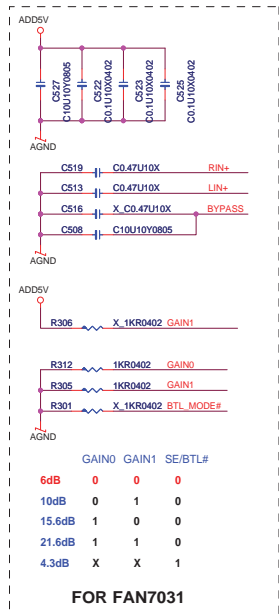


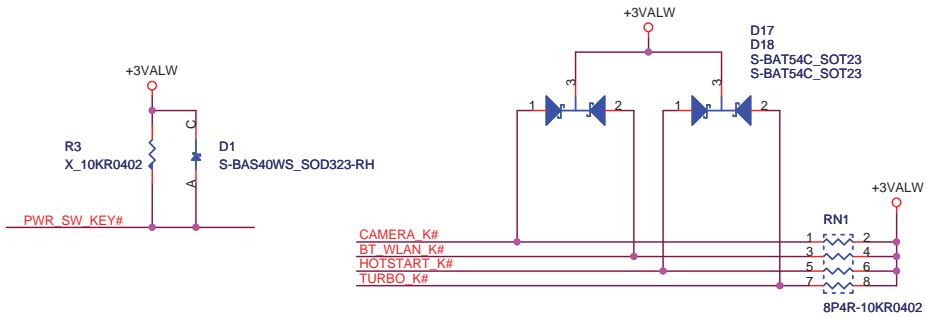
For EMI solution

ANTIPOP CIRCUIT

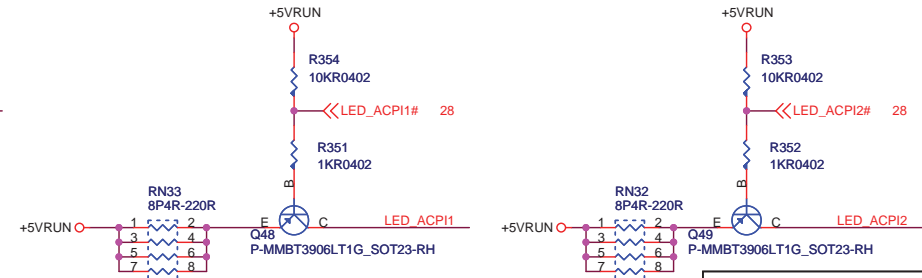
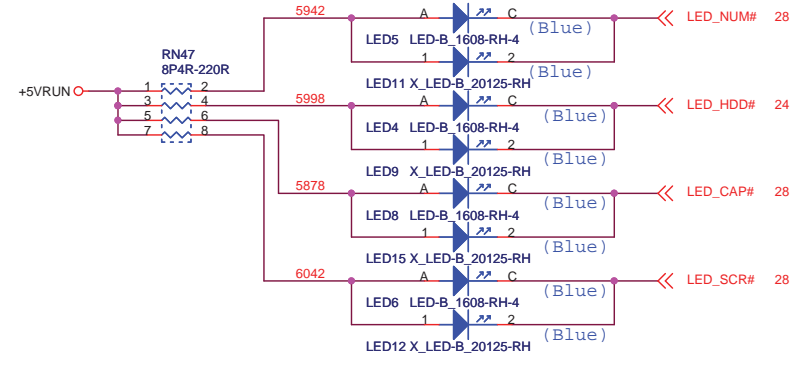
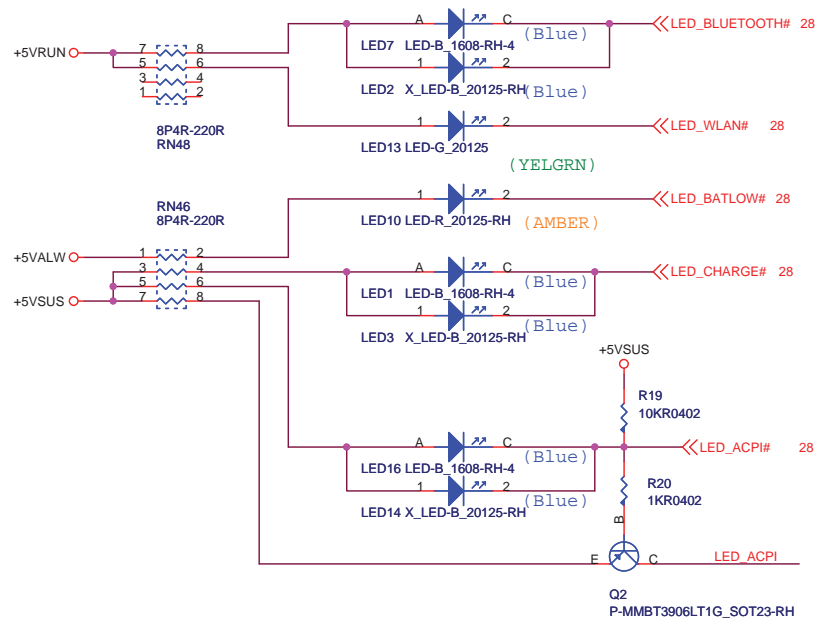
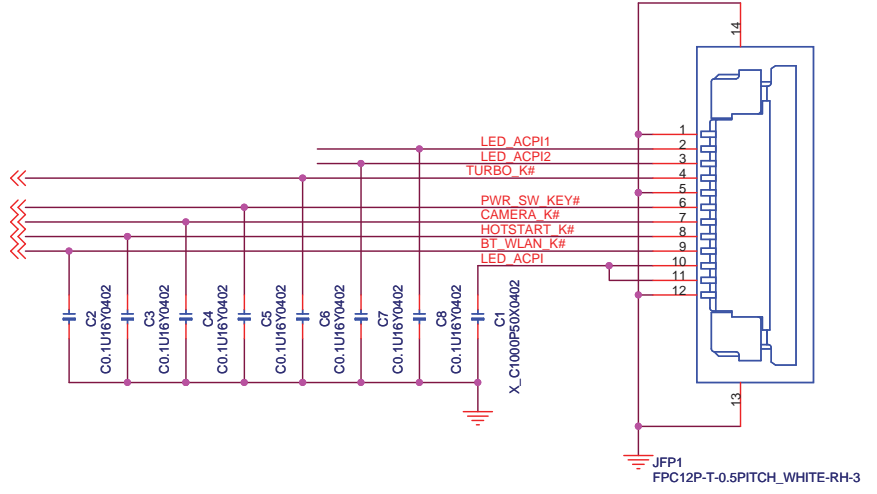


<b>MSI CORPORATION</b>		
Title	<b>AZALIA CODEC(ALC888)</b>	
Size	Document Number	Rev
Custom	<b>MS-163A</b>	OA
Date:	Wednesday, July 11, 2007	Sheet 35 of 54

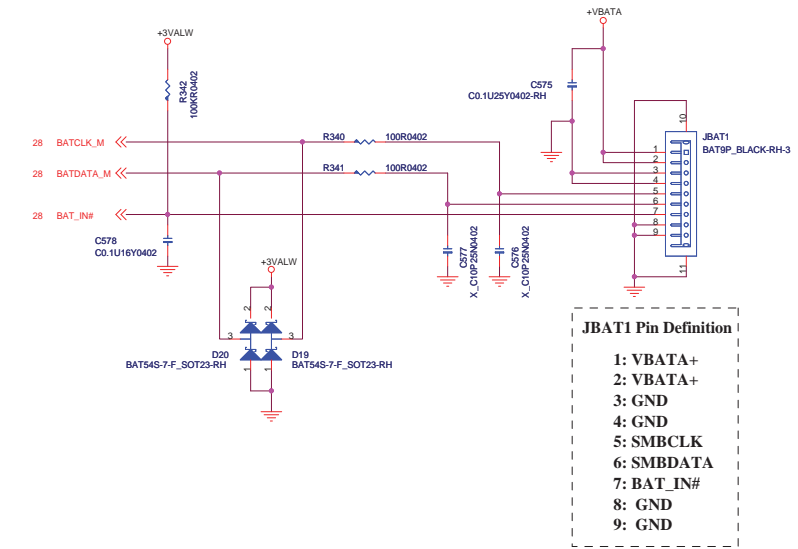
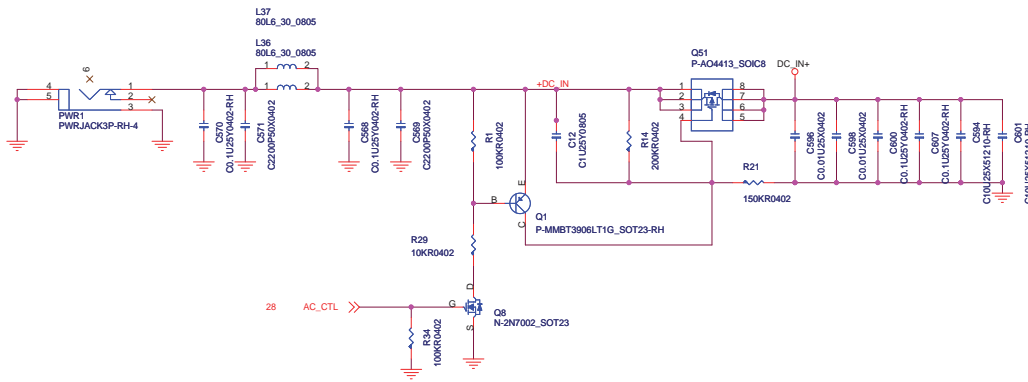




- 28 TURBO\_K#
- 28 PWR\_SW\_KEY#
- 28,29 CAMERA\_K#
- 28 HOTSTART\_K#
- 28 BT\_WLAN\_K#

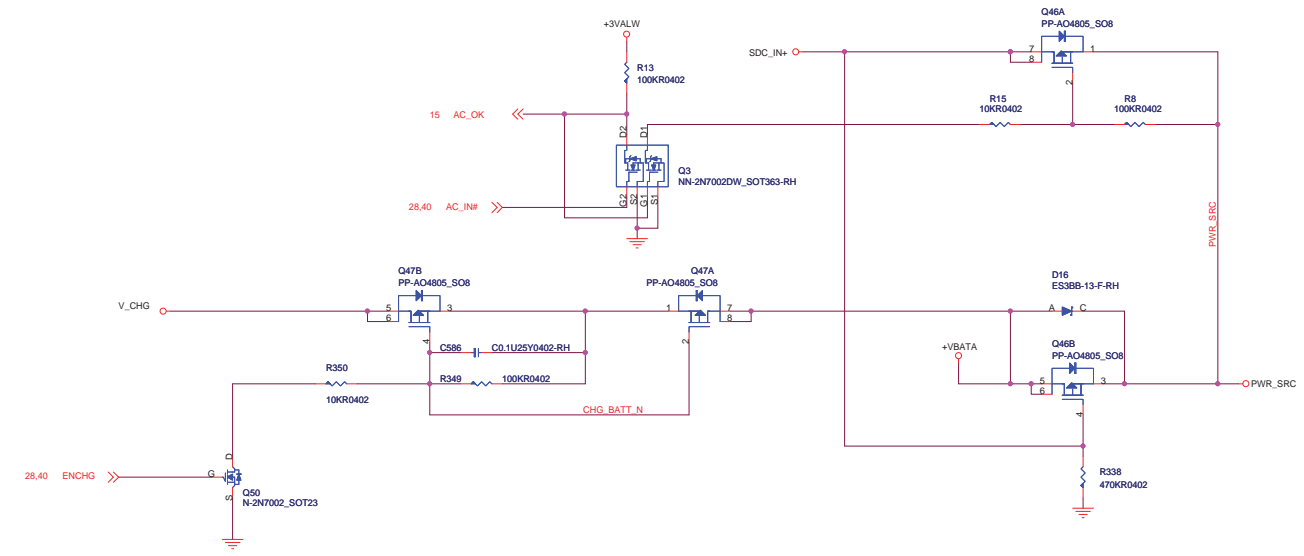


<b>MSI CORPORATION</b>		
Title		
<b>LED &amp; FPC</b>		
Size	Document Number	Rev
B	<b>MS-163A</b>	0A
Date:	Friday, July 06, 2007	Sheet 38 of 54

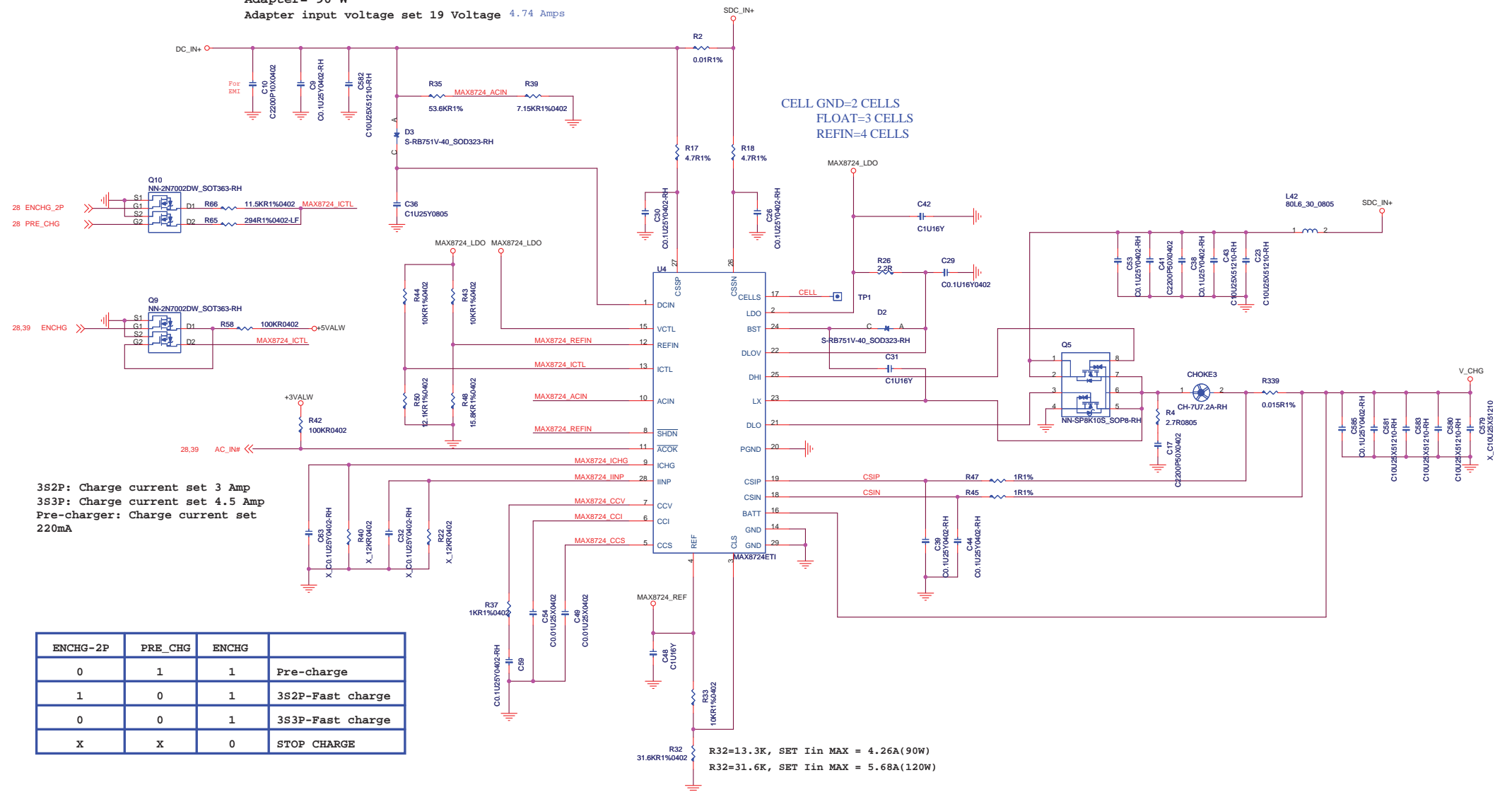


**JBAT1 Pin Definition**

- 1: VBATA+
- 2: VBATA+
- 3: GND
- 4: GND
- 5: SMBCLK
- 6: SMBDATA
- 7: BAT\_IN#
- 8: GND
- 9: GND



Adapter= 120 W  
 Adapter input voltage set 19 Voltage 6.32 Amps  
 Adapter= 90 W  
 Adapter input voltage set 19 Voltage 4.74 Amps



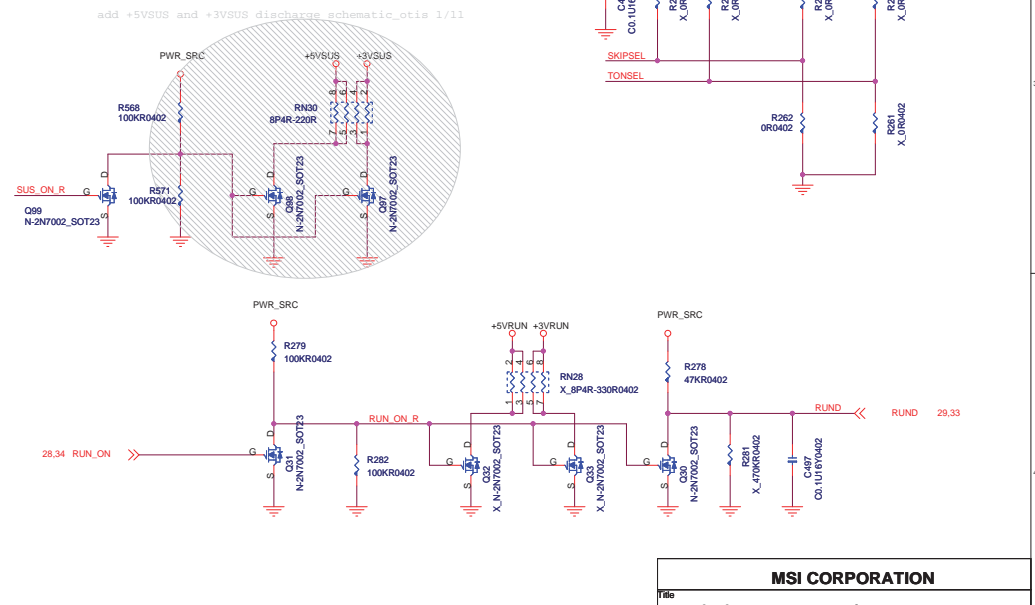
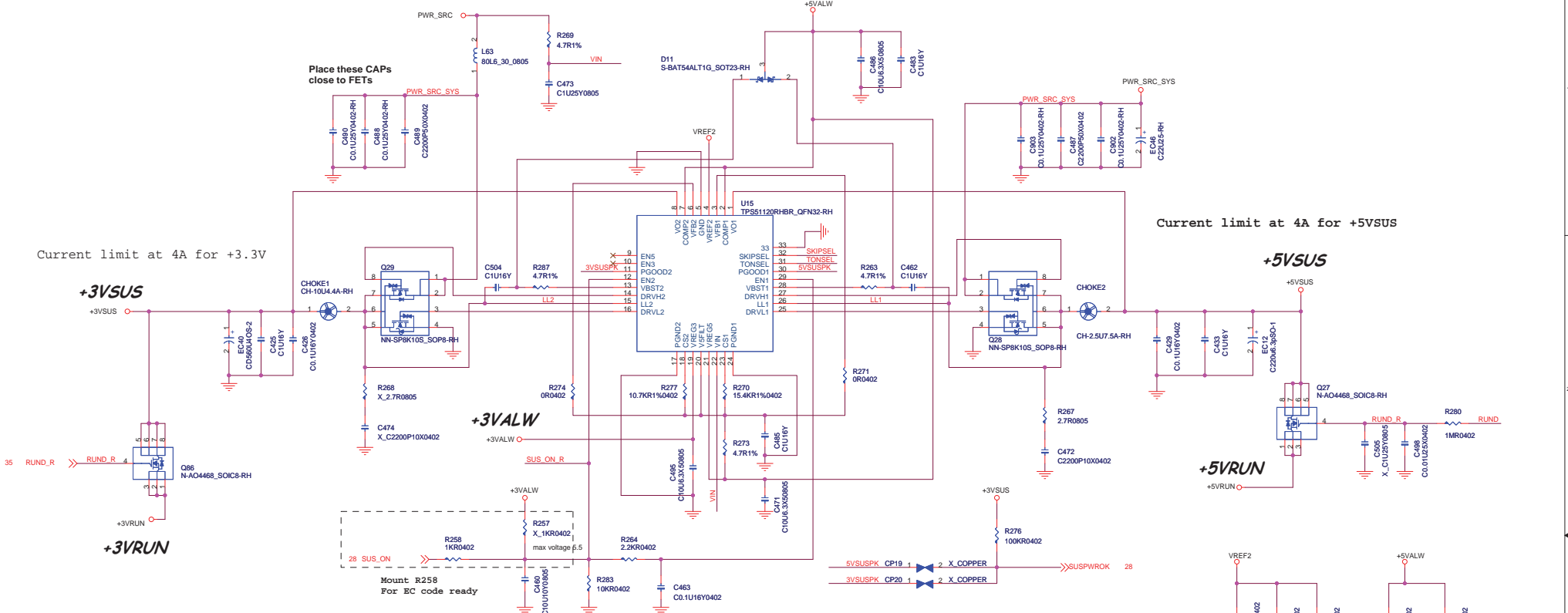
CELL GND=2 CELLS  
 FLOAT=3 CELLS  
 REFIN=4 CELLS

3S2P: Charge current set 3 Amp  
 3S3P: Charge current set 4.5 Amp  
 Pre-charger: Charge current set 220mA

ENCHG-2P	PRE_CHG	ENCHG	
0	1	1	Pre-charge
1	0	1	3S2P-Fast charge
0	0	1	3S3P-Fast charge
X	X	0	STOP CHARGE

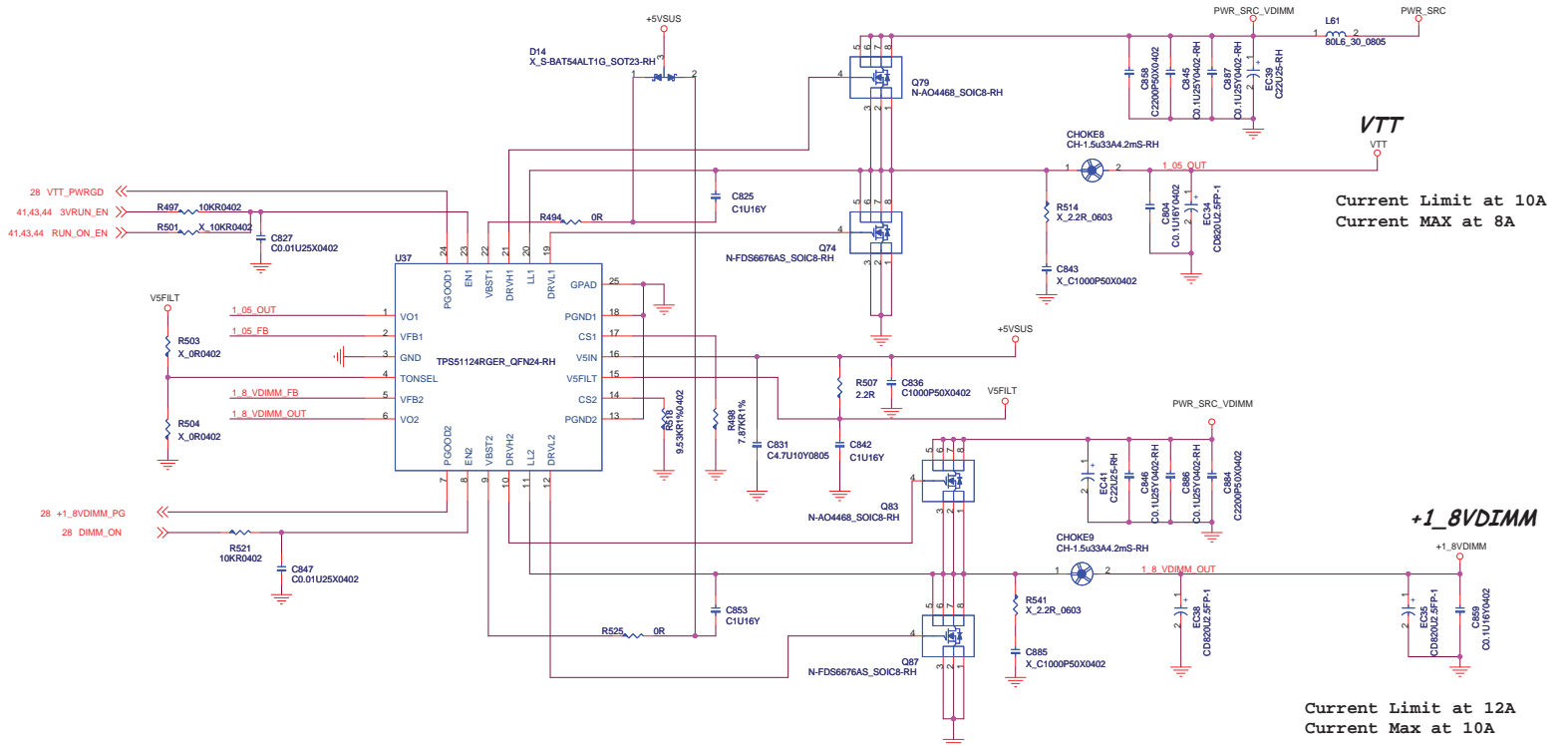
R32=13.3K, SET Iin MAX = 4.26A(90W)  
 R32=31.6K, SET Iin MAX = 5.68A(120W)

**+5VALW**



<b>MSI CORPORATION</b>		
File	SYSTEM POWER 3/5V	
Size	Document Number	Rev
C	MS-163A	0A
Date:	Wednesday, July 11, 2007	Sheet 41 of 54

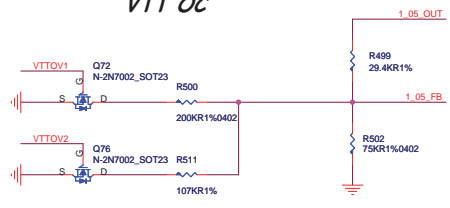




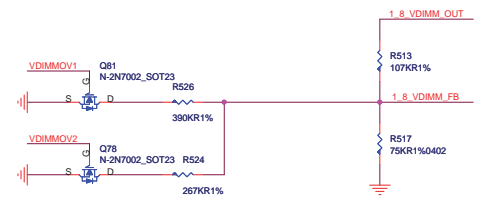
**VTT**  
Current Limit at 10A  
Current MAX at 8A

**+1.8VDIMM**  
Current Limit at 12A  
Current Max at 10A

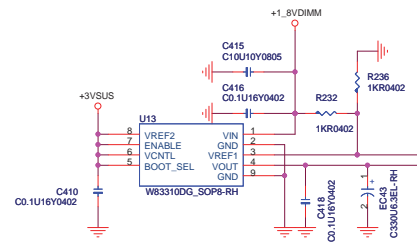
**VTT OC**



**VDIMM OC**



**DDR\_VTT 0.9V**



**VTT OverVoltage TABLE**

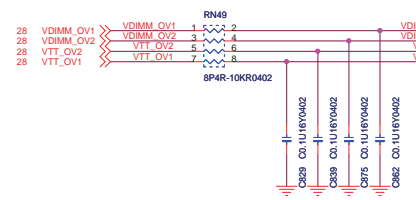
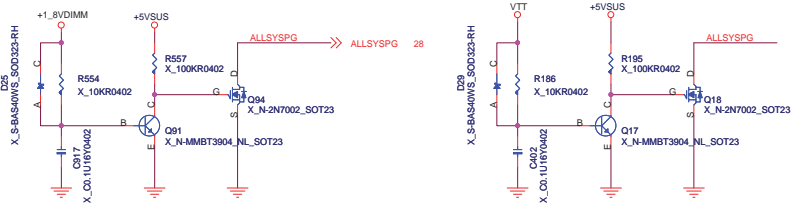
OV1	OV2	VTT OverVoltage
0	0	1.05V(default)
1	0	1.15V
0	1	1.25V

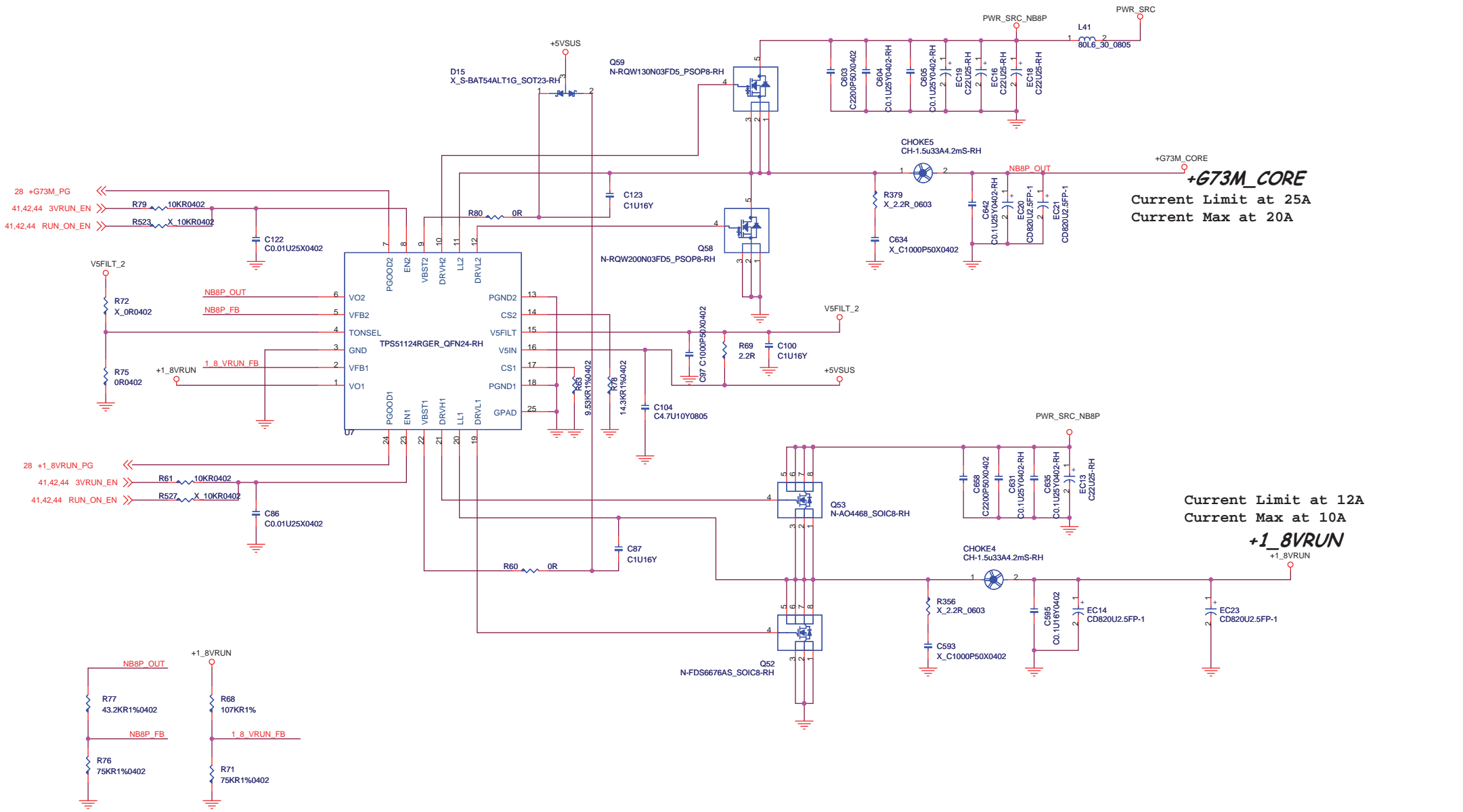
Note:  
1=> HIGH  
0=> LOW

**VDIMM OverVoltage TABLE**

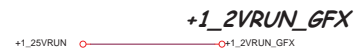
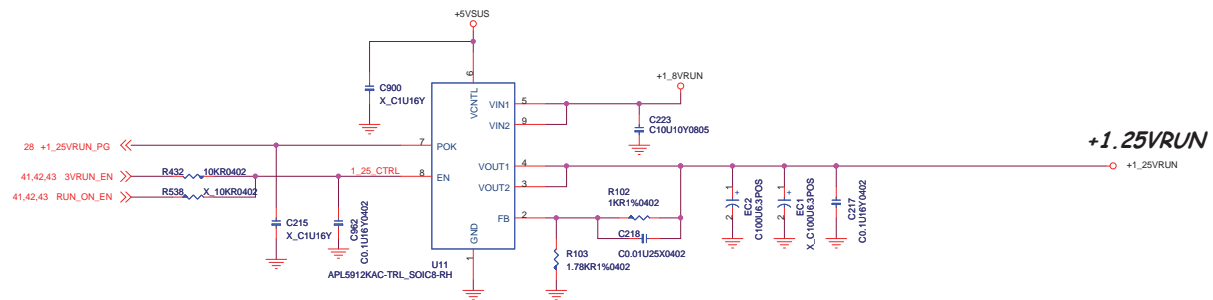
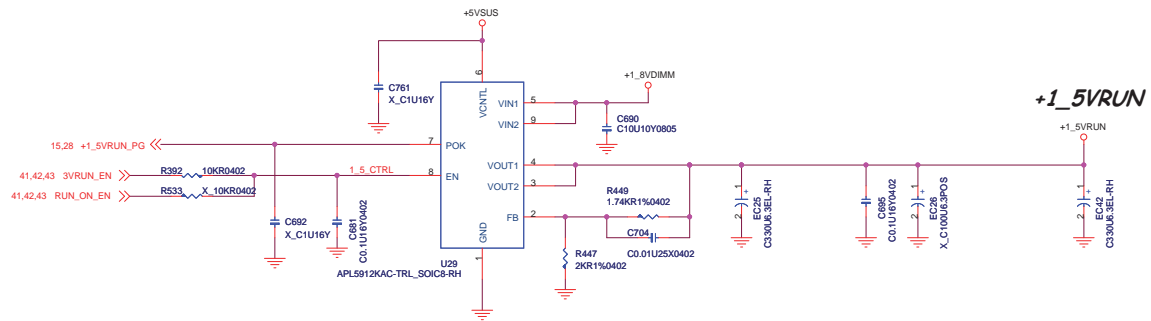
OV1	OV2	VDIMM OverVoltage
0	0	1.85V(default)
1	0	2V
0	1	2.15V

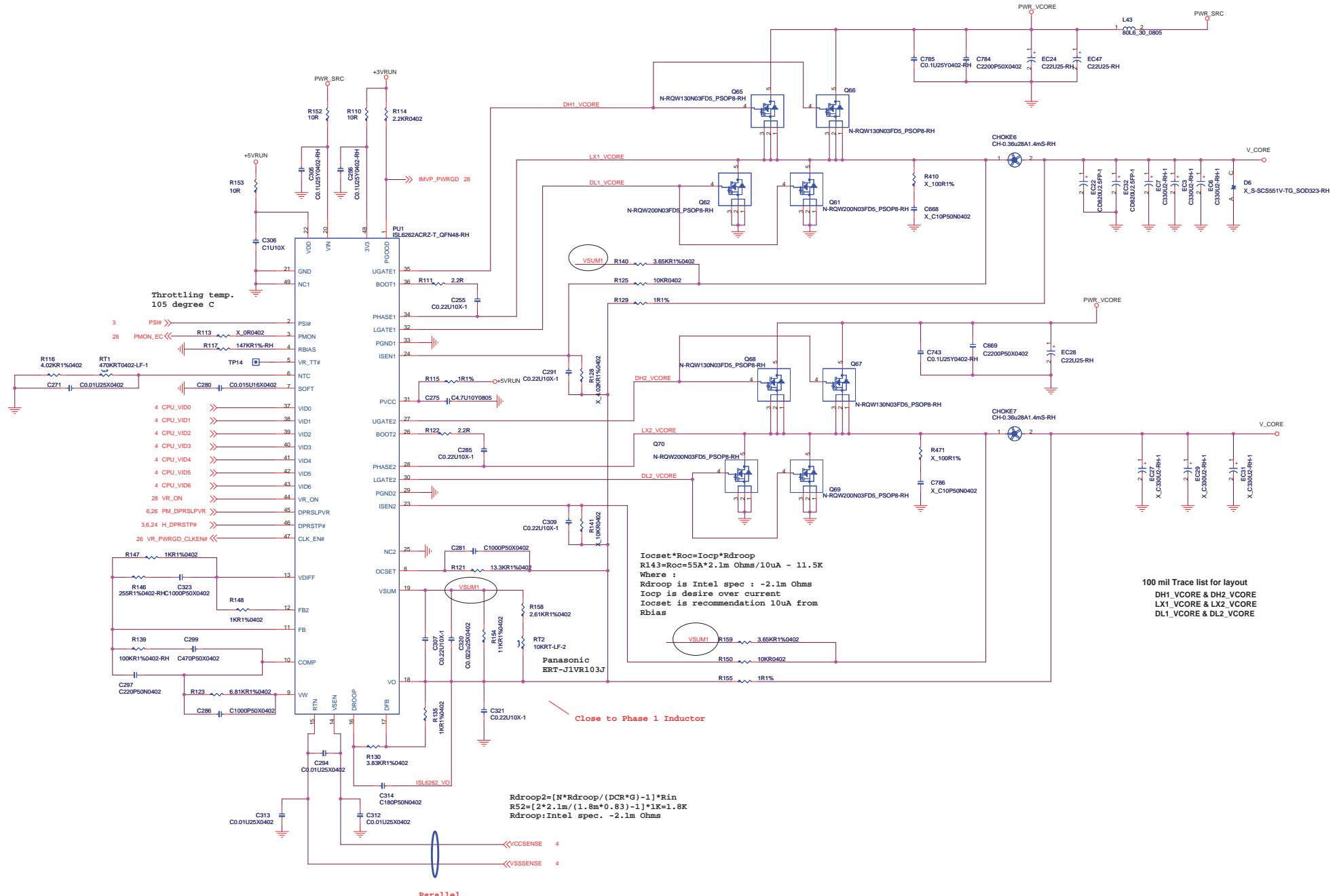
Note:  
1=> HIGH  
0=> LOW





<b>MSI CORPORATION</b>		
Title: <b>+G73M_CORE,1.8VRUN</b>		
Size: Custom	Document Number: <b>MS-163A</b>	Rev: 0A
Date: Wednesday, July 11, 2007	Sheet: 43	of 54





Throttling temp.  
105 degree C

$I_{ocset} \cdot R_{oc} = I_{ocp} \cdot R_{droop}$   
 $R_{143} = R_{oc} = 55A \cdot 2.1m\ \Omega / 10\mu A \sim 11.5K$   
 Where :  
 $R_{droop}$  is Intel spec :  $\sim 2.1m\ \Omega$   
 $I_{ocp}$  is desire over current  
 $I_{ocset}$  is recommendation  $10\mu A$  from Rbias

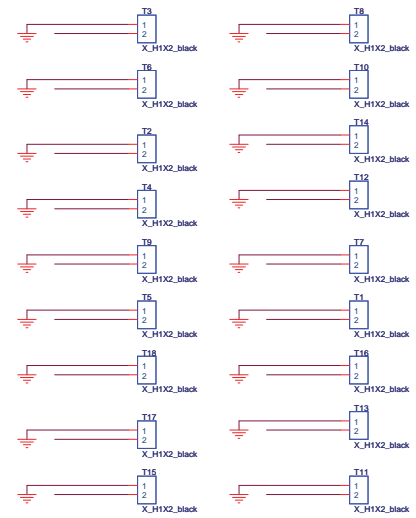
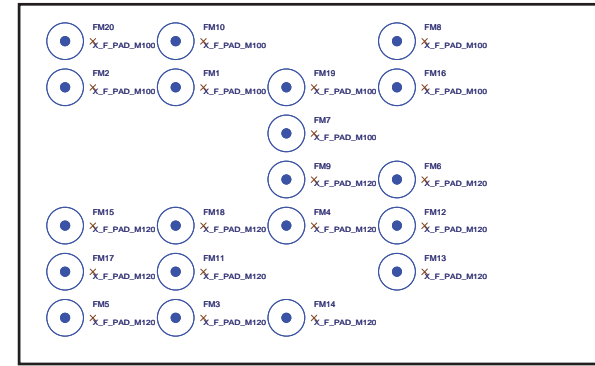
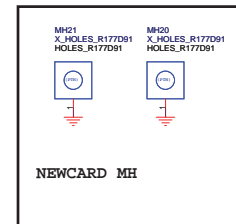
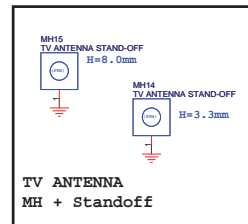
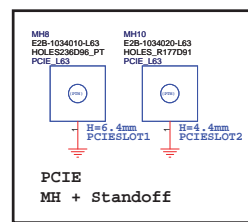
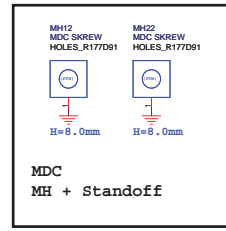
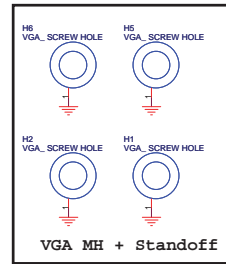
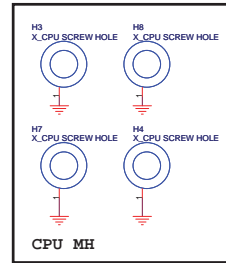
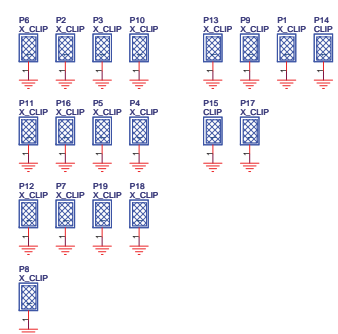
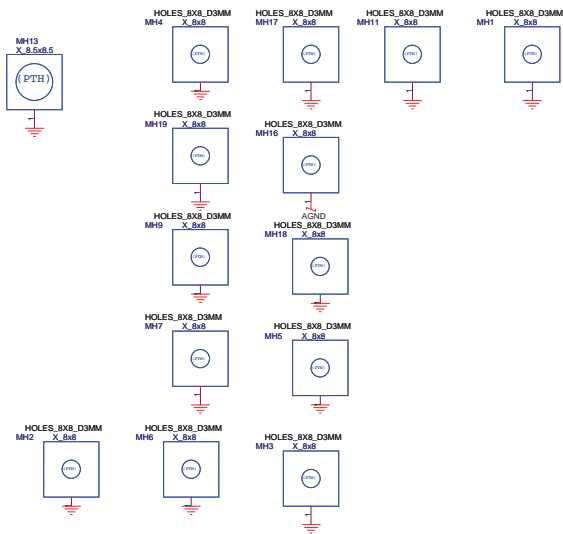
$R_{droop2} = [N \cdot R_{droop} / (DCR \cdot G) - 1] \cdot R_{in}$   
 $R_{52} = [2 \cdot 2.1m / (1.8m \cdot 0.83) - 1] \cdot 1K = 1.8K$   
 $R_{droop}$ : Intel spec.  $\sim 2.1m\ \Omega$

100 mil Trace list for layout  
 DH1\_VCORE & DH2\_VCORE  
 LX1\_VCORE & LX2\_VCORE  
 DL1\_VCORE & DL2\_VCORE

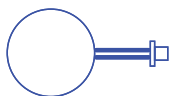
Close to Phase 1 Inductor

Parallel

<b>MSI CORPORATION</b>			
<b>CPU POWER</b>			
File	Document Number	Rev	QA
Size	Custom	MS-163A	
Date: Wednesday, Jun 11, 2007	Sheet	45	of 54



JBAT2



BAT-CR2032

JMDC1\_1  
X\_MODEM\_CARD



MDC改為機構料

PCB1



P30-163A110-D05

FOR MDC

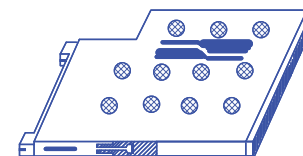


X\_SCREW\_M4.5X2X3 mm



X\_SCREW\_M4.5X2X3 mm

JPE1\_1  
NEW\_CARD



另加上PCI  
EXPRESS 鐵件:  
E2M-6310711-SH4

FOR NEWCARD



SCREW\_M4.5X2X3 mm



SCREW\_M4.5X2X3 mm

FOR PCIE



SCREW\_M4.5X2X3 mm



SCREW\_M4.5X2X3 mm

FOR TV ANTENNA



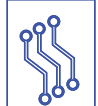
SCREW\_M4.5X2X3 mm

RUB1



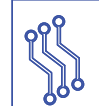
rubber

JPE1\_4



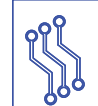
NEW\_CARD\_MYLAR

Y4\_1



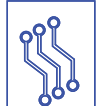
TOP SIZE Y4\_MYLAR

JACK1\_1



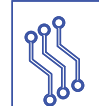
TOP SIZE LINE OUT\_MYLAR

U9\_3



MDC\_BACK\_MYLAR

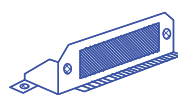
J2\_1



CARDREADER\_MYLAR

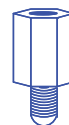
FOR D-SUB

JVGA1\_1



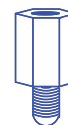
CRT SHIELDING  
E2M-6312511-Y28

JVGA1\_2



SCREW\_4.75X4.9 mm

JVGA1\_3



SCREW\_4.75X4.9 mm

MSI CORPORATION

Title

Manual Part

Size  
B

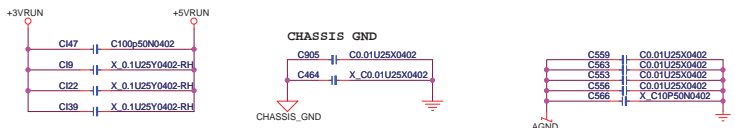
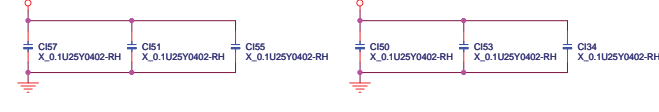
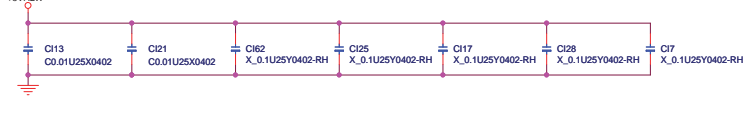
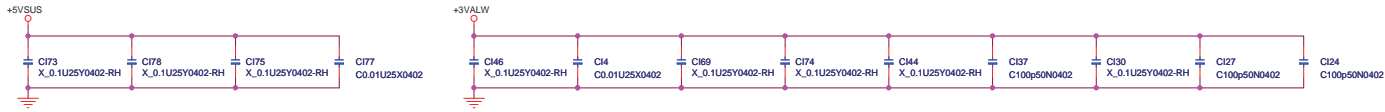
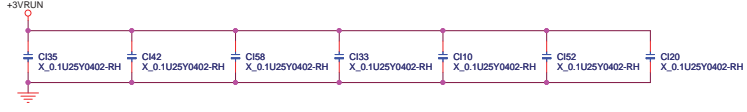
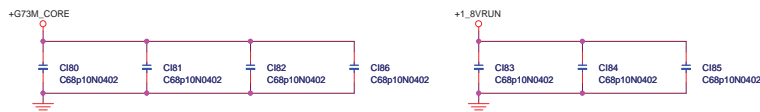
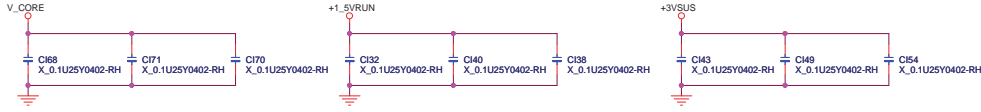
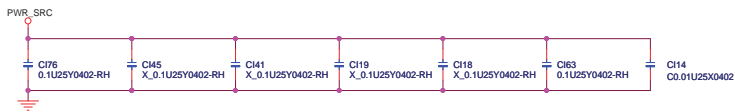
Document Number

MS-163A

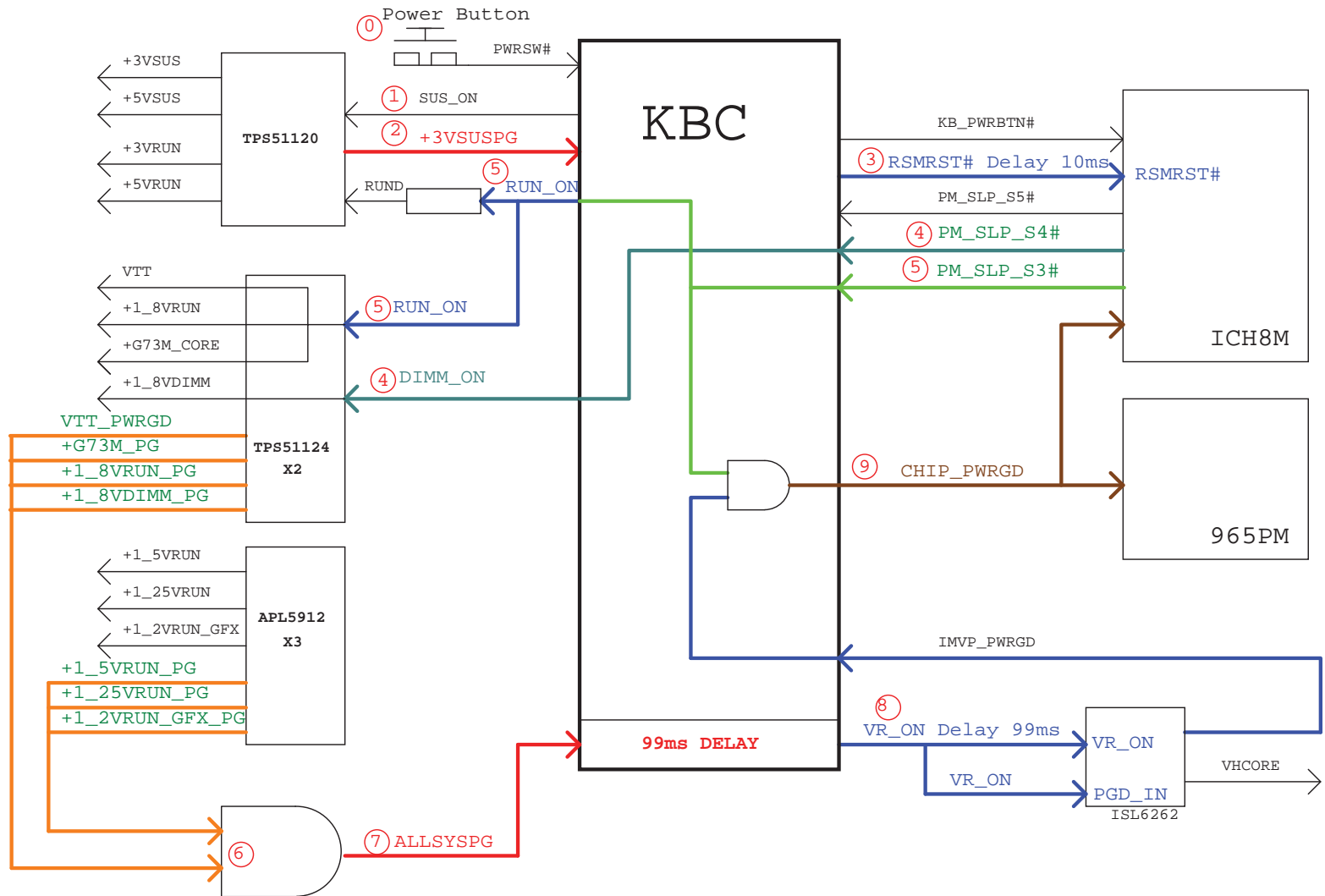
Rev  
0A

Date: Tuesday, July 10, 2007

Sheet 47 of 54



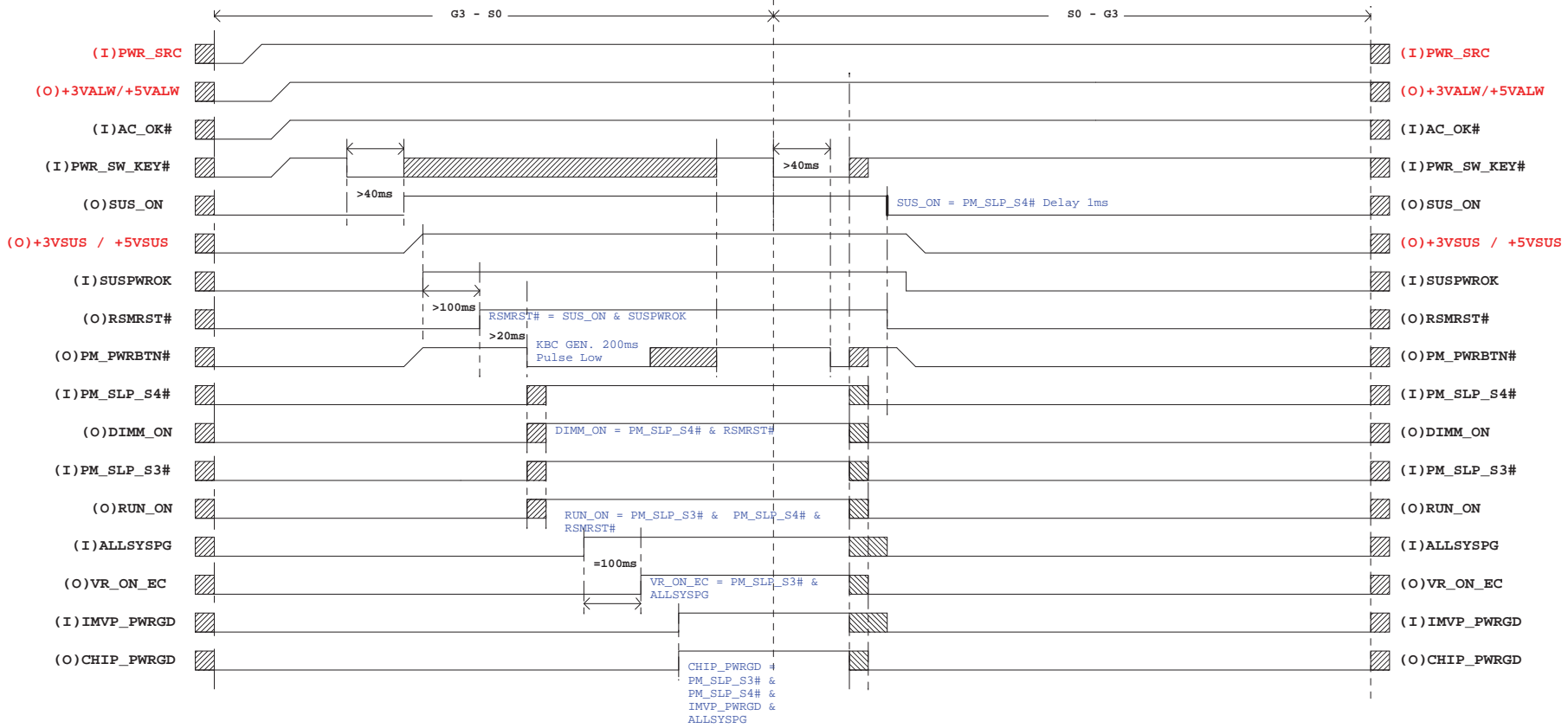




<b>MSI CORPORATION</b>		
Title		
<b>KBC_CTR_PWR</b>		
Size	Document Number	Rev
B	<b>MS-163A</b>	0A
Date:	Monday, May 07, 2007	Sheet 49 of 54

RED: POWER  
BLACK: KBC

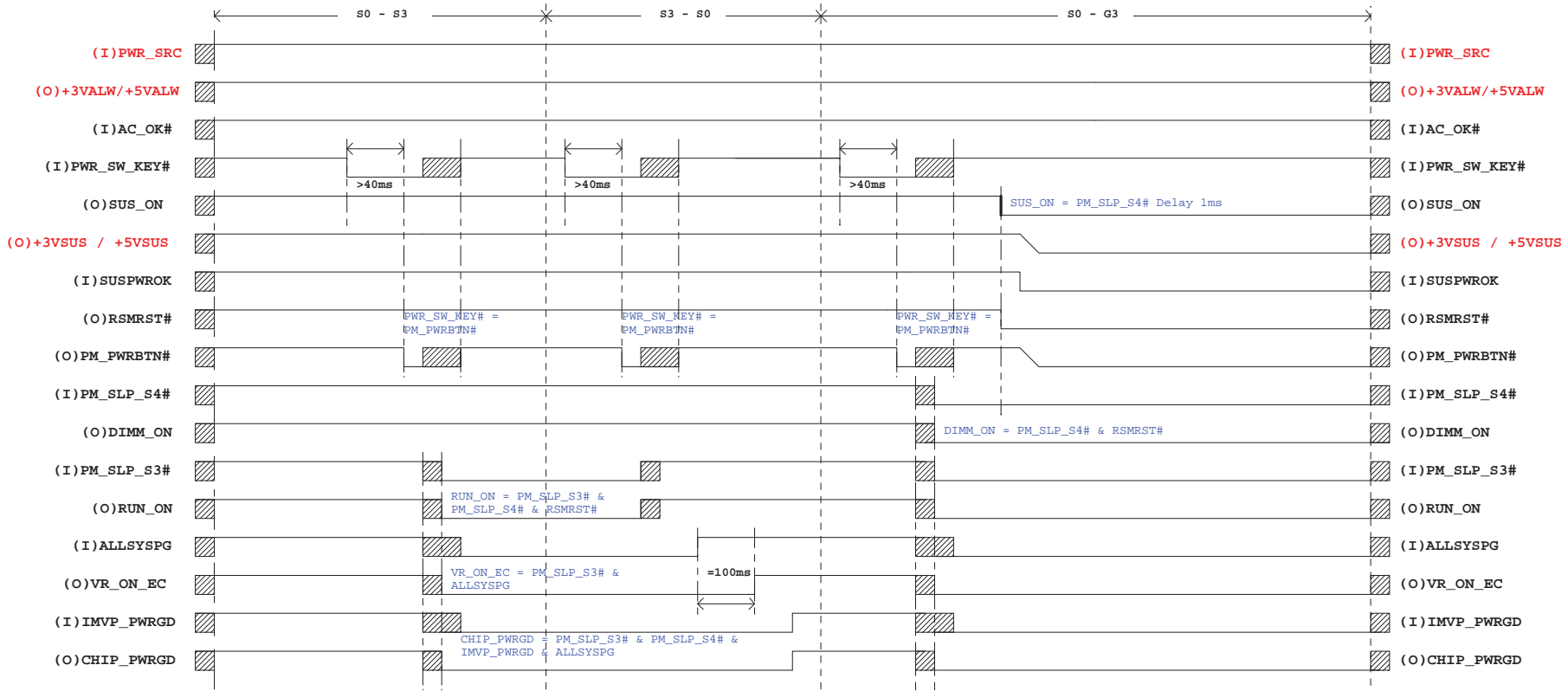
Battery Mode G3 - S0 - G3



<b>MSI CORPORATION</b>			
<b>AC/Battery timing 1</b>			
File			
Size	Document Number	Rev	
Custom	<b>MS-163A</b>	0A	
Date:	Monday, May 07, 2007	Sheet	50 of 54

RED: POWER  
BLACK: KBC

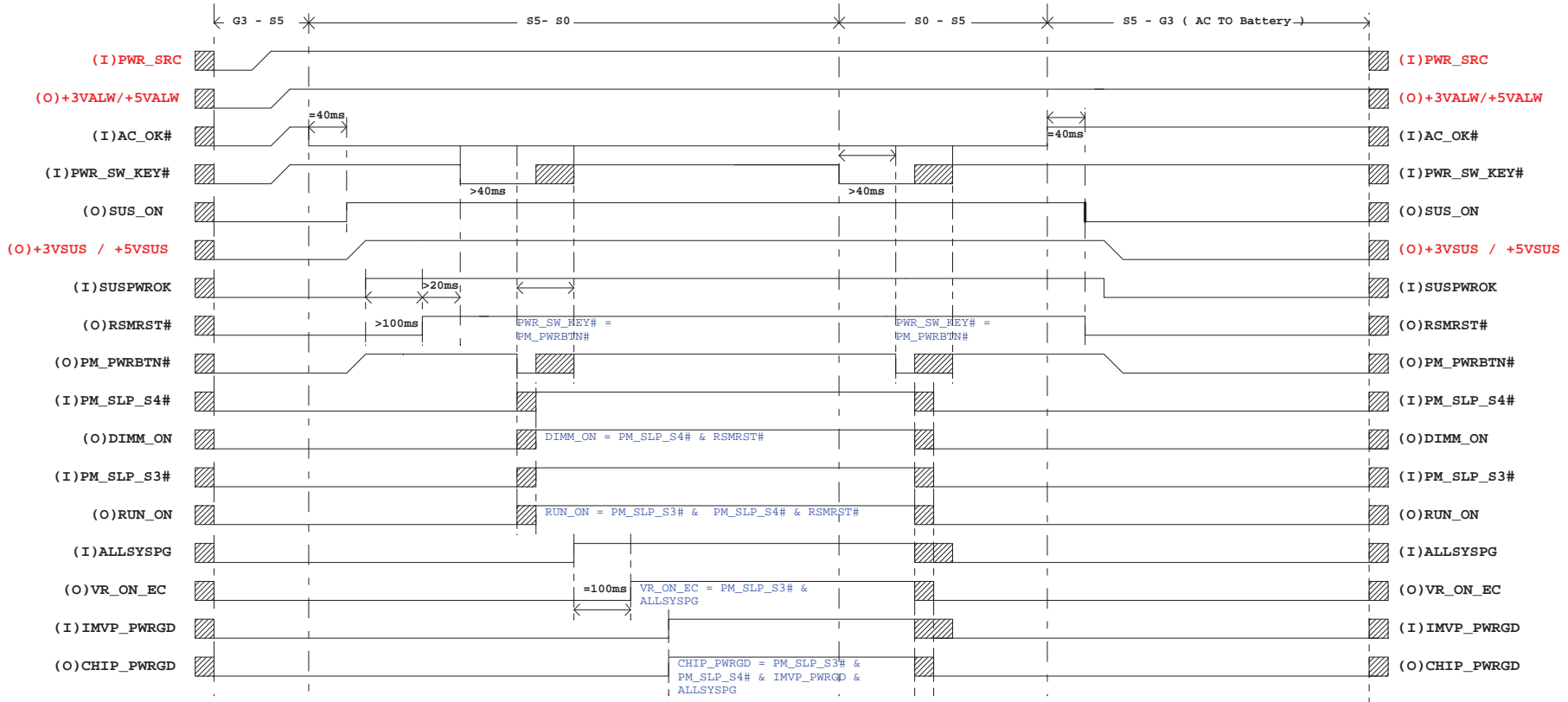
Battery Mode S0 - S3 - S0



<b>MSI CORPORATION</b>			
<b>AC/Battery timing 2</b>			
File			
Size	Document Number	Rev	
Custom	<b>MS-163A</b>	0A	
Date:	Monday, May 07, 2007	Sheet	51 of 54

RED: POWER  
BLACK: KBC

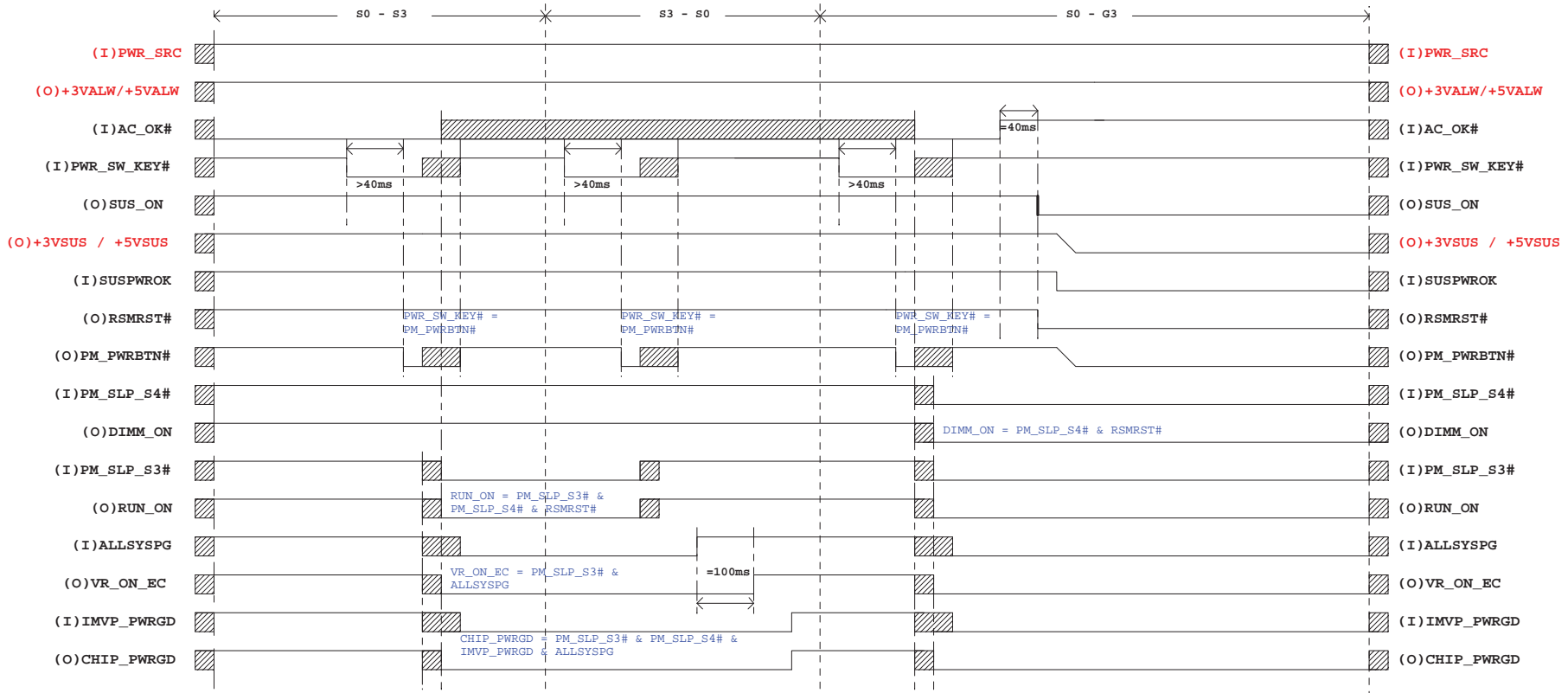
AC Mode G3 - S5 - S0 - S5 - G3



<b>MSI CORPORATION</b>			
File: <b>AC/Battery timing 3</b>			
Size: Custom	Document Number: <b>MS-163A</b>	Rev: 0C	
Date: Monday, May 07, 2007	Sheet: 52 of 54		

RED: POWER  
BLACK: KBC

AC Mode S0 - S3 - S0



<b>MSI CORPORATION</b>			
<b>AC/Battery timing 4</b>			
File			
Size	Document Number	Rev	
Custom	<b>MS-163A</b>	0A	
Date:	Monday, May 07, 2007	Sheet	53 of 54

[www.s-manuals.com](http://www.s-manuals.com)