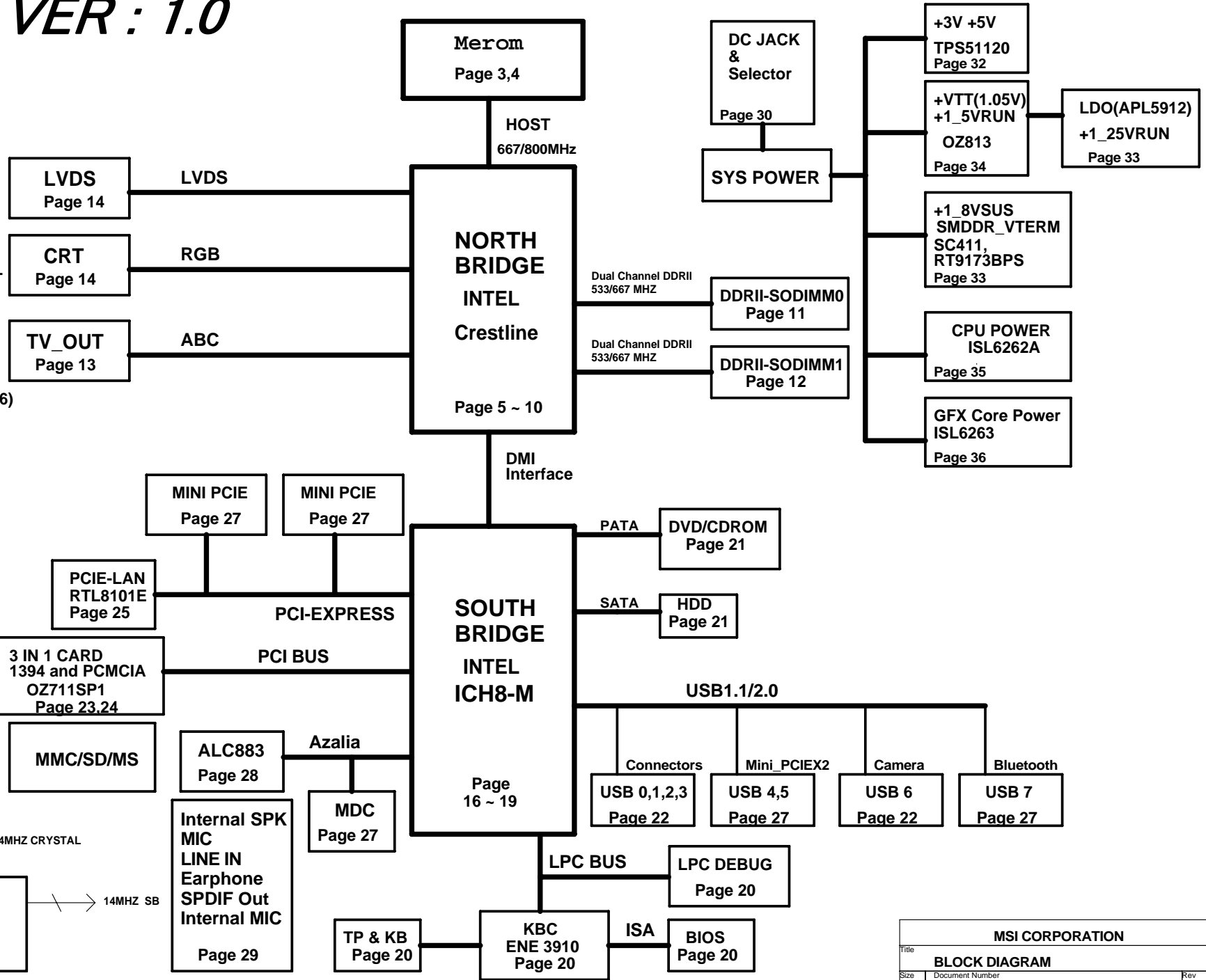


# MS-16371 VER : 1.0

- 01 : BLOCK DIAGRAM
- 02 : PLATFORM
- 03 : Merom-1 (HOST BUS)
- 04 : Merom-2 (POWER/GND)
- 05 : CRESTLINE-1 (HOST BUS)
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- 11 : DDR2\_SODIMM0
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- 13 : DDR2 TREMINATION&TV\_OUT
- 14 : CRT & LVDS
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- 16 : ICH8M-1 (CPU/IDE/Azalia)
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- 18 : ICH8M-3 (SM BUS/GPIO)
- 19 : ICH8M-4 (POWER/GND)
- 20 : KBC/EC/uP (ENE3910-LFQP176)
- 21 : HDD & ODD
- 22 : USB & CMOS
- 23 : OZ711SP1 (PCI Bus/1394)
- 24 : OZ711SP1-2 (PCMCIA&CARD)
- 25 : PCIE LAN (RTL8111B)
- 26 : FAN & LED & SW & PWRGD
- 27 : MINI PCIE & MDC & BT
- 28 : CODEC(ALC888) & Amp
- 29 : Audio Jacks
- 30 : M\_Battery select
- 31 : M\_Battery Charger
- 32 : M\_System Power
- 33 : DDR2 RAM POWER, +1.25V
- 34 : M\_VTT, +1.5V
- 35 : M\_CPU power
- 36 : M\_Graphics Core
- 37 : Screw
- 38 : EMI
- 39 : Power on Sequence
- 40 : Power on Sequence
- 41 : TP Board
- 42 : Launch Board



<b>MSI CORPORATION</b>		
Title <b>BLOCK DIAGRAM</b>		
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## Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
VHORE	Core Voltage for Processor	VR_ON
+VTT	1.05 rail for Processor & 965GM I/O	PM_SLP_S3# ( RUN_ON )
+1_5VRUN	1.5V switched power rail(off in S3-S5)	PM_SLP_S3# ( RUN_ON )
+1_25VRUN	1.25V powe rail NB PLL and PXE (off in S3-S5)	+1_5VRUN
+3VRUN	3.3V switched power rail(off in S3-S5)	RUND ( RUN_ON )
+5VRUN	5.0V switched power rail(off in S3-S5)	RUND (RUN_ON )
SMDDR_VTERM	0.9V DDR Termination voltage (off in S4-S5)	PM_SLP_S3# ( RUN_ON )
+1_8VDIMM	1.8V power rail DDR (off in S4-S5)	PM_SLP_S4# ( DIMM_ON )
+3VSUS	3.3V power rail (off in S4-S5)	SUS_ON
+5VSUS	5.0V power rail (off in S4-S5)	SUS_ON
+3VALW	3.3V always on power rail	PWR_SRC
+5VALW	5.0V always on power rail	PWR_SRC
+V5_AUDIO	5.0V Power rail Audio codec(off in S3-S5)	RUND
VTT_G	Core Voltage for GMCH GPU	GFX_VR_EN

System Power consumption	
CPU Vcore	40W
3V	15W
5V	25W
Graphics Vcore	10W
1.5V	7W
1.05V	10W
PWR_SRC	107W(12A)

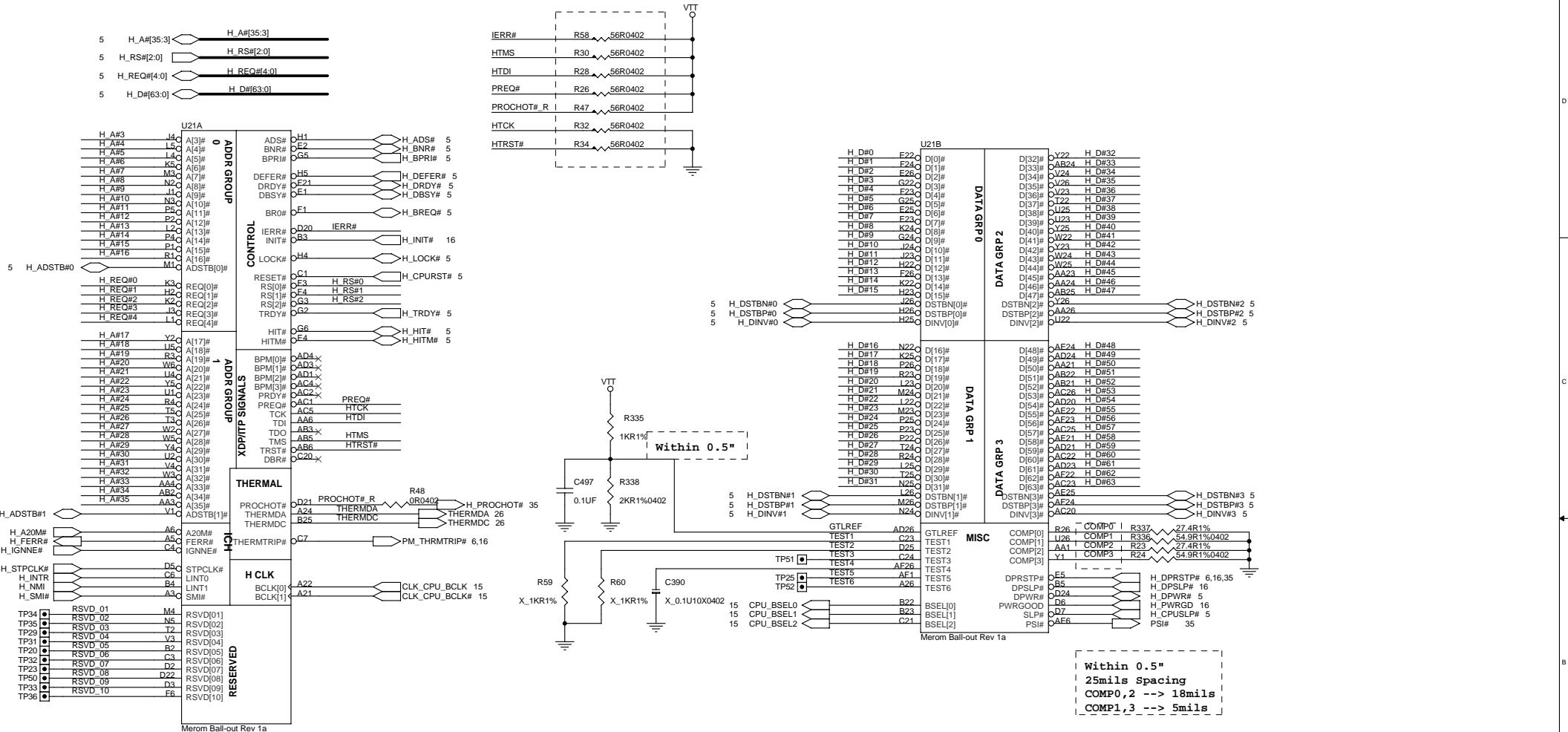
## POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+V*SUS	+V*RUN	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3( Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4( Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on then +V\*SUS will always keep high

MSI CORPORATION

Title			PLATFORM		
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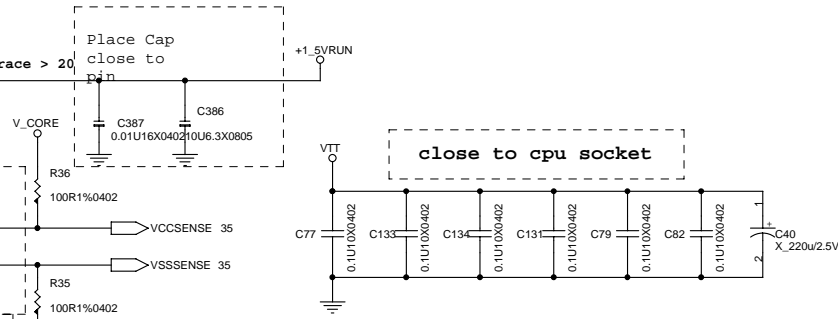
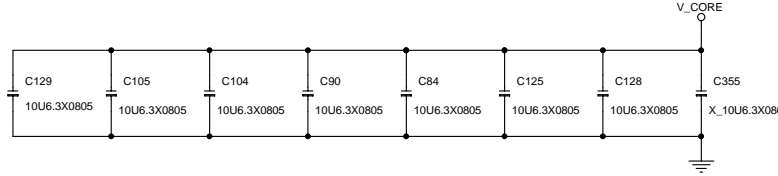
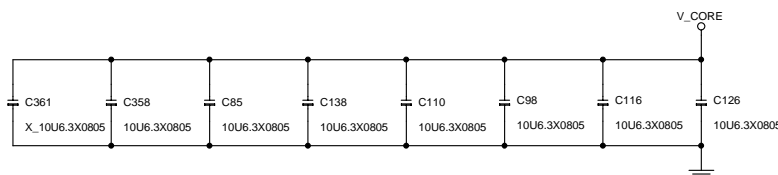
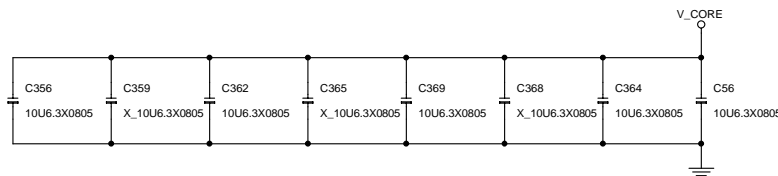
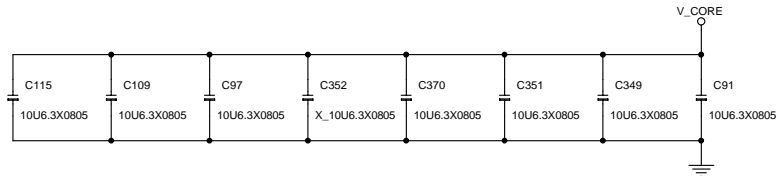
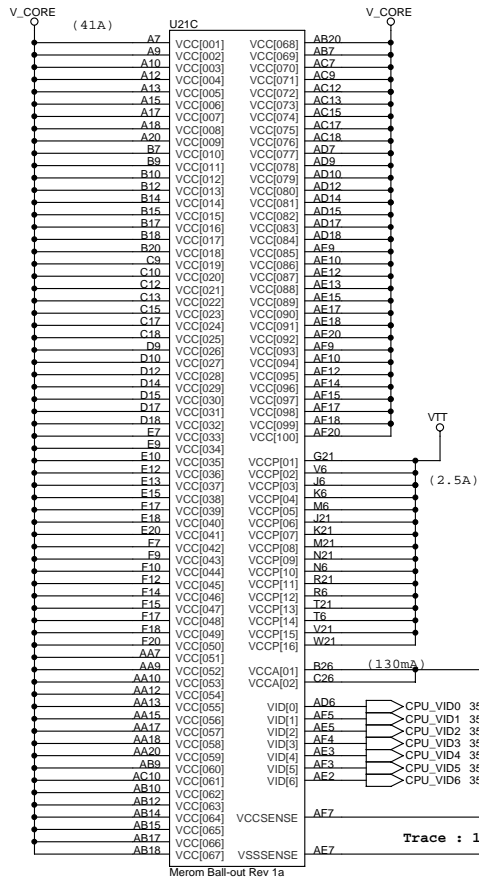
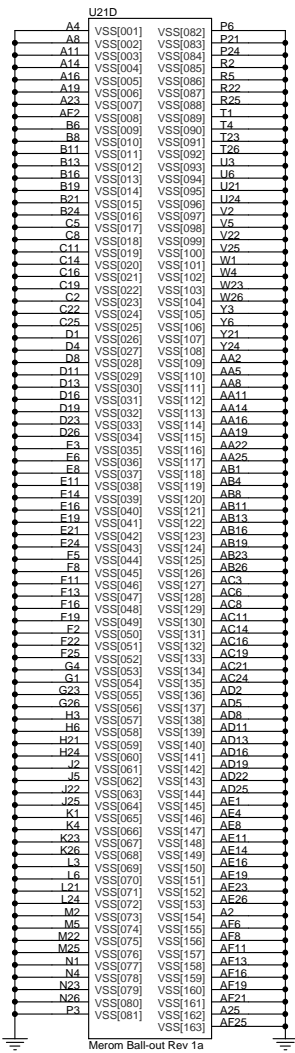


Within 0.5"  
 25mils Spacing  
 COMP0,2 ---> 18mils  
 COMP1,3 ---> 5mils

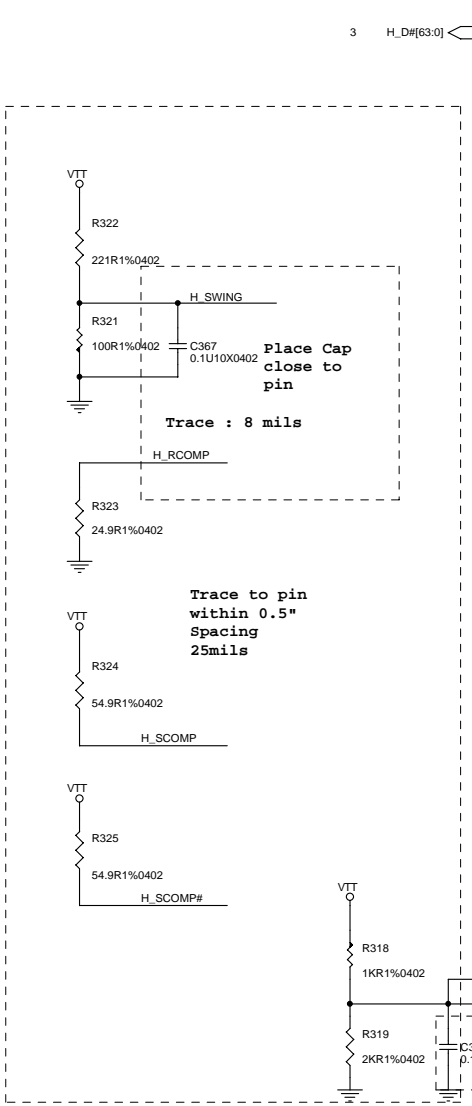
Merom Ball-out Rev 1a

Merom Ball-out Rev 1a

<b>MSI CORPORATION</b>		
Title <b>Merom-1 (HOST BUS)</b>		
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Trace width = 18mils  
Trace spacing = 7mils  
other spacing = 50mils  
length matched within 25mils  
Place R close to CPU within



U20A

H_D#0	E2	H_D# 0
H_D#1	G2	H_D# 1
H_D#2	G7	H_D# 2
H_D#3	M6	H_D# 3
H_D#4	H7	H_D# 4
H_D#5	H3	H_D# 5
H_D#6	G4	H_D# 6
H_D#7	F3	H_D# 7
H_D#8	N8	H_D# 8
H_D#9	H2	H_D# 9
H_D#10	M10	H_D# 10
H_D#11	N12	H_D# 11
H_D#12	N9	H_D# 12
H_D#13	H5	H_D# 13
H_D#14	P13	H_D# 14
H_D#15	K9	H_D# 15
H_D#16	M2	H_D# 16
H_D#17	W10	H_D# 17
H_D#18	Y8	H_D# 18
H_D#19	V4	H_D# 19
H_D#20	M3	H_D# 20
H_D#21	J1	H_D# 21
H_D#22	N6	H_D# 22
H_D#23	N3	H_D# 23
H_D#24	W6	H_D# 24
H_D#25	W9	H_D# 25
H_D#26	N2	H_D# 26
H_D#27	Y7	H_D# 27
H_D#28	V9	H_D# 28
H_D#29	P4	H_D# 29
H_D#30	W3	H_D# 30
H_D#31	N1	H_D# 31
H_D#32	AD12	H_D# 32
H_D#33	AE3	H_D# 33
H_D#34	AD9	H_D# 34
H_D#35	AC9	H_D# 35
H_D#36	AC7	H_D# 36
H_D#37	AC14	H_D# 37
H_D#38	AD11	H_D# 38
H_D#39	AC11	H_D# 39
H_D#40	AB2	H_D# 40
H_D#41	W6	H_D# 41
H_D#42	AB1	H_D# 42
H_D#43	Y3	H_D# 43
H_D#44	AC6	H_D# 44
H_D#45	AE2	H_D# 45
H_D#46	AC3	H_D# 46
H_D#47	P4	H_D# 47
H_D#48	AJ9	H_D# 48
H_D#49	AH8	H_D# 49
H_D#50	AJ14	H_D# 50
H_D#51	AE9	H_D# 51
H_D#52	AE11	H_D# 52
H_D#53	AH12	H_D# 53
H_D#54	AJ5	H_D# 54
H_D#55	AH5	H_D# 55
H_D#56	AJ8	H_D# 56
H_D#57	AE7	H_D# 57
H_D#58	AJ7	H_D# 58
H_D#59	AJ2	H_D# 59
H_D#60	AE5	H_D# 60
H_D#61	AJ3	H_D# 61
H_D#62	AH2	H_D# 62
H_D#63	AH13	H_D# 63

HOST

H_A# 3	J13	H_A#3
H_A# 4	B11	H_A#4
H_A# 5	C11	H_A#5
H_A# 6	M11	H_A#6
H_A# 7	C15	H_A#7
H_A# 8	E16	H_A#8
H_A# 9	L13	H_A#9
H_A# 10	G17	H_A#10
H_A# 11	C14	H_A#11
H_A# 12	K16	H_A#12
H_A# 13	B13	H_A#13
H_A# 14	L16	H_A#14
H_A# 15	L17	H_A#15
H_A# 16	E14	H_A#16
H_A# 17	K19	H_A#17
H_A# 18	P15	H_A#18
H_A# 19	R17	H_A#19
H_A# 20	B16	H_A#20
H_A# 21	H20	H_A#21
H_A# 22	L19	H_A#22
H_A# 23	D17	H_A#23
H_A# 24	M17	H_A#24
H_A# 25	N16	H_A#25
H_A# 26	J19	H_A#26
H_A# 27	B18	H_A#27
H_A# 28	E19	H_A#28
H_A# 29	B17	H_A#29
H_A# 30	B15	H_A#30
H_A# 31	E17	H_A#31
H_A# 32	C18	H_A#32
H_A# 33	A19	H_A#33
H_A# 34	B19	H_A#34
H_A# 35	N19	H_A#35

H_ADS#	G12	H_ADS# 3
H_ADSTB# 0	H17	H_ADSTB#0 3
H_ADSTB# 1	G20	H_ADSTB#1 3
H_BNR#	C8	H_BNR# 3
H_BPRI#	ER	H_BPRI# 3
H_BREQ#	E12	H_BREQ# 3
H_DEFER#	D6	H_DEFER# 3
H_DBSY#	C10	H_DBSY# 3
HPLL_CLK	AM5	CLK_MCH_BCLK# 15
HPLL_CLK#	AM7	CLK_MCH_BCLK# 15
H_DPWR#	H8	H_DPWR# 3
H_DRDY#	K7	H_DRDY# 3
H_HIT#	E4	H_HIT# 3
H_HITM#	C8	H_HITM# 3
H_LOCK#	G10	H_LOCK# 3
H_TRDY#	B7	H_TRDY# 3

H_DIN# 0	K5	H_DIN#0 3
H_DIN# 1	L2	H_DIN#1 3
H_DIN# 2	AD13	H_DIN#2 3
H_DIN# 3	AE13	H_DIN#3 3

H_DSTB# 0	M7	H_DSTB#0 3
H_DSTB# 1	K3	H_DSTB#1 3
H_DSTB# 2	AD2	H_DSTB#2 3
H_DSTB# 3	AH11	H_DSTB#3 3

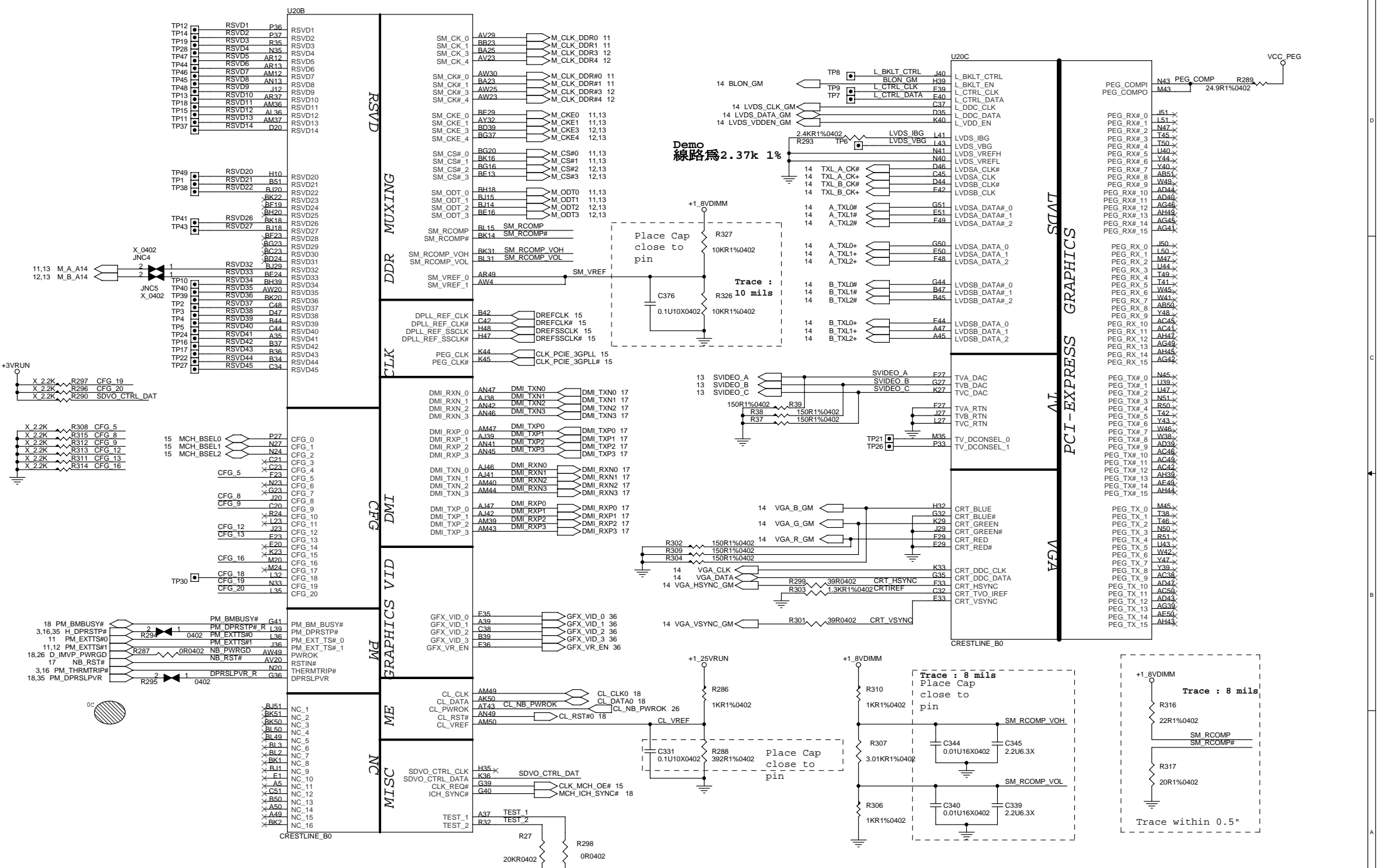
H_DSTBP# 0	L7	H_DSTBP#0 3
H_DSTBP# 1	K2	H_DSTBP#1 3
H_DSTBP# 2	AC2	H_DSTBP#2 3
H_DSTBP# 3	AJ10	H_DSTBP#3 3

H_REQ# 0	M4	H_REQ#0 3
H_REQ# 1	E13	H_REQ#1 3
H_REQ# 2	A11	H_REQ#2 3
H_REQ# 3	H13	H_REQ#3 3
H_REQ# 4	B12	H_REQ#4 3

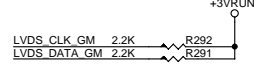
  

H_RS# 0	E12	H_RS#0 3
H_RS# 1	D7	H_RS#1 3
H_RS# 2	D8	H_RS#2 3



**Strapping Configuration**

CFG5 (Default=High)	CFG9 (Default=High)	CFG16 (Default=High)	CFG19 (Default=Low)	CFG20 (Default=Low)	SDVO_CTRL_DATA(Default=Low)
DMI*4==>High DMI*2==>Low	PCIe Graphics Lane: Normal Operation	Dynamic ODT Enabled	DMI Lane Reversal: Normal Operation	Only SDVO or PCIe is operational	SDVO present Low=No SDVO Card Present

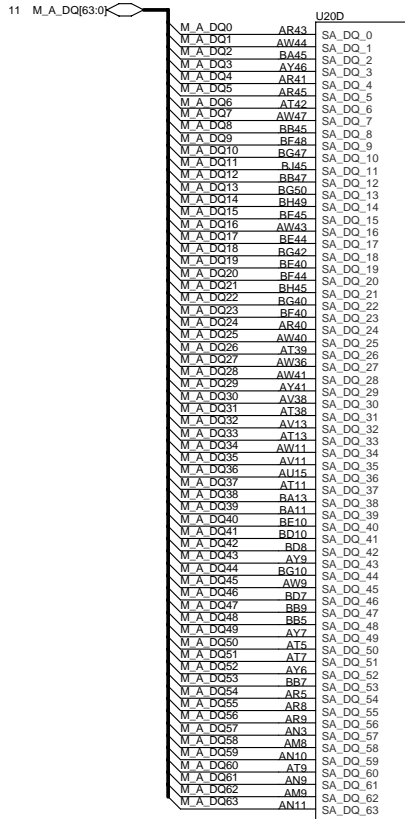


**MSI CORPORATION**

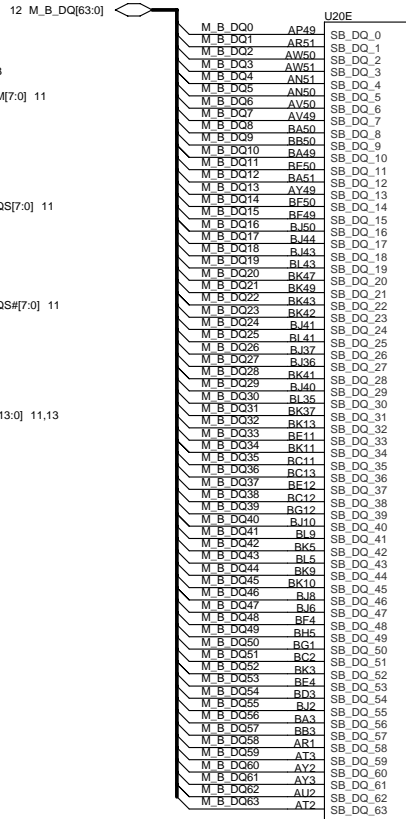
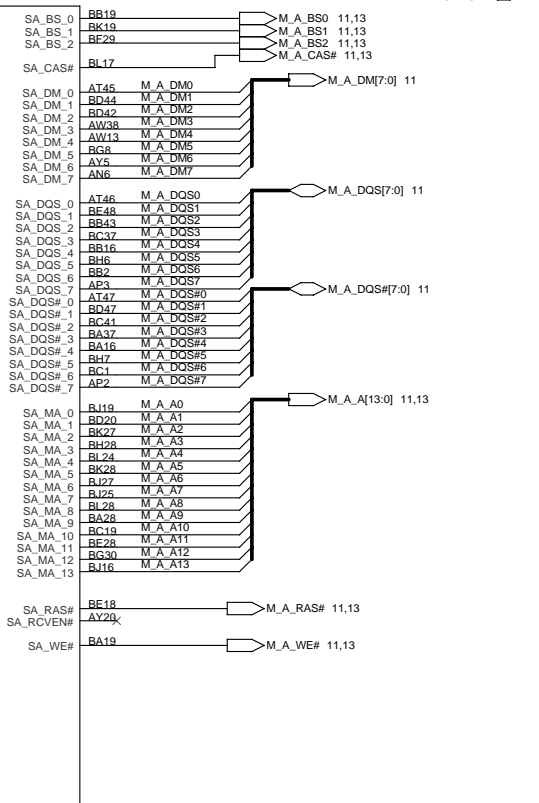
Title: **CRESTLINE-2 (DMI/VGA)**

Size: Document Number  
 Custom: **MS-16371** Rev: 0B

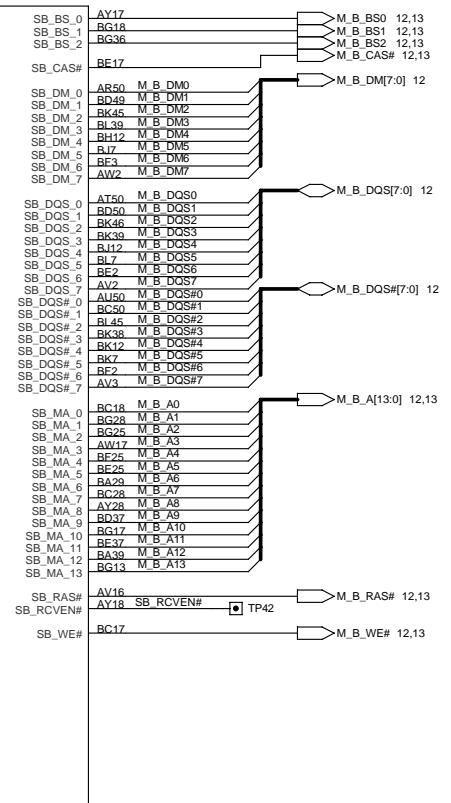
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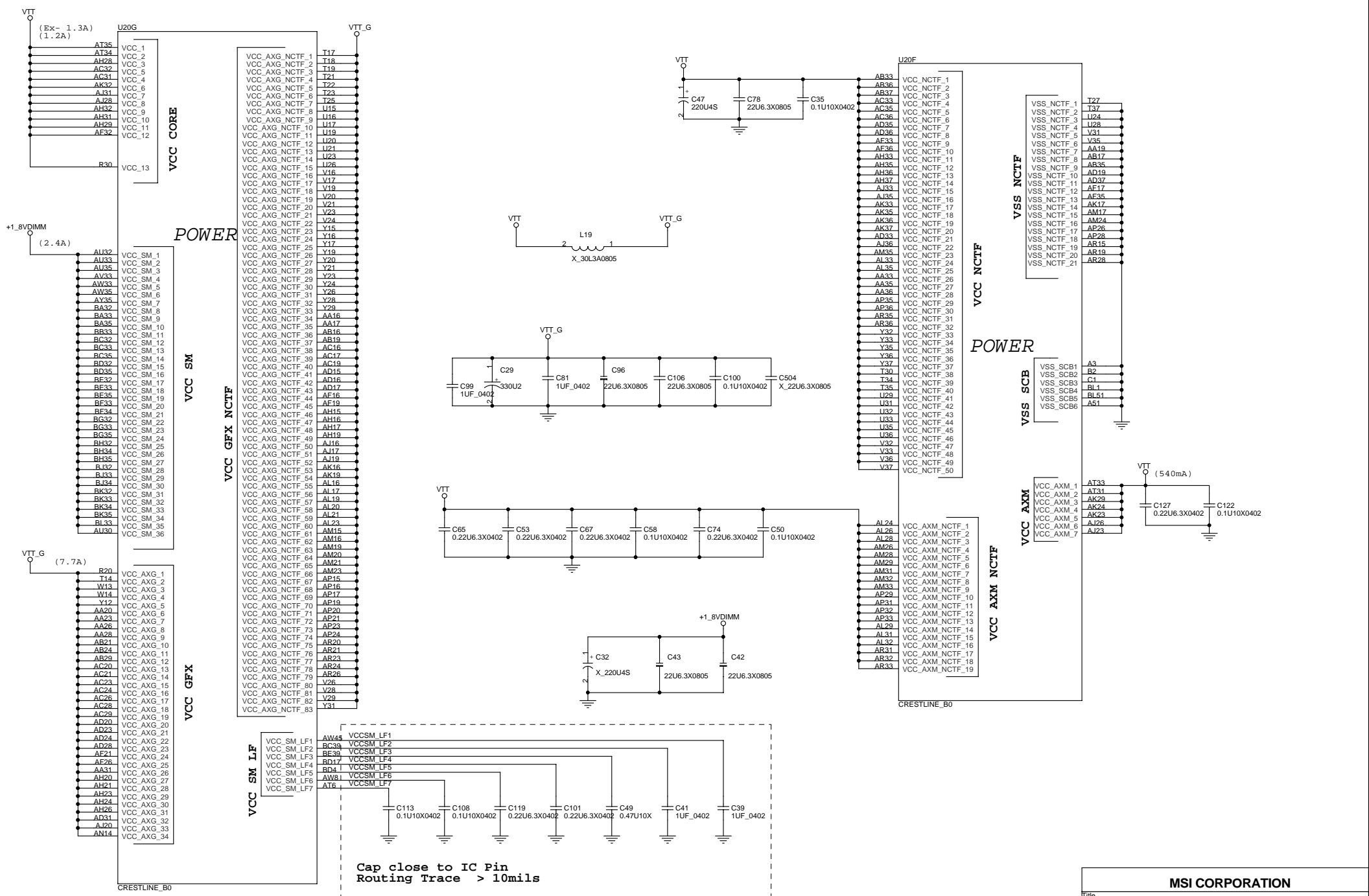
DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B



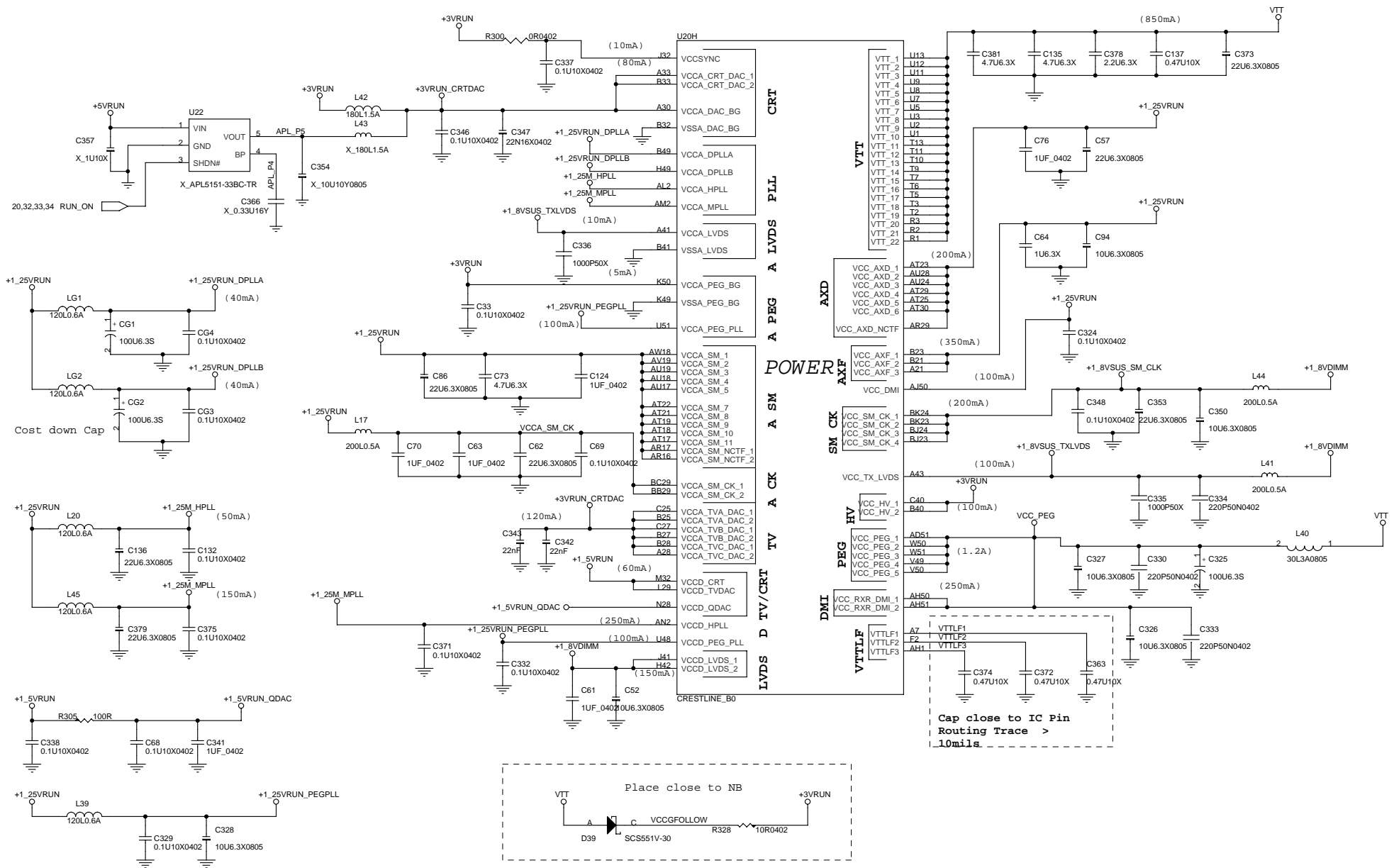
CRESTLINE\_B0



Cap close to IC Pin  
Routing Trace > 10mils

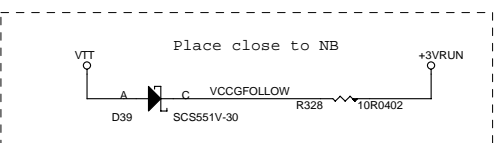
<b>MSI CORPORATION</b>		
<b>CRESTLINE-4 (POWER-1)</b>		
Title	Document Number	Rev
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**POWER**

Cap close to IC Pin  
Routing Trace >  
10mils



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U20I		
A13	VSS_1	VSS_100
A15	VSS_2	VSS_101
A17	VSS_3	VSS_102
A24	VSS_4	VSS_103
AA21	VSS_5	VSS_104
AA24	VSS_6	VSS_105
AA29	VSS_7	VSS_106
AB20	VSS_8	VSS_107
AB23	VSS_9	VSS_108
AB26	VSS_10	VSS_109
AB28	VSS_11	VSS_110
AB31	VSS_12	VSS_111
AC10	VSS_13	VSS_112
AC13	VSS_14	VSS_113
AC3	VSS_15	VSS_114
AC39	VSS_16	VSS_115
AC43	VSS_17	VSS_116
AC47	VSS_18	VSS_117
AD1	VSS_19	VSS_118
AD21	VSS_20	VSS_119
AD26	VSS_21	VSS_120
AD29	VSS_22	VSS_121
AD3	VSS_23	VSS_122
AD41	VSS_24	VSS_123
AD45	VSS_25	VSS_124
AD49	VSS_26	VSS_125
AD5	VSS_27	VSS_126
AD50	VSS_28	VSS_127
AD8	VSS_29	VSS_128
AE10	VSS_30	VSS_129
AE14	VSS_31	VSS_130
AEB	VSS_32	VSS_131
AF20	VSS_33	VSS_132
AF23	VSS_34	VSS_133
AF24	VSS_35	VSS_134
AF31	VSS_36	VSS_135
AG2	VSS_37	VSS_136
AG38	VSS_38	VSS_137
AG43	VSS_39	VSS_138
AG47	VSS_40	VSS_139
AG50	VSS_41	VSS_140
AH3	VSS_42	VSS_141
AH40	VSS_43	VSS_142
AH41	VSS_44	VSS_143
AH7	VSS_45	VSS_144
AH9	VSS_46	VSS_145
AJ11	VSS_47	VSS_146
AJ13	VSS_48	VSS_147
AJ21	VSS_49	VSS_148
AJ24	VSS_50	VSS_149
AJ29	VSS_51	VSS_150
AJ32	VSS_52	VSS_151
AJ43	VSS_53	VSS_152
AJ45	VSS_54	VSS_153
AJ49	VSS_55	VSS_154
AK20	VSS_56	VSS_155
AK21	VSS_57	VSS_156
AK26	VSS_58	VSS_157
AK28	VSS_59	VSS_158
AK31	VSS_60	VSS_159
AK51	VSS_61	VSS_160
AL1	VSS_62	VSS_161
AM11	VSS_63	VSS_162
AM13	VSS_64	VSS_163
AM3	VSS_65	VSS_164
AM4	VSS_66	VSS_165
AM41	VSS_67	VSS_166
AM45	VSS_68	VSS_167
AN1	VSS_69	VSS_168
AN38	VSS_70	VSS_169
AN39	VSS_71	VSS_170
AN43	VSS_72	VSS_171
AN5	VSS_73	VSS_172
AN7	VSS_74	VSS_173
AP4	VSS_75	VSS_174
AP48	VSS_76	VSS_175
AP50	VSS_77	VSS_176
AR11	VSS_78	VSS_177
AR2	VSS_79	VSS_178
AR39	VSS_80	VSS_179
AR44	VSS_81	VSS_180
AR47	VSS_82	VSS_181
AR7	VSS_83	VSS_182
AT10	VSS_84	VSS_183
AT14	VSS_85	VSS_184
AT41	VSS_86	VSS_185
AT49	VSS_87	VSS_186
AU1	VSS_88	VSS_187
AU23	VSS_89	VSS_188
AU29	VSS_90	VSS_189
AU3	VSS_91	VSS_190
AU36	VSS_92	VSS_191
AU49	VSS_93	VSS_192
AU51	VSS_94	VSS_193
AV39	VSS_95	VSS_194
AV48	VSS_96	VSS_195
AW1	VSS_97	VSS_196
AW12	VSS_98	VSS_197
AW16	VSS_99	VSS_198

VSS

CRESTLINE\_B0

U20J		
C46	VSS_199	VSS_287
AW29	VSS_200	VSS_288
C7	VSS_201	VSS_289
AW5	VSS_202	VSS_290
D13	VSS_203	VSS_291
D24	VSS_204	VSS_292
D3	VSS_205	VSS_293
AY24	VSS_206	VSS_294
D39	VSS_207	VSS_295
D45	VSS_208	VSS_296
D49	VSS_209	VSS_297
E10	VSS_210	VSS_298
AY47	VSS_211	VSS_299
AY50	VSS_212	VSS_300
B10	VSS_213	VSS_301
F20	VSS_214	VSS_302
F32	VSS_215	VSS_303
F47	VSS_216	VSS_304
B29	VSS_217	VSS_305
F36	VSS_218	
F4	VSS_219	
B38	VSS_220	
F40	VSS_221	
F50	VSS_222	
B46	VSS_223	
B5	VSS_224	
B8	VSS_225	
BA1	VSS_226	
BA17	VSS_227	
G24	VSS_228	
G28	VSS_229	
BA2	VSS_230	
G29	VSS_231	
G33	VSS_232	
BB12	VSS_233	
G42	VSS_234	
G45	VSS_235	
GB4	VSS_236	
GB8	VSS_237	
H24	VSS_238	
H28	VSS_239	
H4	VSS_240	
H45	VSS_241	
BC25	VSS_242	
BC36	VSS_243	
BC40	VSS_244	
BC51	VSS_245	
J24	VSS_246	
BD13	VSS_247	
J28	VSS_248	
BD2	VSS_249	
J33	VSS_250	
BD28	VSS_251	
J35	VSS_252	
BD45	VSS_253	
BD48	VSS_254	
BD5	VSS_255	
BE1	VSS_256	
BE19	VSS_257	
BE23	VSS_258	
BE30	VSS_259	
L17	VSS_260	
BE42	VSS_261	
L20	VSS_262	
BE51	VSS_263	
L24	VSS_264	
BEA	VSS_265	
L28	VSS_266	
BE12	VSS_267	
L3	VSS_268	
RF16	VSS_269	
L33	VSS_270	
RF36	VSS_271	
L49	VSS_272	
RG19	VSS_273	
M28	VSS_274	
RG2	VSS_275	
M42	VSS_276	
MG24	VSS_277	
M46	VSS_278	
RG29	VSS_279	
M49	VSS_280	
RG39	VSS_281	
M5	VSS_282	
RG44	VSS_283	
M50	VSS_284	
MG	VSS_285	
NG	VSS_286	
N11	VSS_287	
N14	VSS_288	
BH17	VSS_289	
N17	VSS_290	
N29	VSS_291	
BH44	VSS_292	
N32	VSS_293	
BH8	VSS_294	
N36	VSS_295	
BH11	VSS_296	
N39	VSS_297	
BH13	VSS_298	
N44	VSS_299	
BH38	VSS_300	
N49	VSS_301	
BH4	VSS_302	
N7	VSS_303	
BH42	VSS_304	
P19	VSS_305	
BH46	VSS_306	
P2	VSS_307	
BK15	VSS_308	
P23	VSS_309	
BK17	VSS_310	
P3	VSS_311	
BK25	VSS_312	
P50	VSS_313	
BK29	VSS_314	
R49	VSS_315	
BK36	VSS_316	
T39	VSS_317	
BK40	VSS_318	
T43	VSS_319	
BK44	VSS_320	
T47	VSS_321	
BK6	VSS_322	
U41	VSS_323	
BK8	VSS_324	
U45	VSS_325	
BL11	VSS_326	
U50	VSS_327	
BL13	VSS_328	
V2	VSS_329	
BL19	VSS_330	
V3	VSS_331	
BL22	VSS_332	
BL37	VSS_333	
BL47	VSS_334	
C12	VSS_335	
C16	VSS_336	
C19	VSS_337	
C28	VSS_338	
C29	VSS_339	
C33	VSS_340	
C36	VSS_341	
C41	VSS_342	

VSS

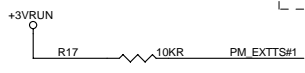
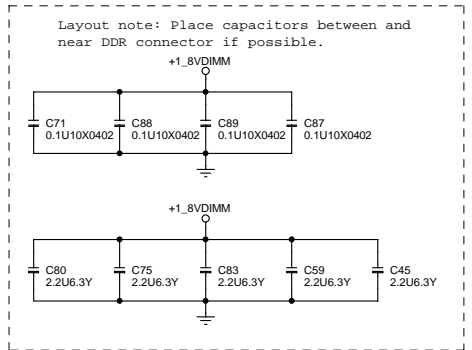
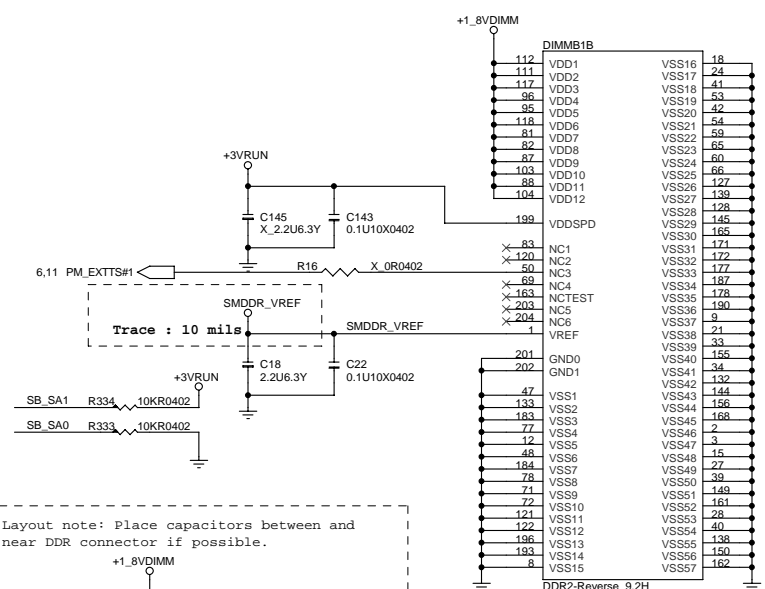
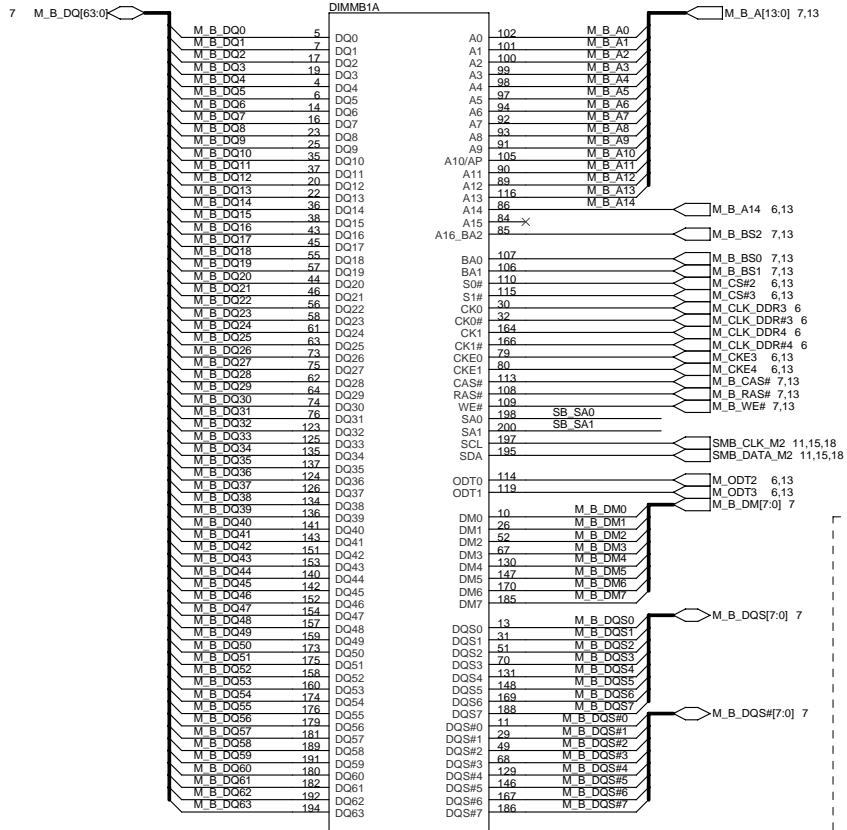
CRESTLINE\_B0

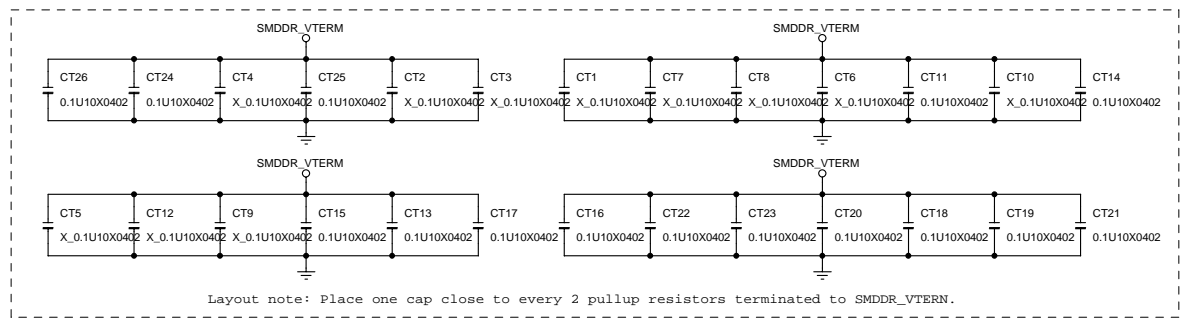
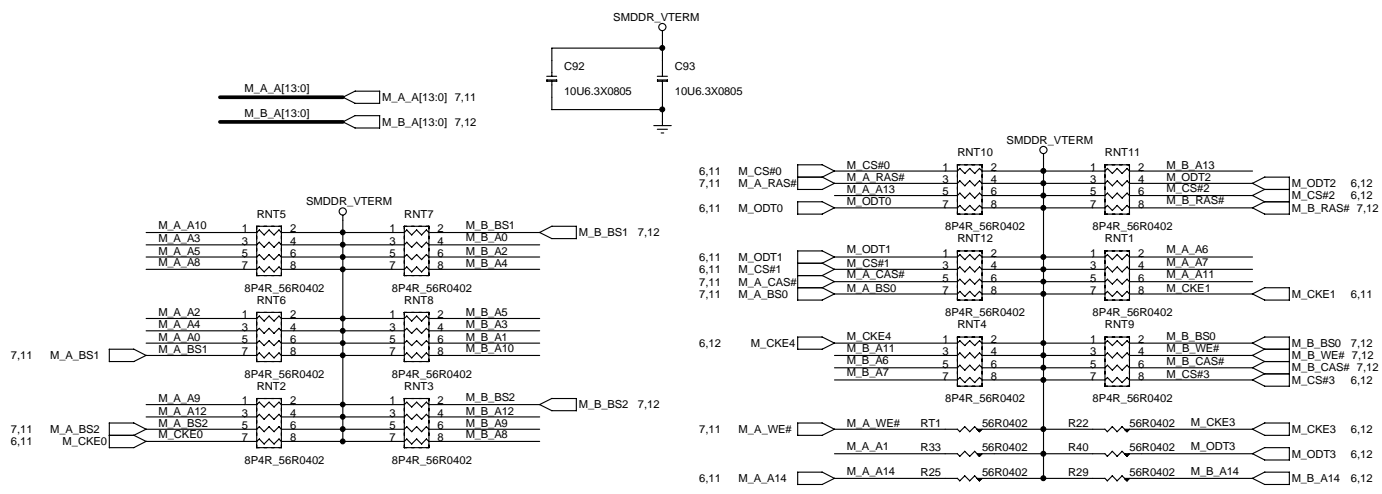
W11		
W39	VSS_288	
W43	VSS_289	
W47	VSS_290	
W5	VSS_291	
W7	VSS_292	
Y13	VSS_293	
Y2	VSS_294	
Y41	VSS_295	
Y45	VSS_296	
Y49	VSS_297	
Y5	VSS_298	
Y50	VSS_299	
Y11	VSS_300	
P28	VSS_301	
T29	VSS_302	
T31	VSS_303	
T33	VSS_304	
R28	VSS_305	
AA32	VSS_306	
AB32	VSS_307	
AD32	VSS_308	
AF28	VSS_309	
AF29	VSS_310	
AT27	VSS_311	
AV25	VSS_312	
H50	VSS_313	

MSI CORPORATION

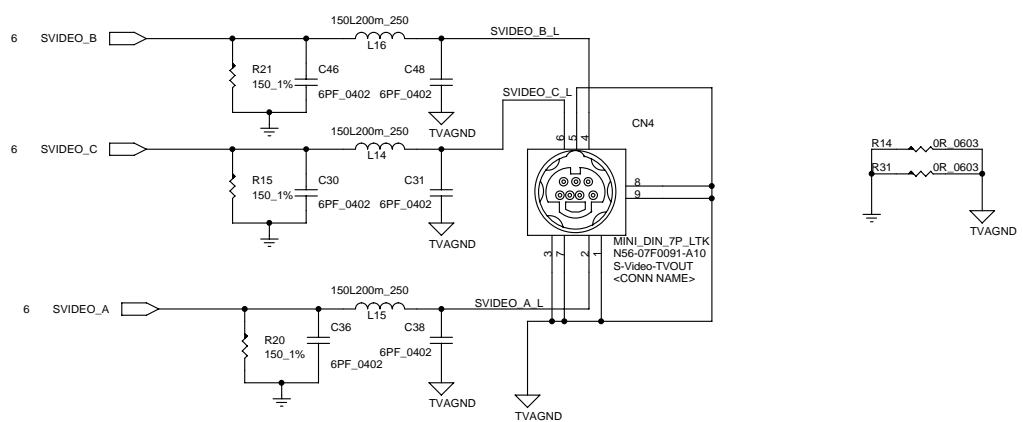
Title		
CRESTLINE-6 (VSS)		
Size	Document Number	Rev
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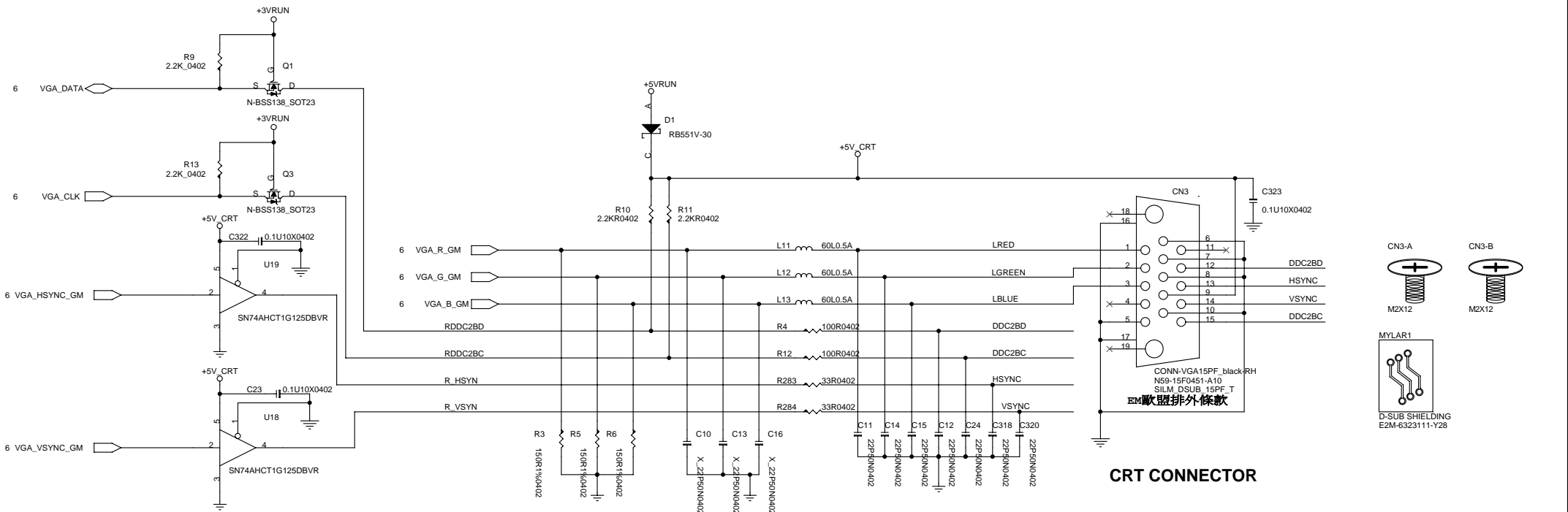




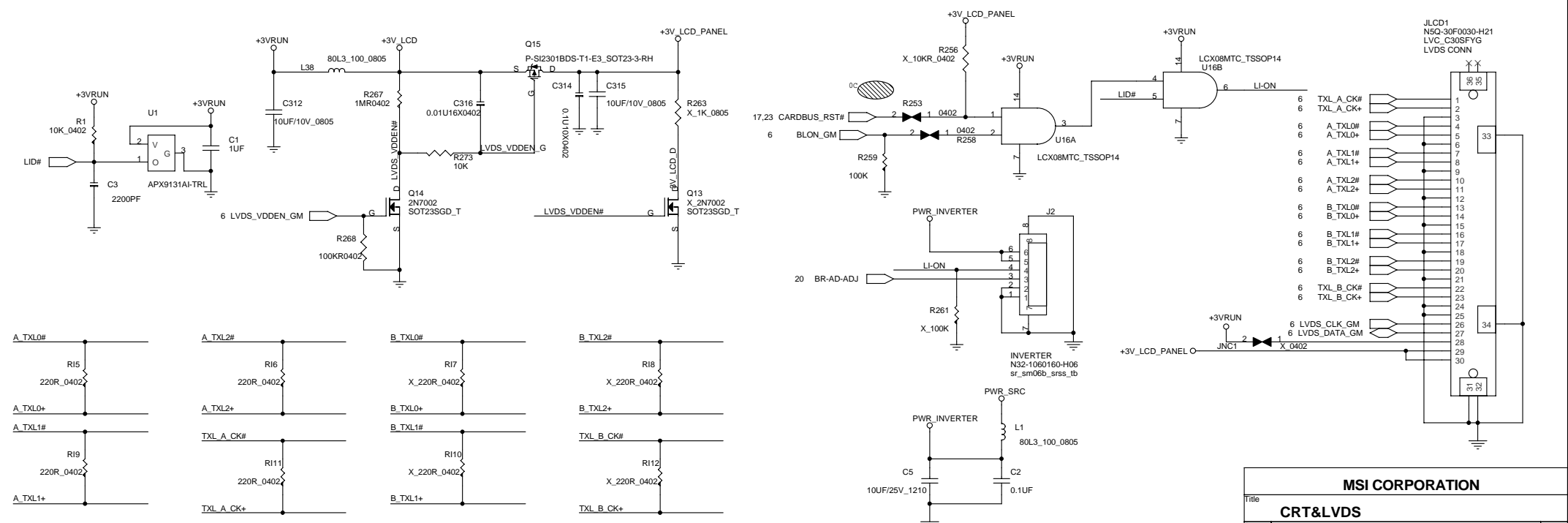
Video Filter SPEC:  
 $C = 6pF \pm 20\%$ , 16V, 0603  
 $L = 150\text{ohm}@100\text{MHz}$ , 100mA (min)



<b>MSI CORPORATION</b>		
Title <b>DDR2 TREFINATION&amp;TV_OUT</b>		
Size	Document Number	Rev
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Date:	Thursday, February 15, 2007	Sheet 13 of 42

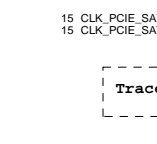
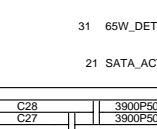
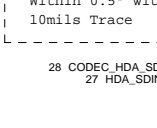
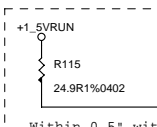
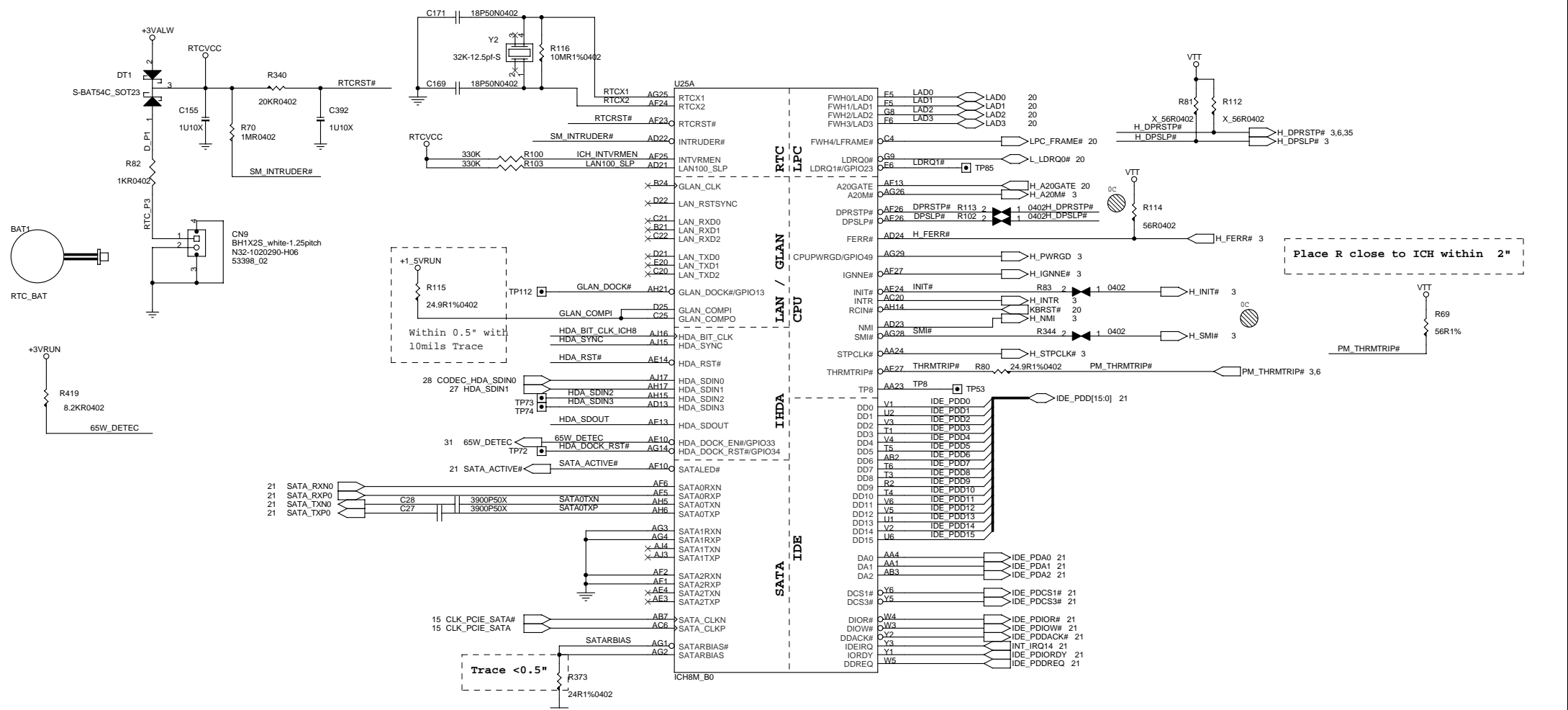


**CRT CONNECTOR**



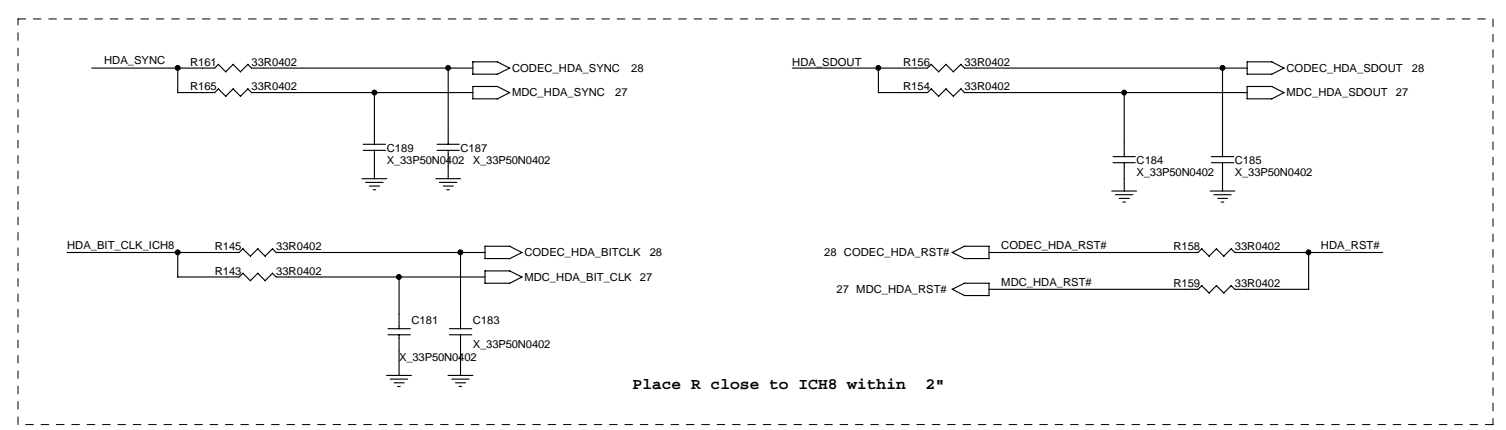
<b>MSI CORPORATION</b>		
<b>CRT&amp;LVDS</b>		
Size	Document Number	Rev
Custom	<b>MS-16371</b>	0B
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Place R close to ICH within 2"

Trace <0.5"

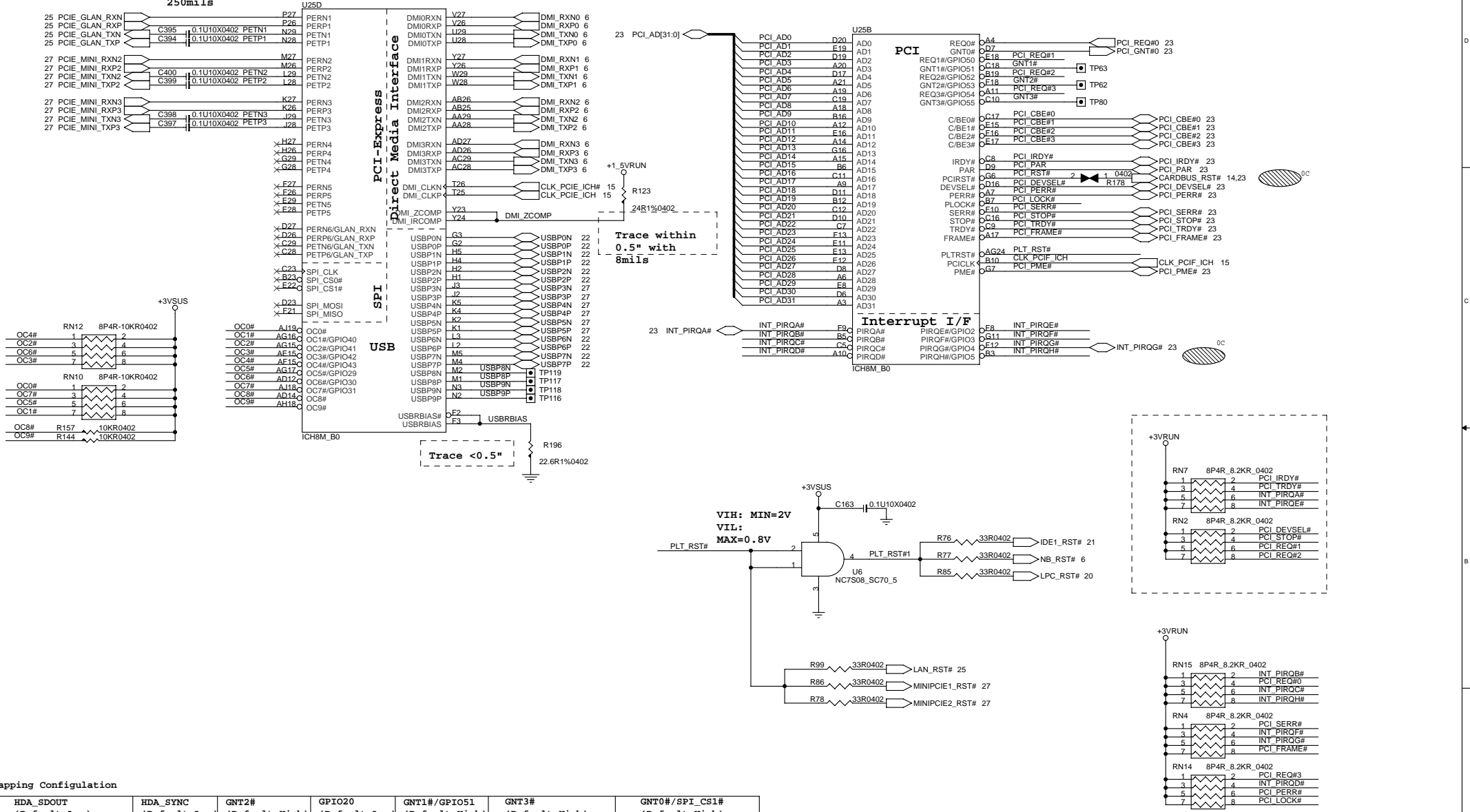


Place R close to ICH8 within 2"

<b>MSI CORPORATION</b>		
Title <b>ICH8M-1 (CPU/IDE/Azalia)</b>		
Size Custom	Document Number <b>MS-16371</b>	Rev 0B
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place Cap  
close to  
IC#8 within  
250mils



Trace within  
0.5" with  
8mils

Trace <0.5"

VIH: MIN=2V  
VIL: MAX=0.8V

Strapping Configuration

HDA_SDOUT (Default=Low)	HDA_SYNC (Default=Low)	GNT2# (Default=High)	GPIO20 (Default=Low)	GNT1#/GPIO51 (Default=High)	GNT3# (Default=High)	GNT0#/SPI_CS1# (Default=High)
XOR chain testing==>Low Set bit 1 of RPC.PC==>High	Set bit 0 of RPC.PC	Set bit 2 of RPC.PC2	Reserved	ESI Strap (server only)	Top-block swap mode ==>Low	Boot BIOS destination selection

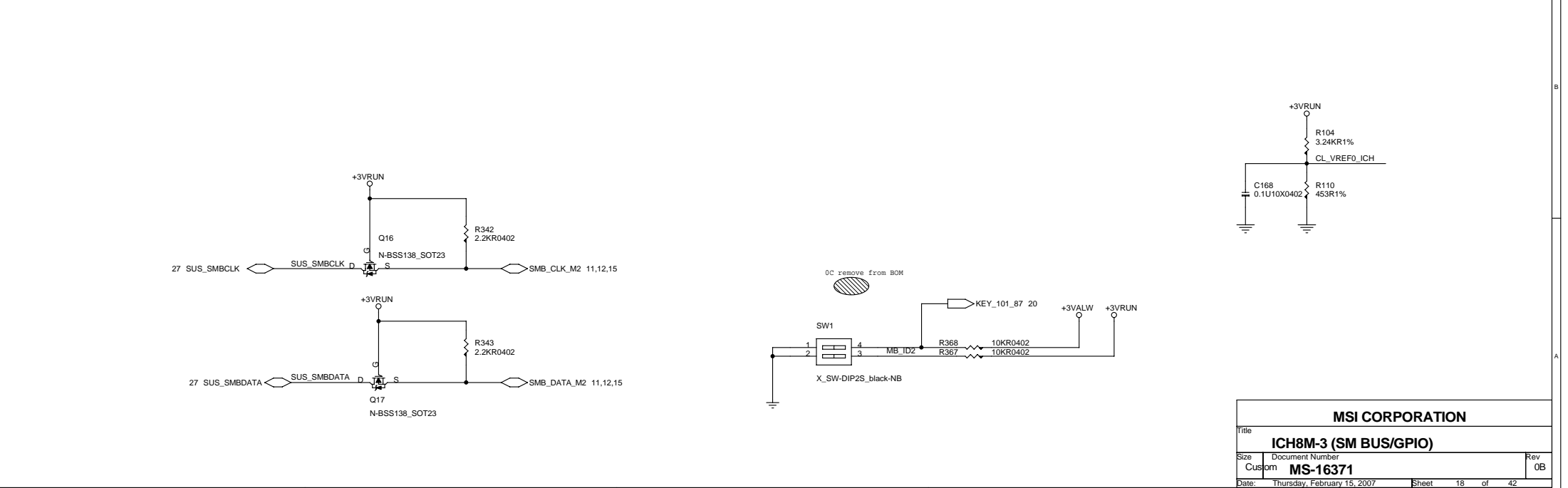
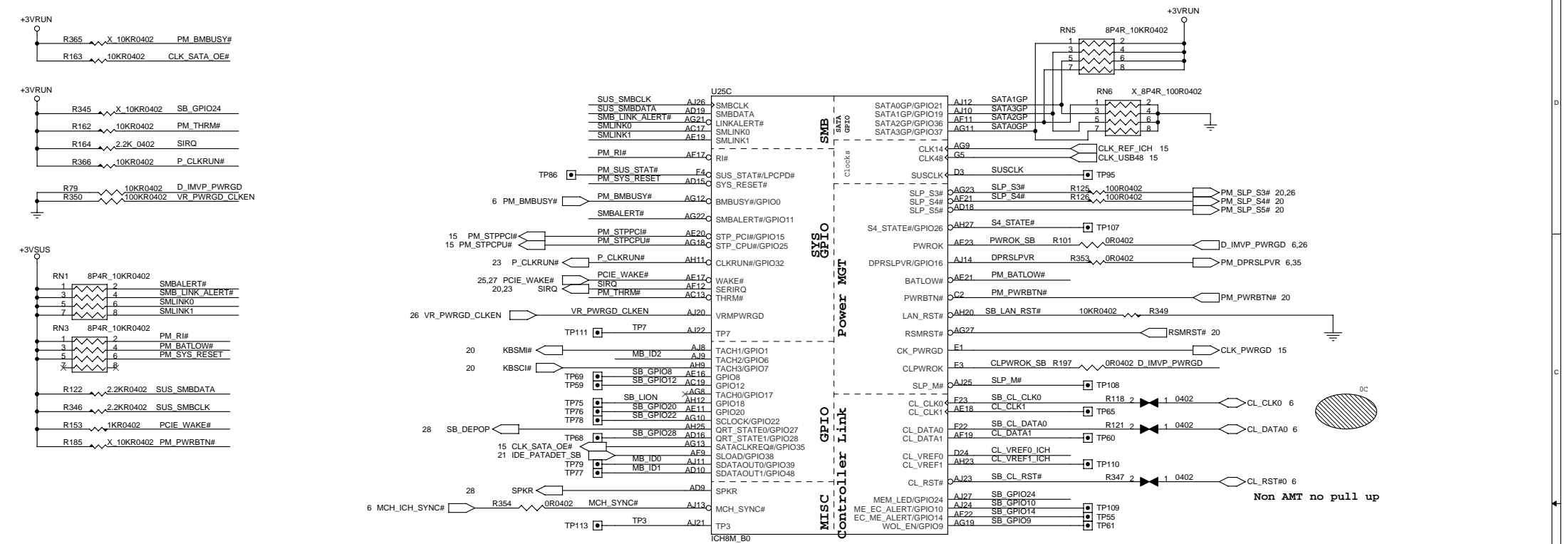
INTVRMEN	LAN100_SLP	SATALED# (Default=High)	SPKR (Default=Low)	TP3 (Default=High)	GPIO33/HDA_DOCK_EN# (Default=High)
Enable integrated Vccsus1_05, Vccsus1_5,VccCL1_5==High	Enable integrated VccLAN11_05,VccCL1_05==High	Set bit 27 of MPC.LR	No Reboot mode==>High	XOR chain Entrance	Flash Descriptor Security overridden==>Low Flash Descriptor will be in effect==>High

**MSI CORPORATION**

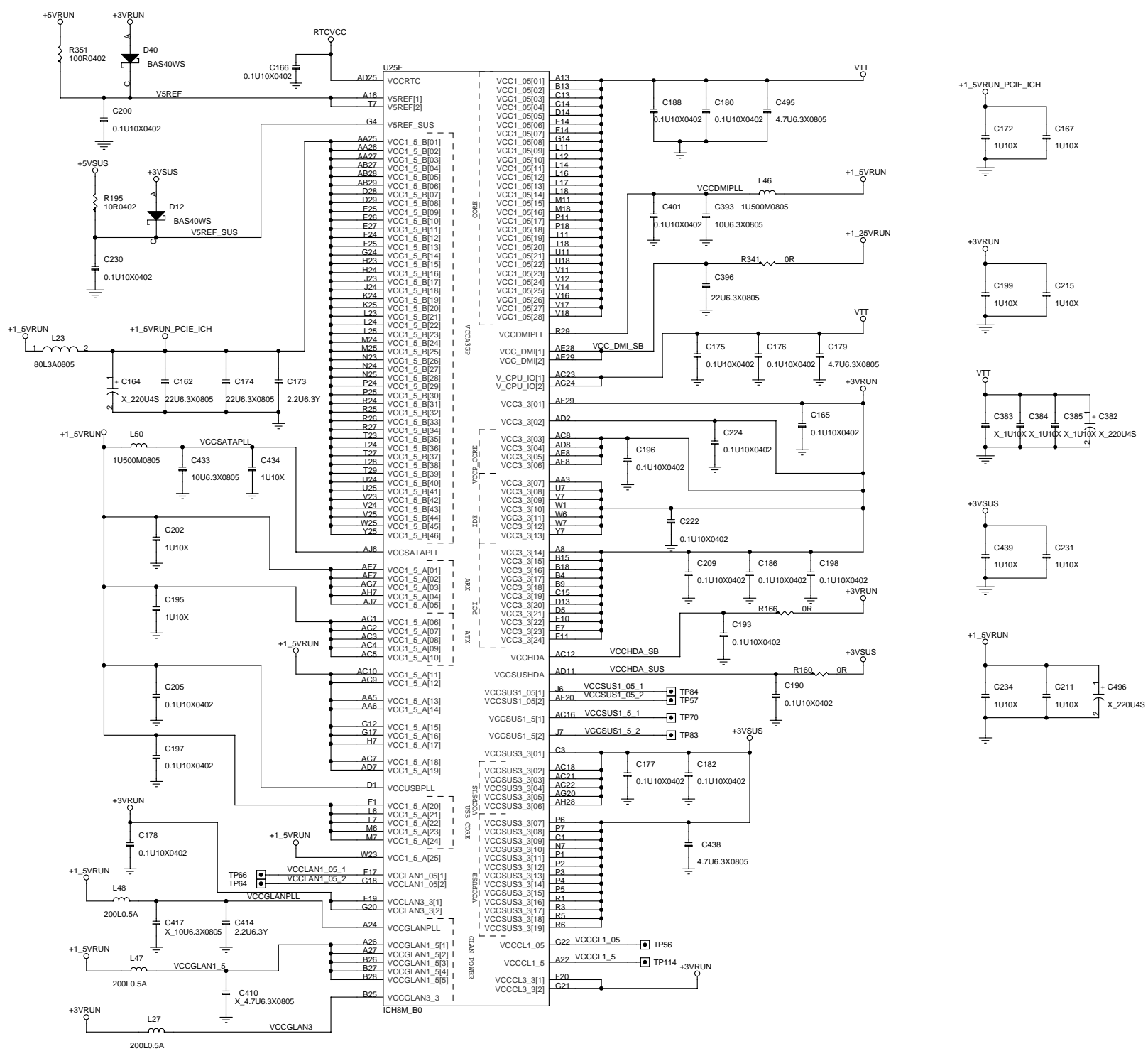
Title: **ICH8M-2 (PCI/USB/PCIE/DMI)**

Size: Document Number  
Custom: **MS-16371** Rev: 0B

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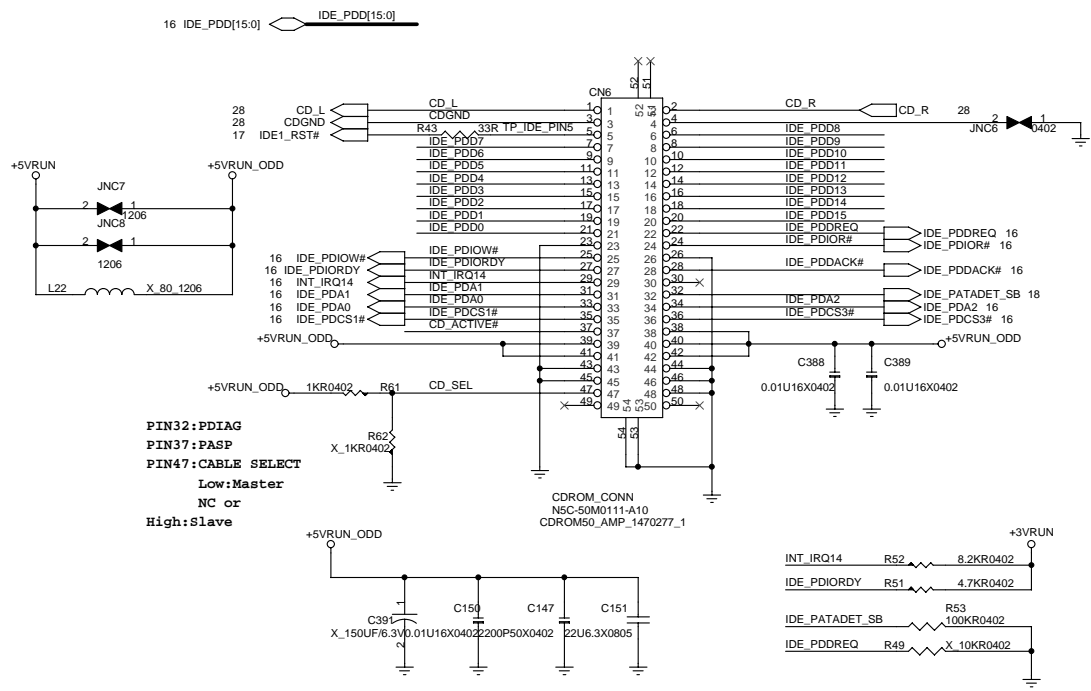
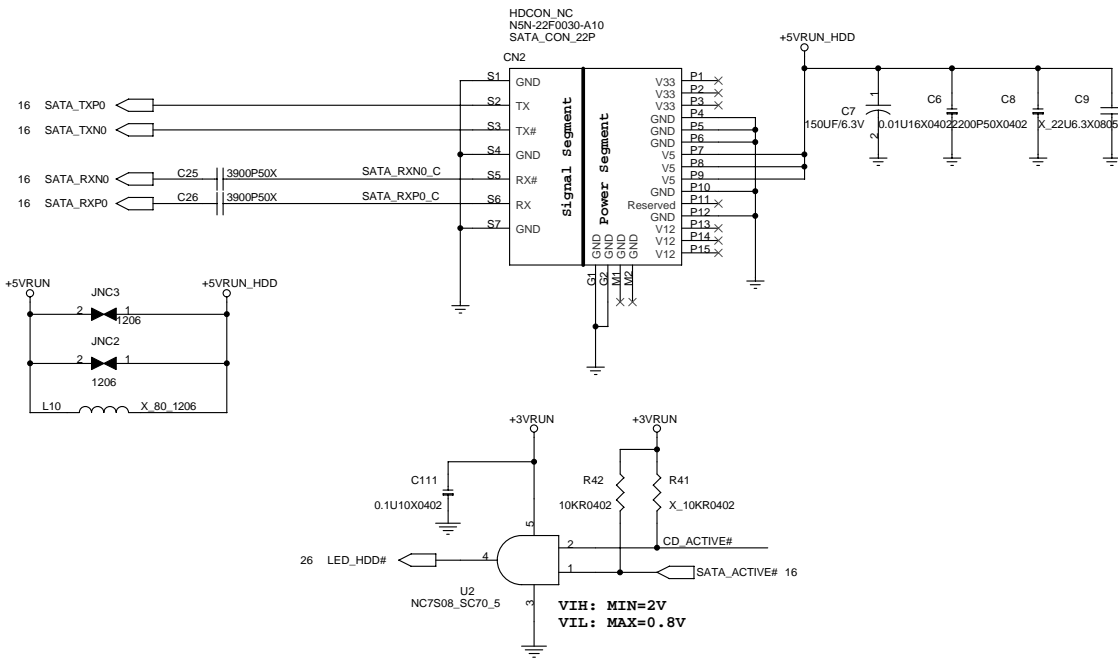


<b>MSI CORPORATION</b>		
Title <b>ICH8M-3 (SM BUS/GPIO)</b>		
Size Custom	Document Number <b>MS-16371</b>	Rev 0B
Date: Thursday, February 15, 2007	Sheet 18	of 42

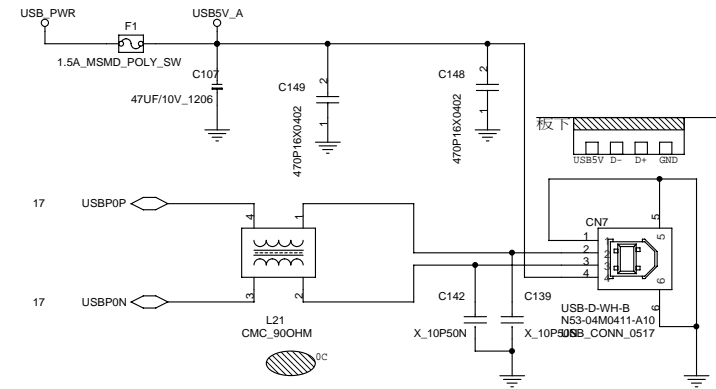
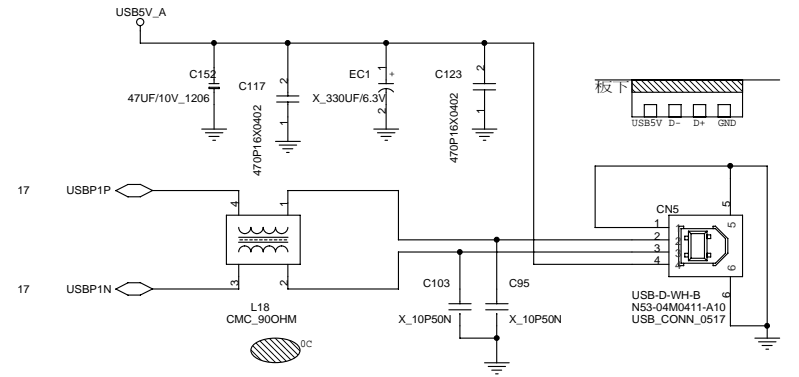
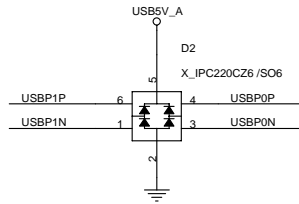
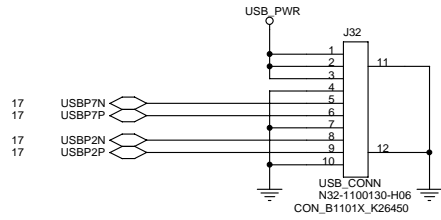
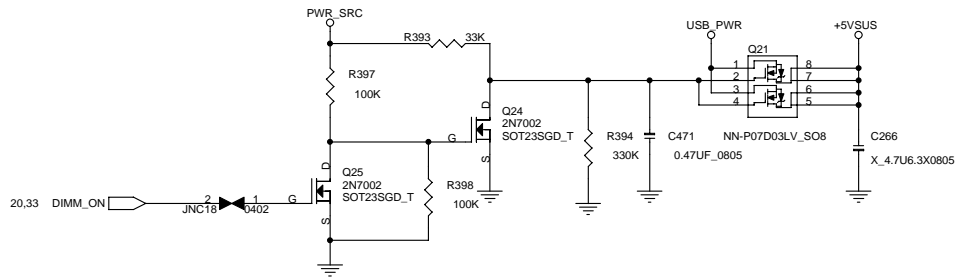


Pin	Signal	Pin	Signal
A23	VSS[001]	VSS[099]	K7
A5	VSS[002]	VSS[100]	L1
AA2	VSS[003]	VSS[101]	L13
AA3	VSS[004]	VSS[102]	L15
AA7	VSS[005]	VSS[103]	L26
AB1	VSS[006]	VSS[104]	L27
AB24	VSS[007]	VSS[105]	L4
AC11	VSS[008]	VSS[106]	L5
AC14	VSS[009]	VSS[107]	M12
AC25	VSS[010]	VSS[108]	M13
AC26	VSS[011]	VSS[109]	M14
AC27	VSS[012]	VSS[110]	M15
AD17	VSS[013]	VSS[111]	M16
AD20	VSS[014]	VSS[112]	M17
AD28	VSS[015]	VSS[113]	M23
AD29	VSS[016]	VSS[114]	M28
AD3	VSS[017]	VSS[115]	M29
AD4	VSS[018]	VSS[116]	N1
AD6	VSS[019]	VSS[117]	N11
AE1	VSS[020]	VSS[118]	N12
AE12	VSS[021]	VSS[119]	N13
AE2	VSS[022]	VSS[120]	N14
AE22	VSS[023]	VSS[121]	N15
AD1	VSS[024]	VSS[122]	N16
AE25	VSS[025]	VSS[123]	N17
AE5	VSS[026]	VSS[124]	N18
AE6	VSS[027]	VSS[125]	N19
AE14	VSS[028]	VSS[126]	N27
AE26	VSS[029]	VSS[127]	N28
AE16	VSS[030]	VSS[128]	N4
AF18	VSS[031]	VSS[129]	N5
AE3	VSS[032]	VSS[130]	N6
AE4	VSS[033]	VSS[131]	P12
AG5	VSS[034]	VSS[132]	P13
AG6	VSS[035]	VSS[133]	P14
VSS[036]	VSS[134]	VSS[135]	P15
AH10	VSS[037]	VSS[136]	P16
AH13	VSS[038]	VSS[137]	P17
AH16	VSS[039]	VSS[138]	P18
AH19	VSS[040]	VSS[139]	P19
AH2	VSS[041]	VSS[140]	R11
AH28	VSS[042]	VSS[141]	R12
AH24	VSS[043]	VSS[142]	R13
AH26	VSS[044]	VSS[143]	R14
AH3	VSS[045]	VSS[144]	R15
AH4	VSS[046]	VSS[145]	R16
AH8	VSS[047]	VSS[146]	R17
AJ5	VSS[048]	VSS[147]	R18
B11	VSS[049]	VSS[148]	R28
B14	VSS[050]	VSS[149]	R4
B17	VSS[051]	VSS[150]	R12
B2	VSS[052]	VSS[151]	T12
B20	VSS[053]	VSS[152]	T13
B22	VSS[054]	VSS[153]	T14
B8	VSS[055]	VSS[154]	T15
C24	VSS[056]	VSS[155]	T16
C26	VSS[057]	VSS[156]	T17
C27	VSS[058]	VSS[157]	T18
C6	VSS[059]	VSS[158]	U12
D12	VSS[060]	VSS[159]	U13
D15	VSS[061]	VSS[160]	U14
D2	VSS[062]	VSS[161]	U15
D4	VSS[063]	VSS[162]	U16
F21	VSS[064]	VSS[163]	U23
F24	VSS[065]	VSS[164]	U26
E4	VSS[066]	VSS[165]	U3
E9	VSS[067]	VSS[166]	U13
F15	VSS[068]	VSS[167]	U15
F28	VSS[069]	VSS[168]	U16
F29	VSS[070]	VSS[169]	U17
F7	VSS[071]	VSS[170]	V29
G1	VSS[072]	VSS[171]	W2
G11	VSS[073]	VSS[172]	W26
E2	VSS[074]	VSS[173]	W27
G10	VSS[075]	VSS[174]	Y28
G13	VSS[076]	VSS[175]	Y29
G19	VSS[077]	VSS[176]	Y4
G23	VSS[078]	VSS[177]	Y28
G26	VSS[079]	VSS[178]	Y4
G28	VSS[080]	VSS[179]	AB23
G27	VSS[081]	VSS[180]	AB5
H25	VSS[082]	VSS[181]	AB6
H28	VSS[083]	VSS[182]	AD5
H29	VSS[084]	VSS[183]	U4
H3	VSS[085]	VSS[184]	W24
H6	VSS[086]	VSS[185]	
H6	VSS[087]	VSS[186]	
J1	VSS[088]	VSS_NCTF[01]	A1
J25	VSS[089]	VSS_NCTF[02]	A2
J26	VSS[090]	VSS_NCTF[03]	A28
J27	VSS[091]	VSS_NCTF[04]	A29
J4	VSS[092]	VSS_NCTF[05]	AH1
J6	VSS[093]	VSS_NCTF[06]	AH29
K23	VSS[094]	VSS_NCTF[07]	A11
K28	VSS[095]	VSS_NCTF[08]	A12
K29	VSS[096]	VSS_NCTF[09]	A128
K3	VSS[097]	VSS_NCTF[10]	A129
K6	VSS[098]	VSS_NCTF[11]	B1
VSS[099]	VSS[099]	VSS_NCTF[12]	B29

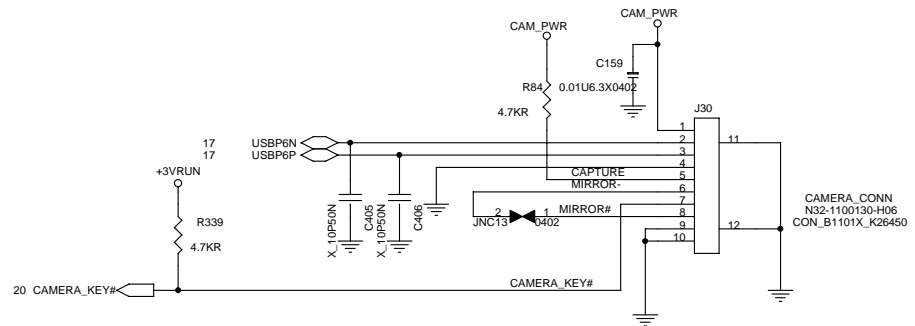
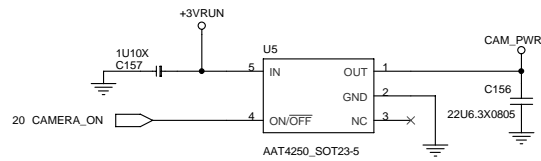




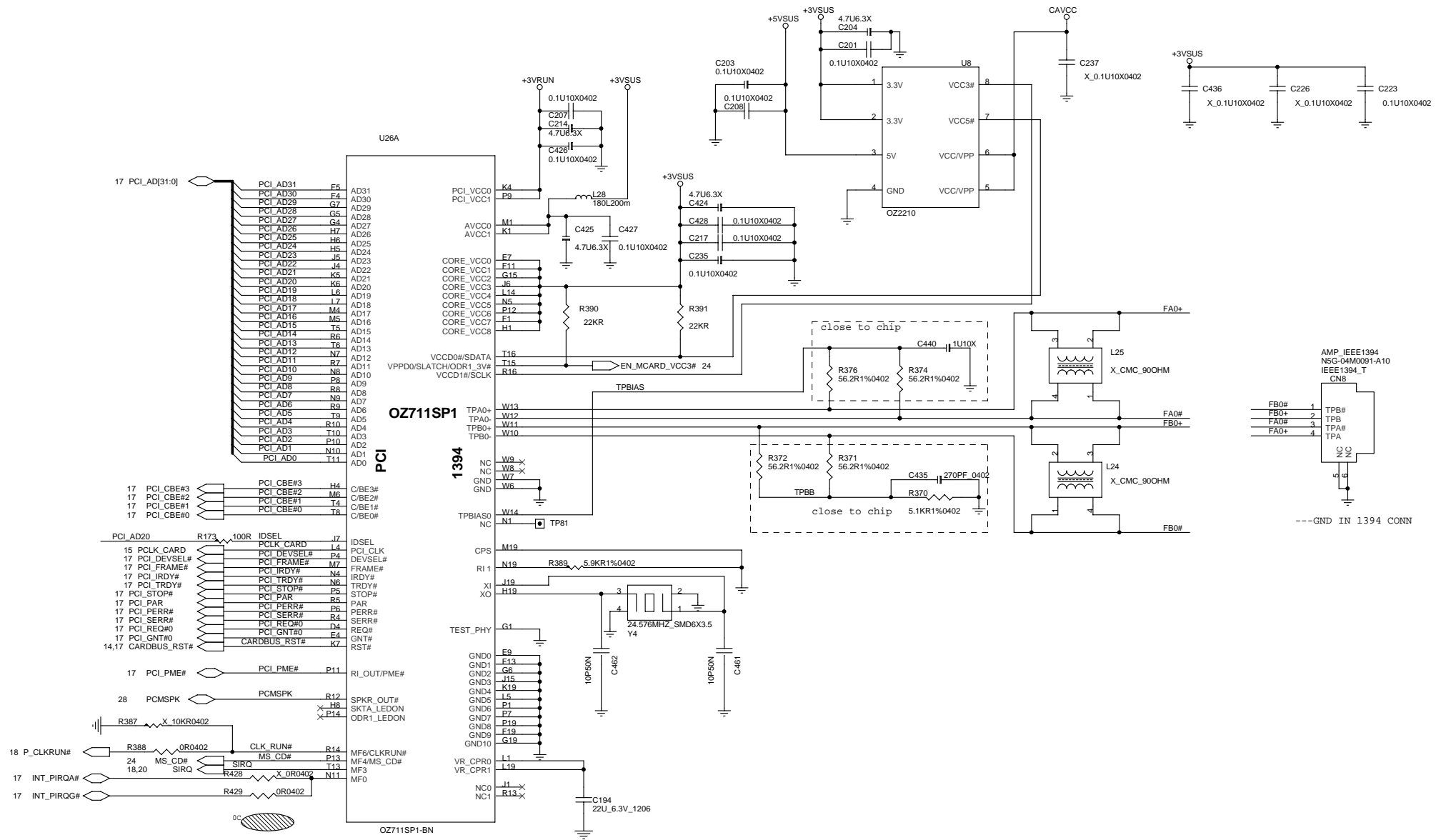
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Title	<b>HDD&amp;ODD</b>	
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### DIGITAL CAMERA



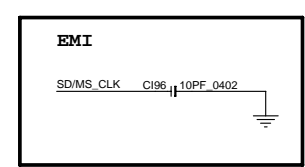
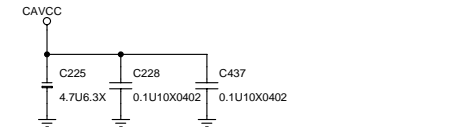
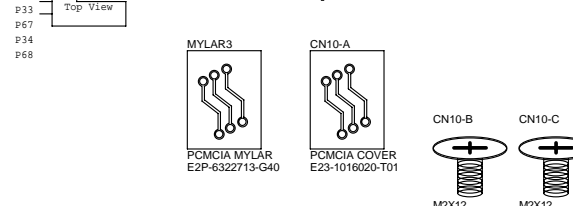
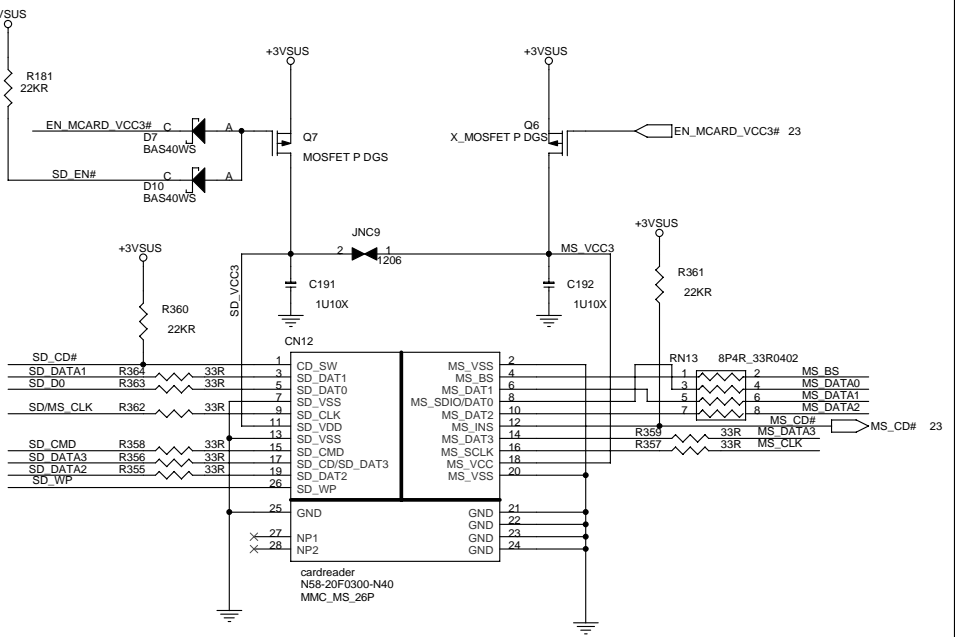
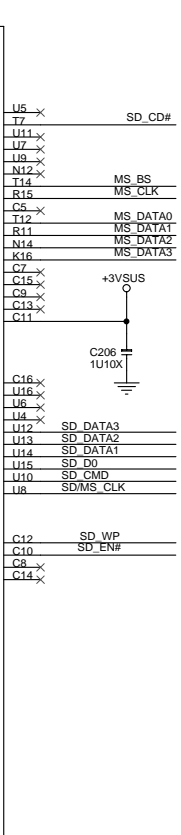
<b>MSI CORPORATION</b>		
Title	<b>USB &amp; CMOS</b>	
Size	Document Number	Rev
Custom	<b>MS-16371</b>	<b>0B</b>
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<b>MSI CORPORATION</b>		
Title <b>OZ711SP1-1(PCI Bus / 1394 )</b>		
Size	Document Number	Rev
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PCMCIA 68P: 1016 TAISOL_146-2221210-01_PCMCIA_SMT NSD-68M0220-T01					
GND	P01	GND	P35	GND	
CAD0	P02	CAD0(D3)	CCD1#(CD1#)	P36	CCD1#
CAD1	P03	CAD1(D4)	CAD2(D11)	P37	CAD2
CAD3	P04	CAD3(D5)	CAD4(D12)	P38	CAD4
CAD5	P05	CAD5(D6)	CAD6(D13)	P39	CAD6
CAD7	P06	CAD7(D7)	RFU(R2_D14)	P40	R2_D14
CC/BE#0	P07	CC/BE#0(CE1#)	CAD8(D15)	P41	CAD8
CAD9	P08	CAD9(A10)	CAD10(CE2#)	P42	CAD10
CAD11	P09	CAD11(OE#)	CVS1	P43	CVS1
CAD12	P10	CAD12(A11)	CAD13(IORD#)	P44	CAD13
CAD14	P11	CAD14(A9)	CAD15(IOWR#)	P45	CAD15
CC/BE#1	P12	CC/BE1#(A8)	CAD16(A17)	P46	CAD16
CPAR	P13	CPAR(A13)	RFU(R2_A18)	P47	R2_A18
CPERR#	P14	CPERR#(A14)	CBLOCK#(A19)	P48	CBLOCK#
CGNT#	P15	CGNT#(WE#)	CSTOP#(A20)	P49	CSTOP#
CINT#	P16	CINT#(IRQ#)	CDEVSEL#(A21)	P50	CDEVSEL#
CAVCC	P17	VCC	VCC	P51	CAVCC
CAVCC	P18	VPP	VPP	P52	CAVCC
CCLK	P19	CCLK(A16)	CTRDY#(A22)	P53	CTRDY#
CIRDY#	P20	CIRDY#(A15)	CFRAME#(A23)	P54	CFRAME#
CC/BE#2	P21	CC/BE2#(A12)	CAD17(A24)	P55	CAD17
CAD18	P22	CAD18(A7)	CAD19(A25)	P56	CAD19
CAD20	P23	CAD20(A6)	CVS2	P57	CVS2
CAD21	P24	CAD21(A5)	CRESET#(RESET)	P58	CRST#
CAD22	P25	CAD22(A4)	CSERR#(WAIT#)	P59	CSERR#
CAD23	P26	CAD23(A3)	CREQ#(INPACK#)	P60	CREQ#
CAD24	P27	CAD24(A2)	CC/BE3#(REG#)	P61	CC/BE#3
CAD25	P28	CAD25(A1)	CAUDIO(BVD2/SPKR#)	P62	CAUDIO#
CAD26	P29	CAD26(A0)	CSTSCHNG(BVD1/R1#)	P63	CSTSCHNG
CAD27	P30	CAD27(D0)	CAD28(D8)	P64	CAD28
CAD29	P31	CAD29(D1)	CAD30(D9)	P65	CAD30
R2_D2	P32	RFU(R2_D2)	CAD31(D10)	P66	CAD31
CCLKRUN#	P33	CCLKRUN#(IO16#)	CCD2#(CD2#)	P67	CCD2#
GND	P34	GND	GND	P68	GND

U26B		
CAD31	E5	D10/CAD31
CAD30	E6	D9/CAD30
CAD29	E6	D1/CAD29
CAD28	D6	D8/CAD28
CAD27	E7	D0/CAD27
CAD26	D9	A0/CAD26
CAD25	G10	A1/CAD25
CAD24	F10	A2/CAD24
CAD23	D11	A3/CAD23
CAD22	G11	A4/CAD22
CAD21	D12	A5/CAD21
CAD20	F12	A6/CAD20
CAD19	D13	A25/CAD19
CAD18	E13	A7/CAD18
CAD17	G13	A24/CAD17
CAD16	H15	A17/CAD16
CAD15	J13	I0WR#CAD15
CAD14	H16	A9/CAD14
CAD13	J14	IORD#CAD13
CAD12	J14	A11/CAD12
CAD11	K13	CE#CAD11
CAD10	K14	CE#CAD10
CAD9	K15	A10/CAD9
CAD8	L15	D15/CAD8
CAD7	L13	D7/CAD7
CAD6	M14	D13/CAD6
CAD5	M15	D6/CAD5
CAD4	M16	D12/CAD4
CAD3	M13	D5/CAD3
CAD2	N13	D11/CAD2
CAD1	N15	D4/CAD1
CAD0	P16	D3/CAD0
CC/BE#3	F10	REG#CCBE3#
CC/BE#2	D14	A12/CCBE2#
CC/BE#1	H14	A8/CCBE1#
CC/BE#0	L16	CE1#/CCBE0#
CLK	F15	A16/CLK
CIRDY#	D15	A23/CIRDY#
CTRDY#	D16	A22/CTRDY#
CDEVSEL#	F16	A21/CDEVSEL#
CSTOP#	F15	A20/CSTOP#
CPAR	G16	A13/CPAR
CPERR#	F16	A14/CPERR#
CSERR#	D8	WAIT#/CSERR#
CREQ#	F11	INPACK#/CREQ#
CINT#	F14	WE#/CINT#
CBLOCK#	G14	RDY#/REO#/CINT#
CCLKRUN#	G8	WP#/IOIS16/CCLKRUN#
CRST#	F12	RESET/CRST#
R2_D2	D5	A18/RFU
R2_D14	M16	D2/RFU
R2_A18	H13	A18/RFU
CVS1	F9	V51/VS1
CVS2	G12	V52/VS2
CCD1#	P15	CD1#/CCD1#
CCD2#	D7	CD2#/CCD2#
CAUDIO#	E8	BVD2/SPKR#/CAUDIO
CSTSCHNG	F8	BVD1/R1#/CSTSCHNG



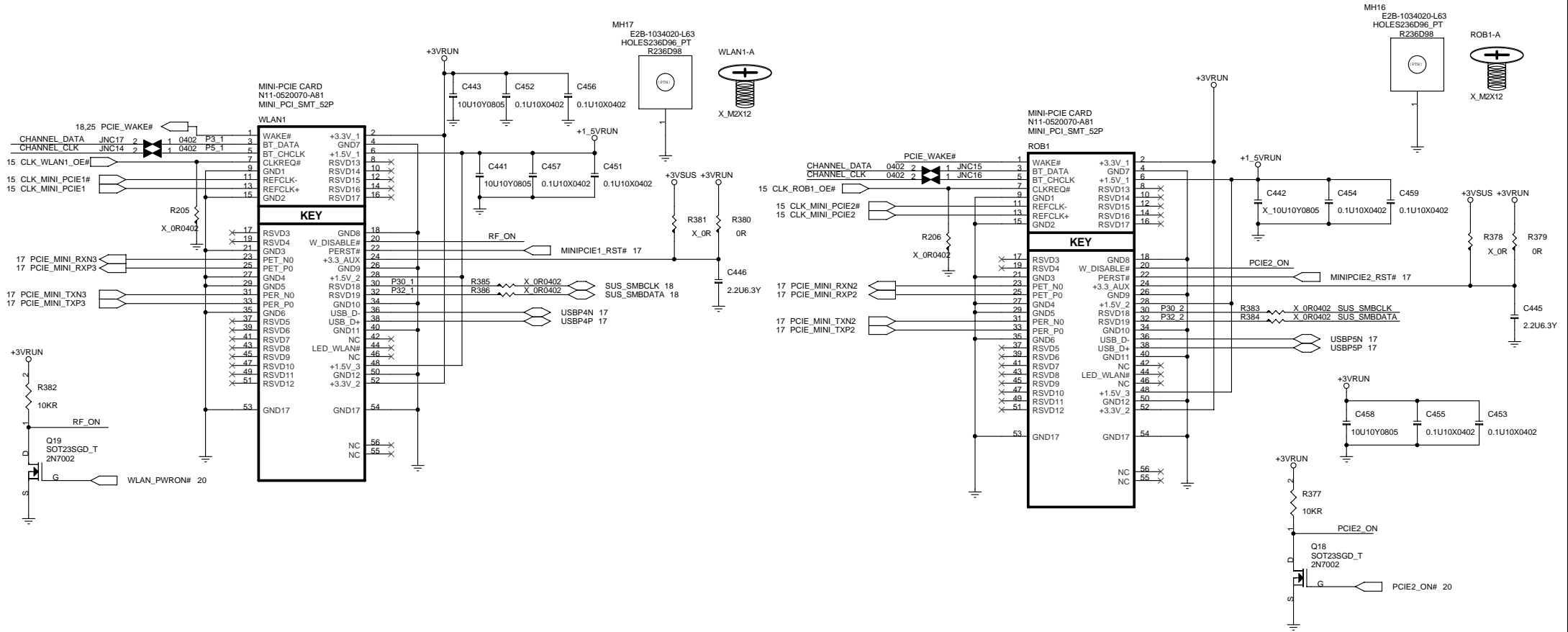
<b>MSI CORPORATION</b>		
Title <b>OZ711SP1-2(PCMCIA / CARD)</b>		
Size	Document Number	Rev
Custom	<b>MS-16371</b>	0B
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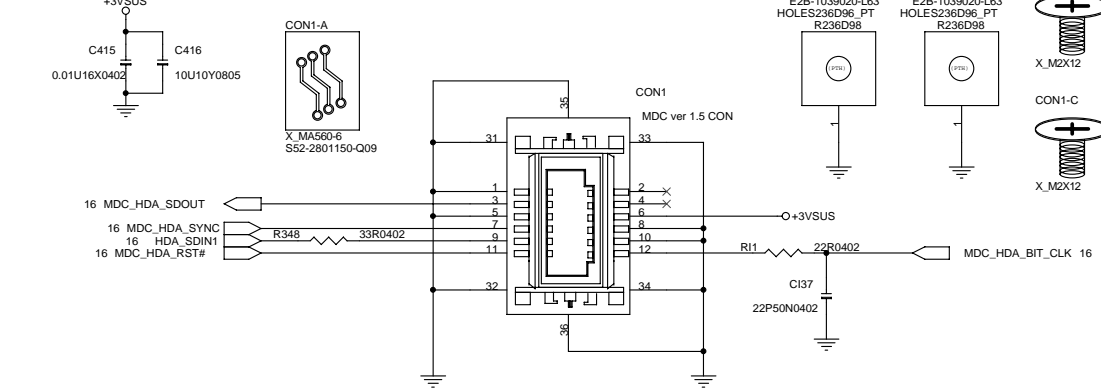




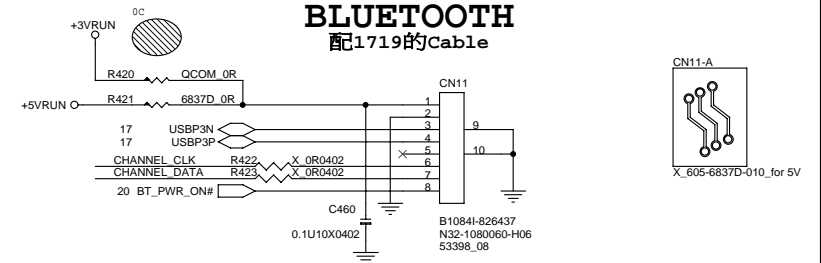
# WLAN and Robson



# MDC Connector Ver 1.5

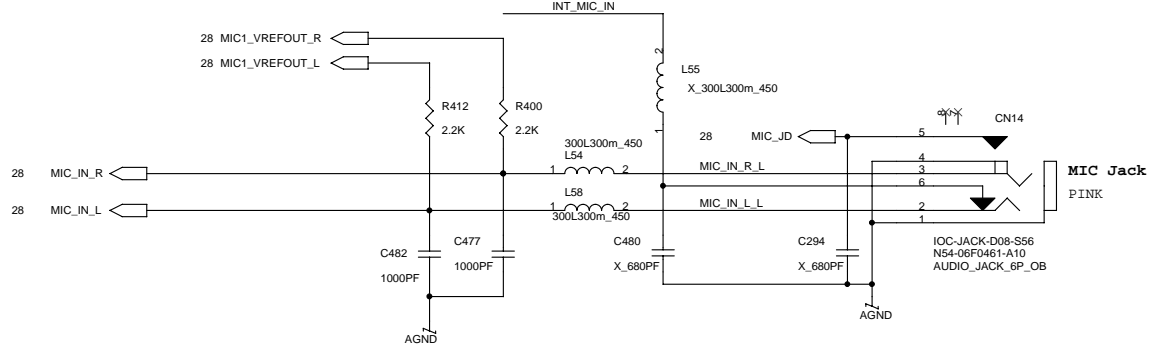
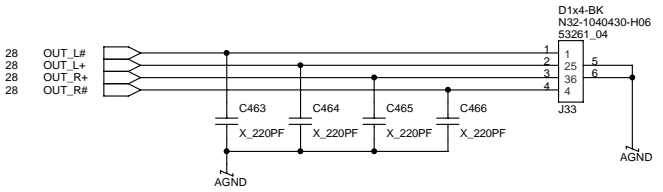
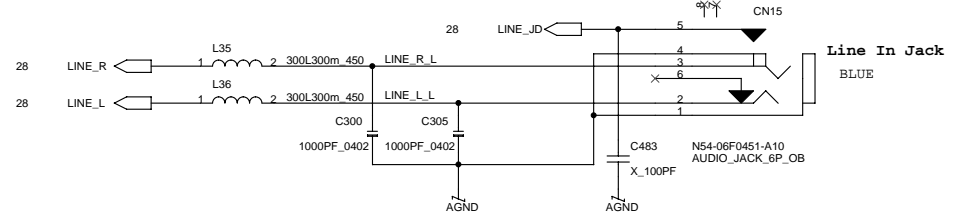
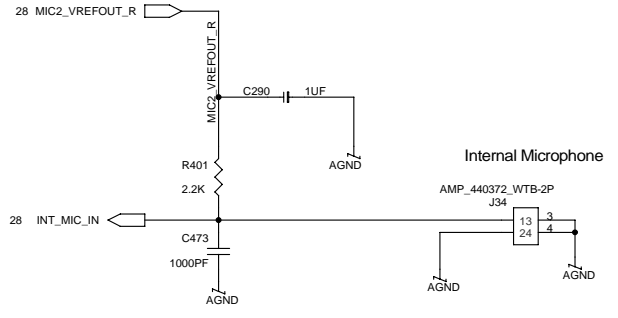
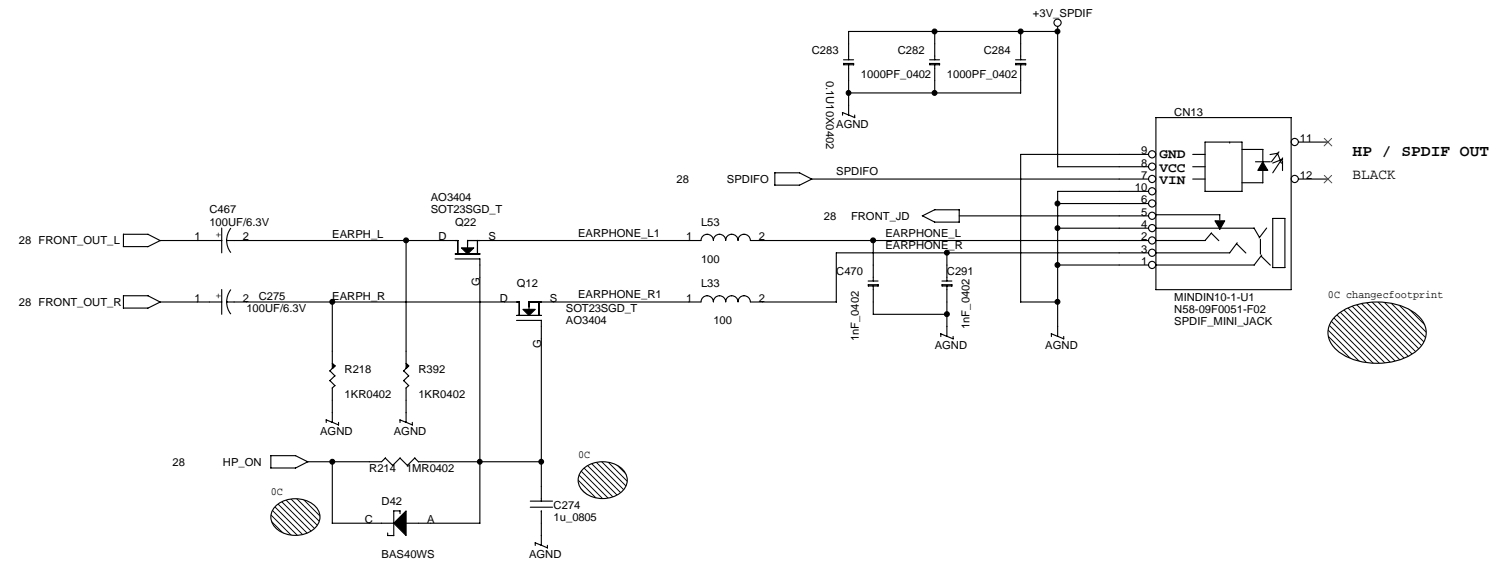
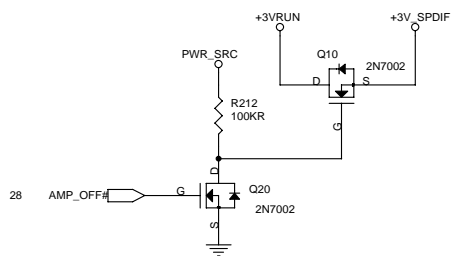


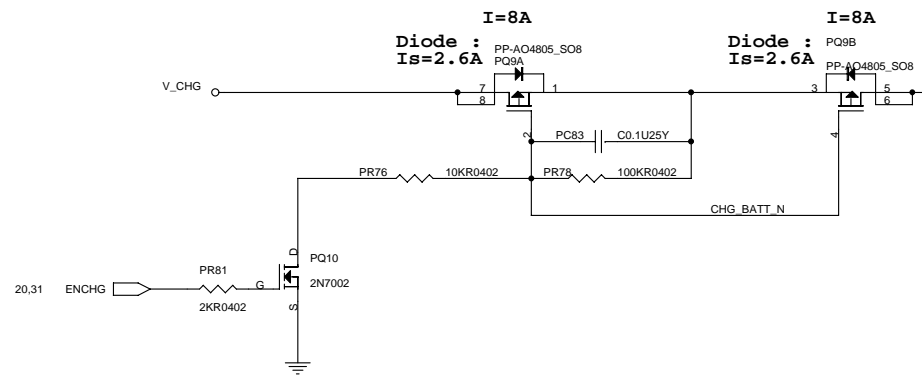
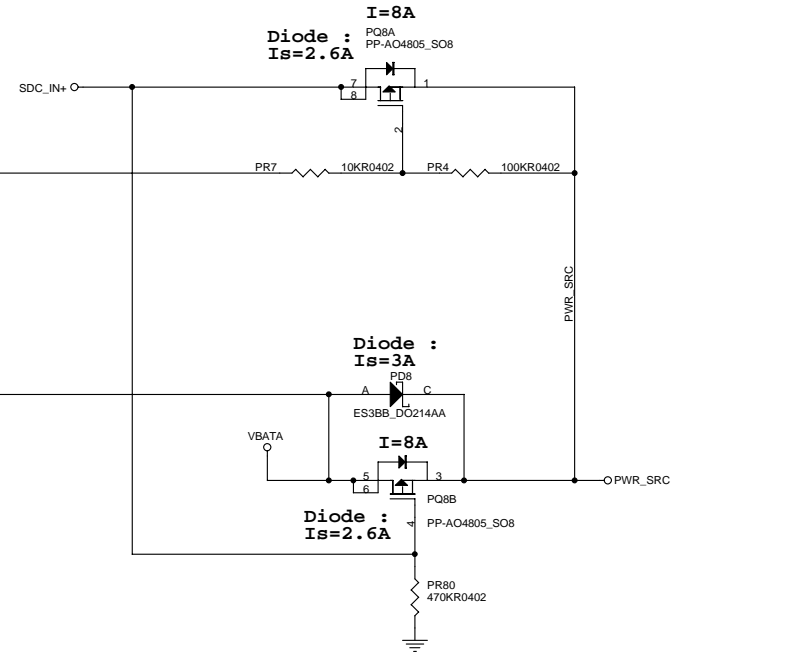
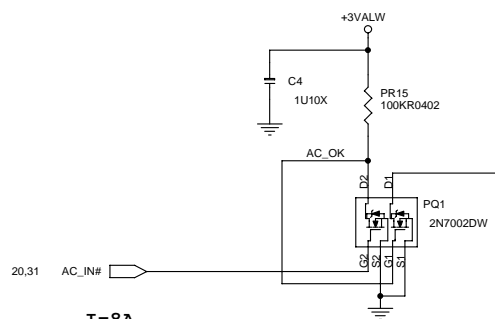
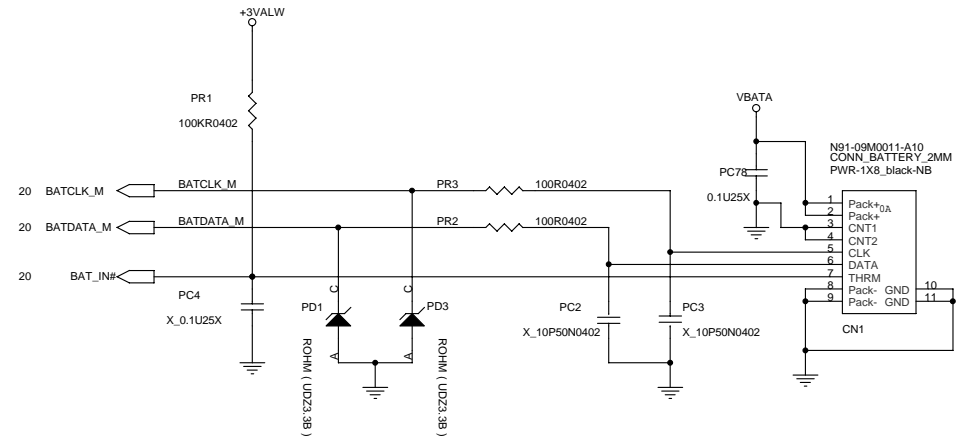
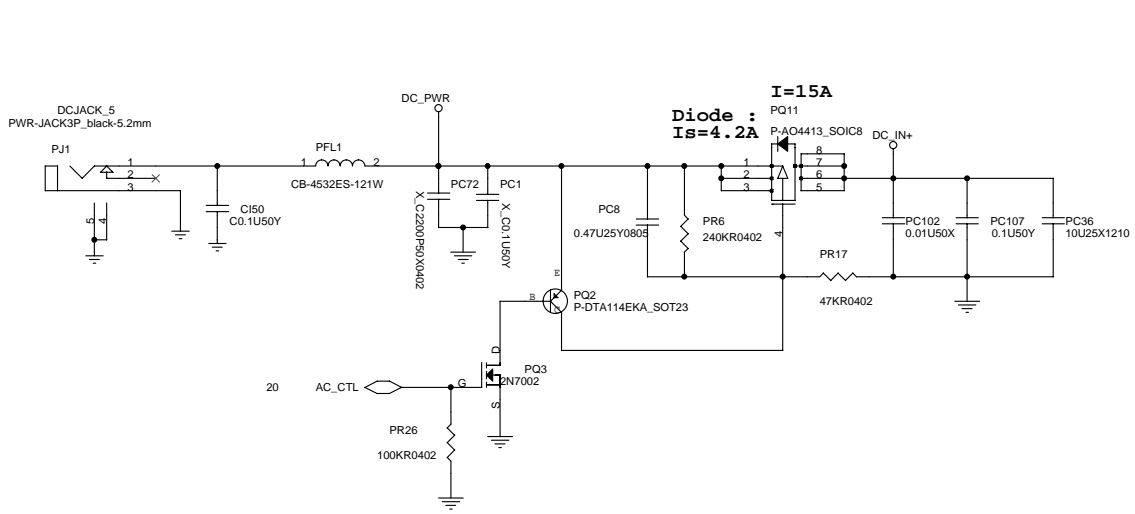
# BLUETOOTH 配1719的cable



<b>MSI CORPORATION</b>		
Title	<b>Mini PCIE &amp; MDC &amp; BT</b>	
Size	Document Number	Rev
Custom	<b>MS-16371</b>	<b>0B</b>
Date:	Thursday, February 15, 2007	Sheet 27 of 42

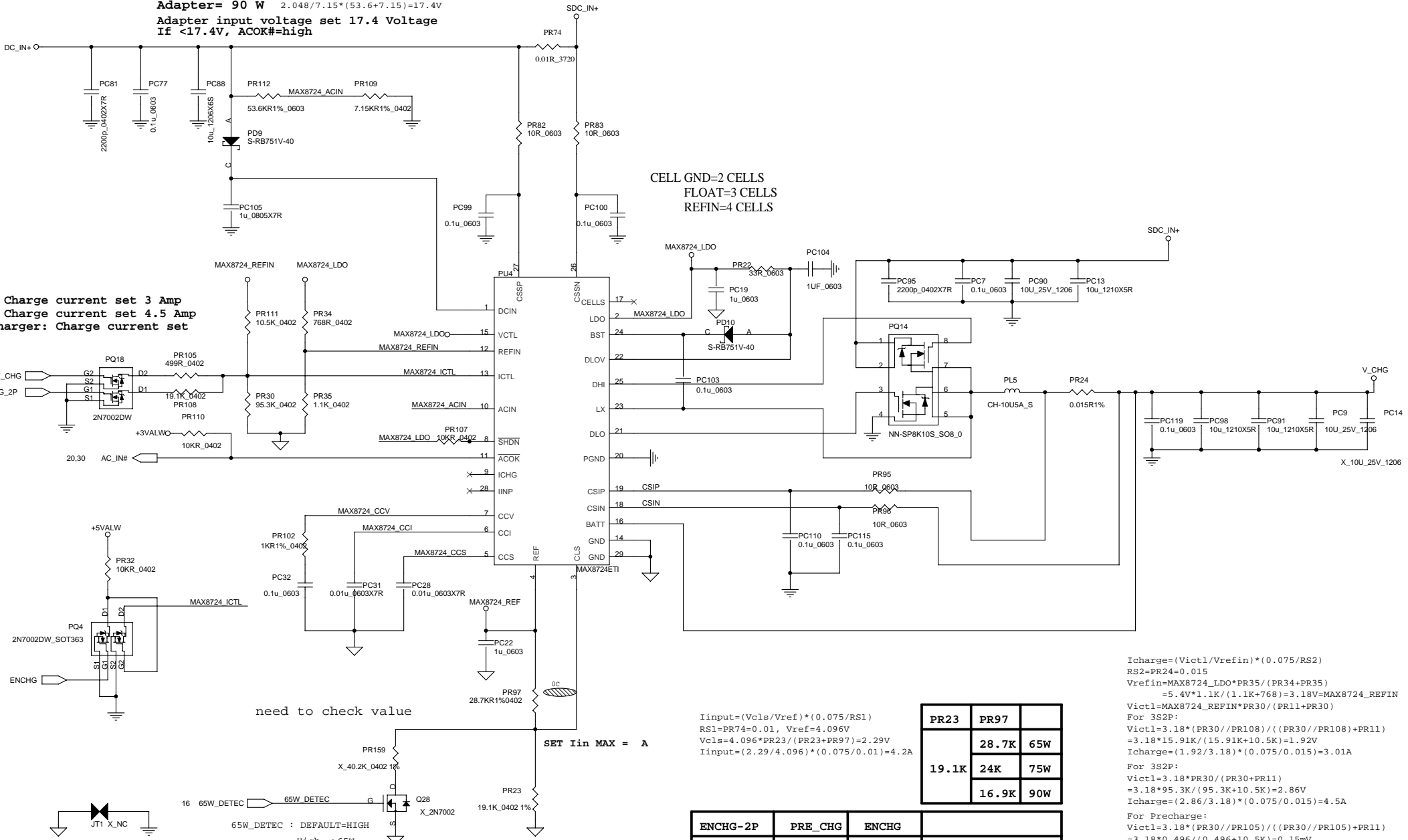






<b>MSI CORPORATION</b>		
Title	<b>Battery Select</b>	
Size	Document Number	Rev
Custom	<b>MS-16371</b>	<b>0B</b>
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(Vref/2)/(PR109\*(PR112+PR109))  
**Adapter= 90 W** 2.048/7.15\*(53.6+7.15)=17.4V  
**Adapter input voltage set 17.4 Voltage**  
**If <17.4V, ACOK#=high**



CELL GND=2 CELLS  
 FLOAT=3 CELLS  
 REFIN=4 CELLS

**3S2P: Charge current set 3 Amp**  
**3S3P: Charge current set 4.5 Amp**  
**Pre-charger: Charge current set 220mA**

need to check value

**90W for LG**  
 PR97-A  
 X-16.9KR1%-0402

Iinput=(Vcls/Vref)\*(0.075/RS1)  
 RS1=PR74=0.01, Vref=4.096V  
 Vcls=4.096\*PR23/(PR23+PR97)=2.29V  
 Iinput=(2.29/4.096)\*(0.075/0.01)=4.2A

PR23	PR97	
	28.7K	65W
19.1K	24K	75W
	16.9K	90W

Icharge=(Victl/Vrefin)\*(0.075/RS2)  
 RS2=PR24=0.015  
 Vrefin=MAX8724\_LDO\*PR35/(PR34+PR35)  
 =5.4V\*1.1K/(1.1K+768)=3.18V=MAX8724\_REFIN  
 For 3S2P:  
 Victl=MAX8724\_REFIN\*PR30/(PR11+PR30)  
 Victl=3.18\*(PR30//PR108)/((PR30//PR108)+PR11)  
 =3.18\*15.91K/(15.91K+10.5K)=1.92V  
 Icharge=(1.92/3.18)\*(0.075/0.015)=3.01A  
 For 3S3P:  
 Victl=3.18\*PR30/(PR30+PR11)  
 =3.18\*95.3K/(95.3K+10.5K)=2.86V  
 Icharge=(2.86/3.18)\*(0.075/0.015)=4.5A  
 For Precharge:  
 Victl=3.18\*(PR30//PR105)/((PR30//PR105)+PR11)  
 =3.18\*0.496/(0.496+10.5K)=0.15mV  
 Icharge=(0.15mV/3.18)\*(0.075/0.015)=0.236mA

ENCHG-2P	PRE_CHG	ENCHG	
0	1	1	Pre-charge
1	0	1	3S2P-Fast charge
0	0	1	3S3P-Fast charge
0	0	0	STOP CHARGE

**MSI CORPORATION**

**Battery Charger**

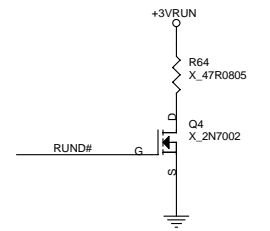
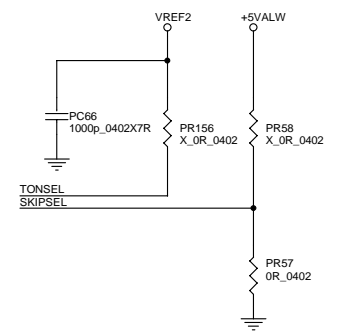
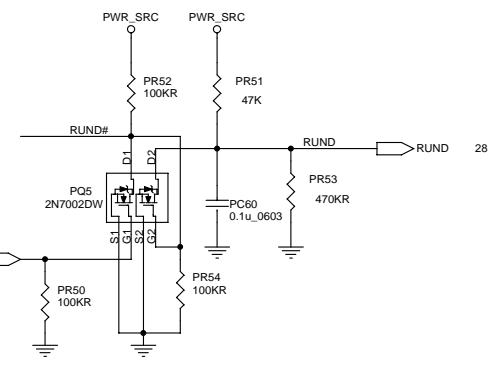
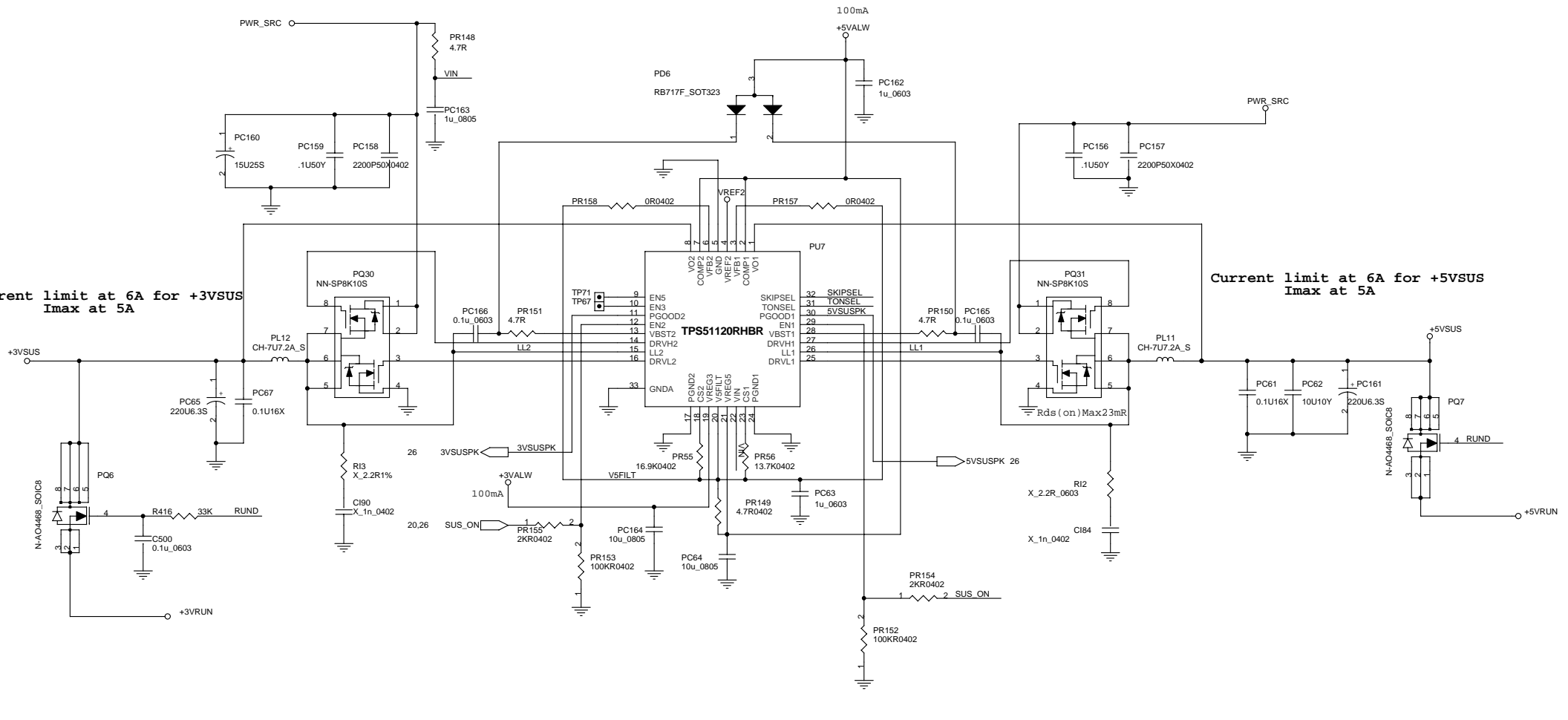
Title: **Battery Charger**

Size: Custom Document Number: **MS-16371** Rev: 0B

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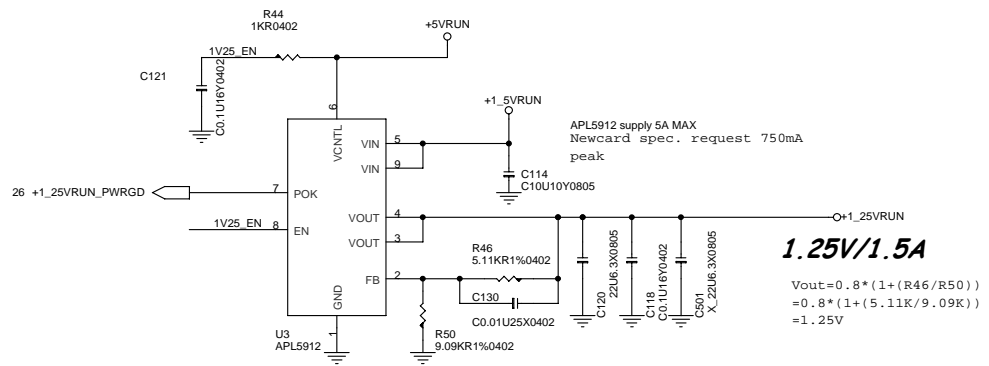
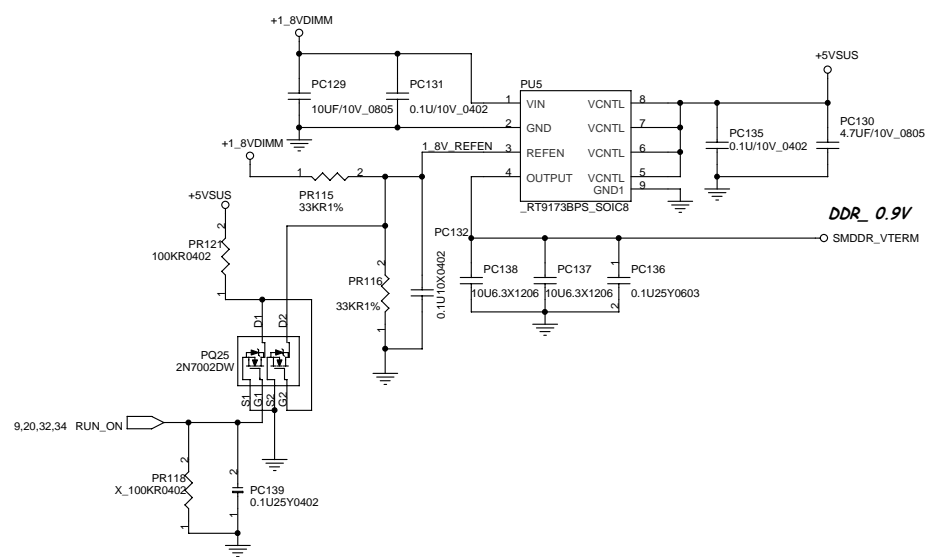
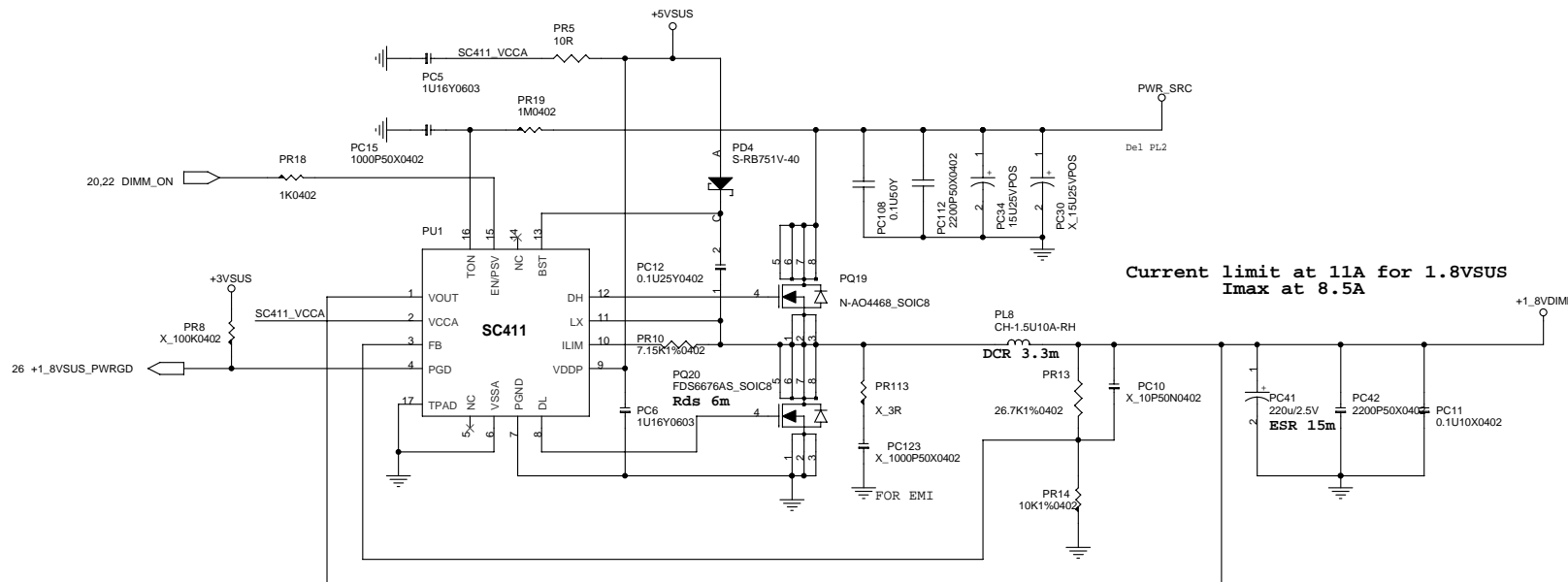
Current limit at 6A for +3VSUS  
I<sub>max</sub> at 5A

Current limit at 6A for +5VSUS  
I<sub>max</sub> at 5A

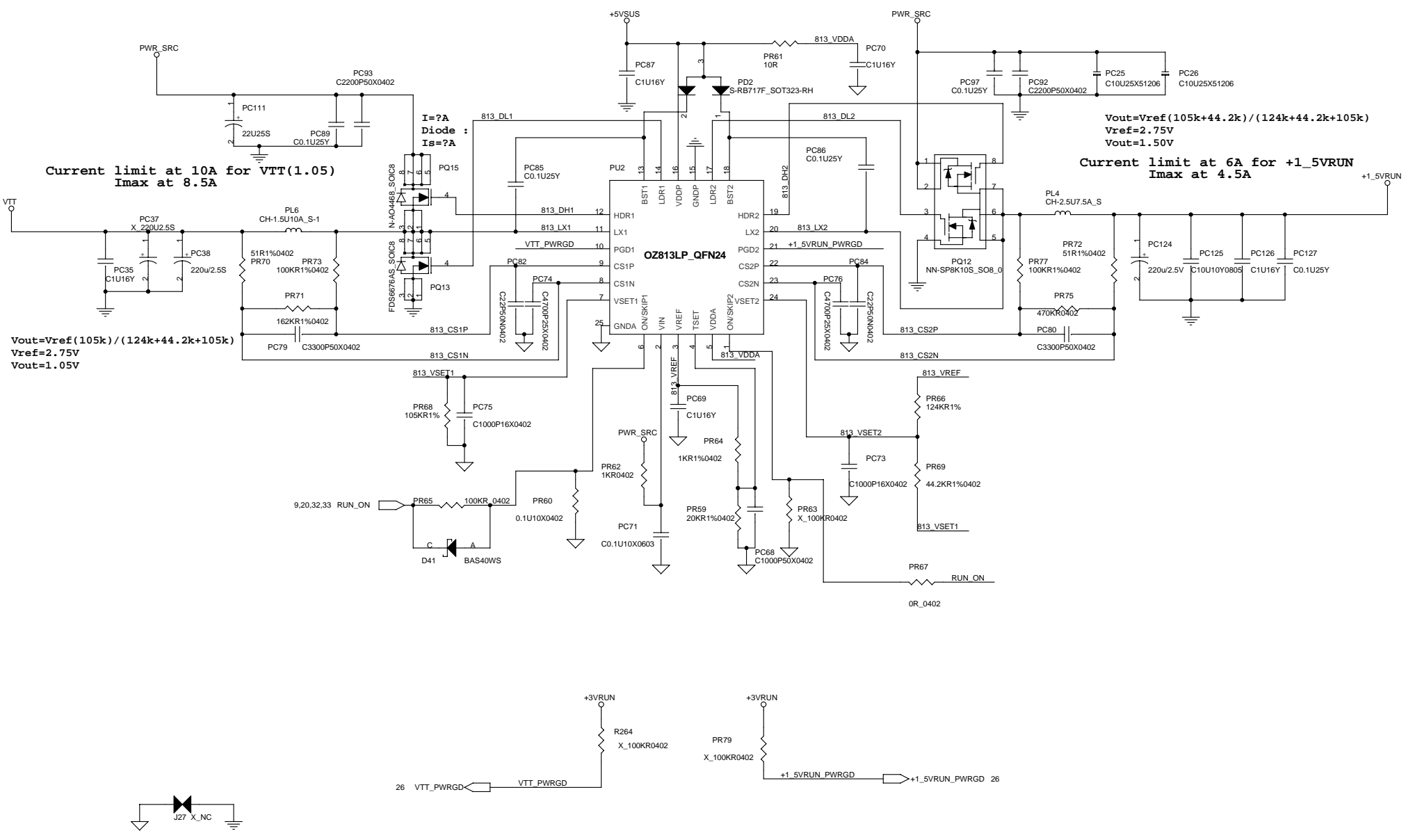


<b>MSI CORPORATION</b>		
Title	<b>SYSTEM POWER 3/5V</b>	
Size	Document Number	Rev
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<b>MSI CORPORATION</b>		
Title <b>DDR2 RAM POWER, +1.25V</b>		
Size	Document Number	Rev
Cus	<b>MS-16371</b>	0B
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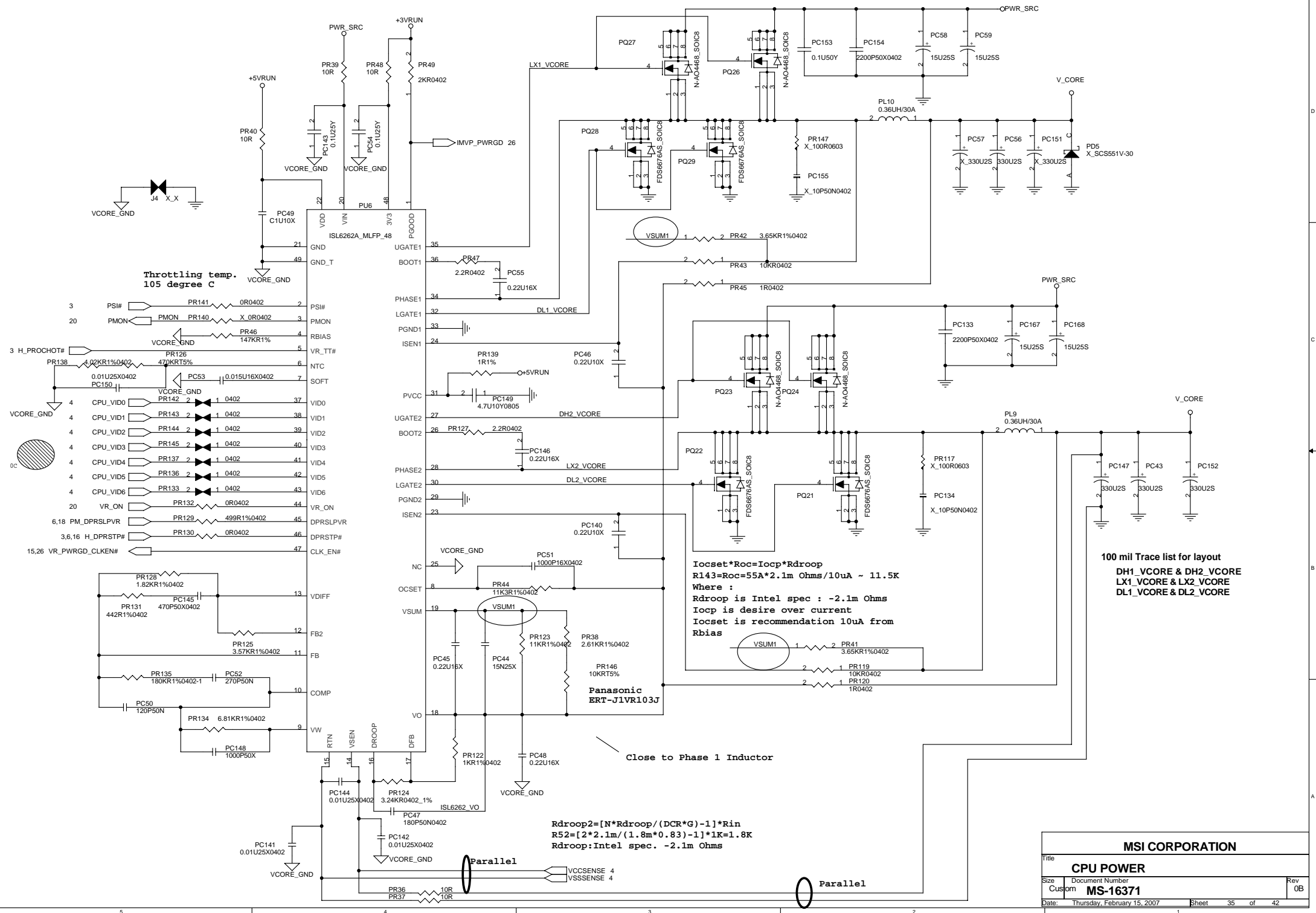
Current limit at 10A for VTT(1.05)  
Imax at 8.5A

$V_{out} = V_{ref} (105k + 44.2k) / (124k + 44.2k + 105k)$   
 $V_{ref} = 2.75V$   
 $V_{out} = 1.50V$

Current limit at 6A for +1.5V\_VRUN  
Imax at 4.5A

$V_{out} = V_{ref} (105k) / (124k + 44.2k + 105k)$   
 $V_{ref} = 2.75V$   
 $V_{out} = 1.05V$

<b>MSI CORPORATION</b>		
<b>+1.5V_VRUN , VTT POWER</b>		
Title		
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Throttling temp.  
105 degree c

$I_{ocset} * R_{oc} = I_{ocp} * R_{droop}$   
 $R143 = R_{oc} = 55A * 2.1m \text{ Ohms} / 10uA \sim 11.5K$   
 Where :  
 $R_{droop}$  is Intel spec : -2.1m Ohms  
 $I_{ocp}$  is desire over current  
 $I_{ocset}$  is recommendation 10uA from Rbias

$R_{droop2} = [N * R_{droop} / (DCR * G) - 1] * R_{in}$   
 $R52 = [2 * 2.1m / (1.8m * 0.83) - 1] * 1K = 1.8K$   
 $R_{droop} = \text{Intel spec.} \sim 2.1m \text{ Ohms}$

100 mil Trace list for layout  
 DH1\_VCORE & DH2\_VCORE  
 LX1\_VCORE & LX2\_VCORE  
 DL1\_VCORE & DL2\_VCORE

Close to Phase 1 Inductor

Parallell

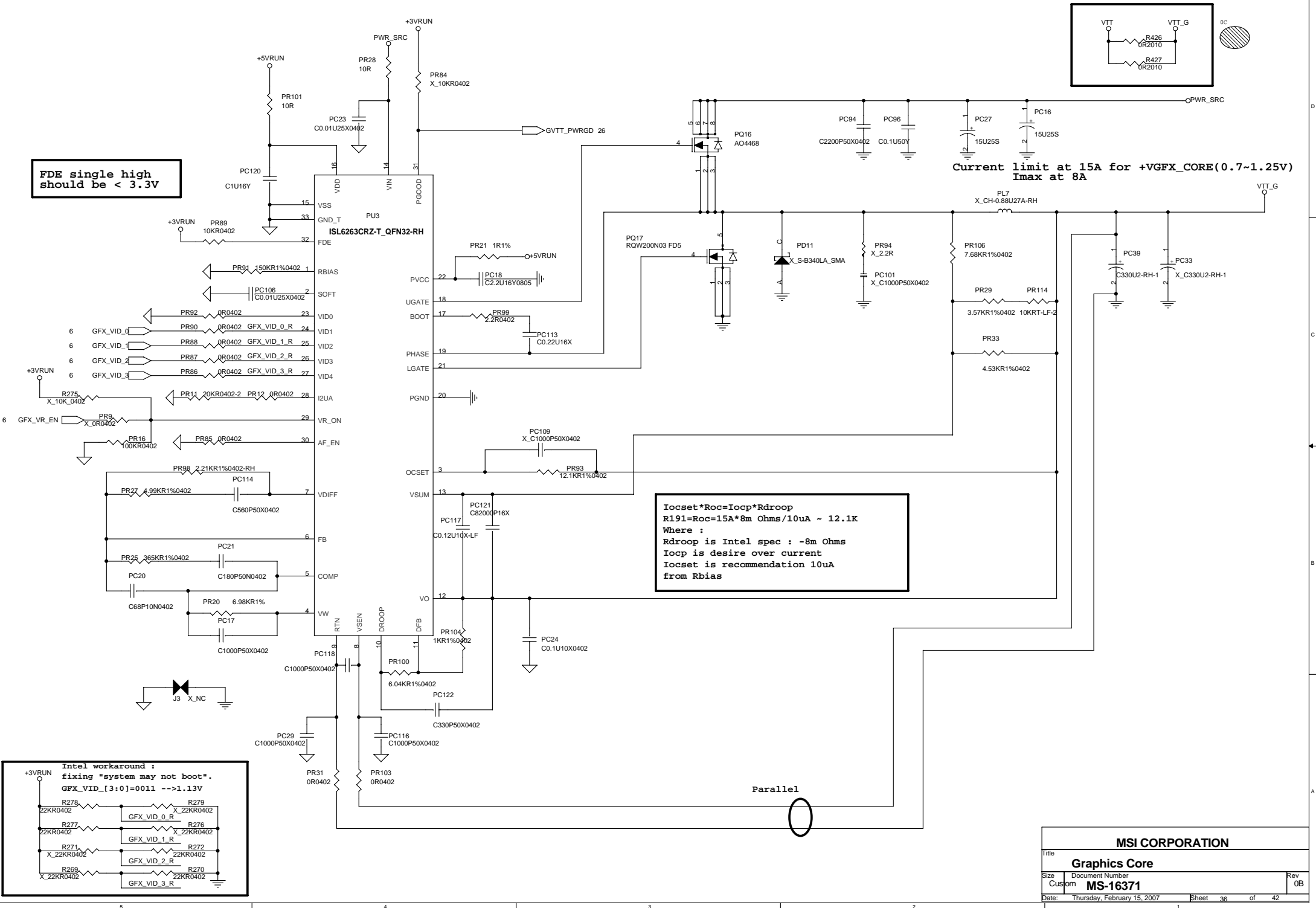
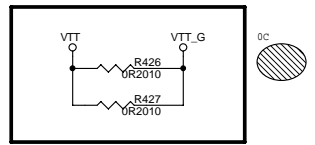
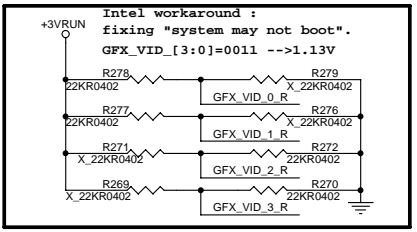
Parallell

<b>MSI CORPORATION</b>		
Title	<b>CPU POWER</b>	
Size	Document Number	Rev
Custom	<b>MS-16371</b>	0B
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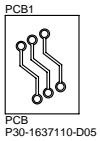
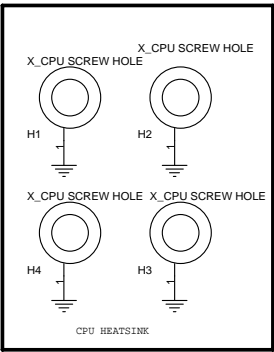
FDE single high should be < 3.3V

Current limit at 15A for +VGFX\_CORE(0.7~1.25V)  
I<sub>max</sub> at 8A

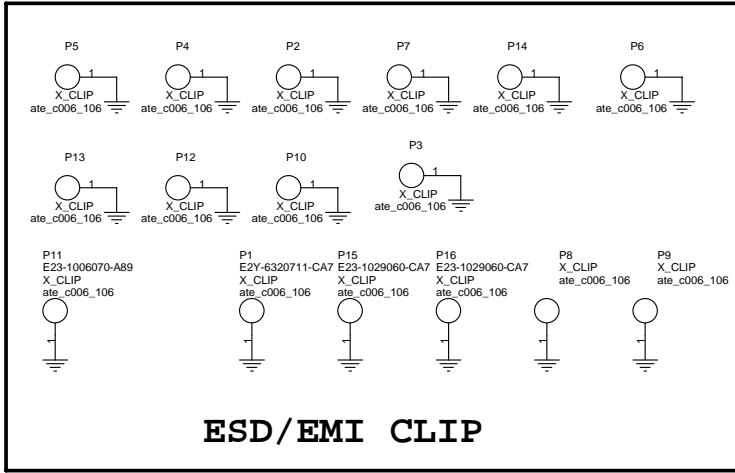
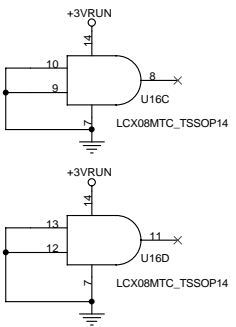
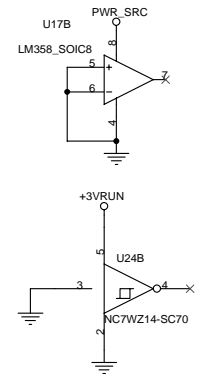
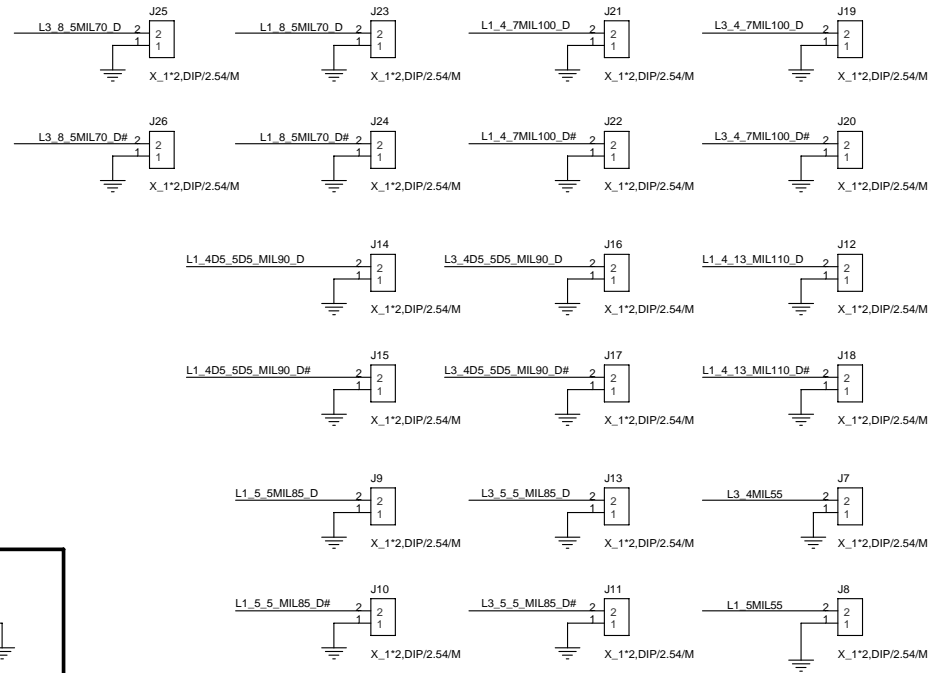
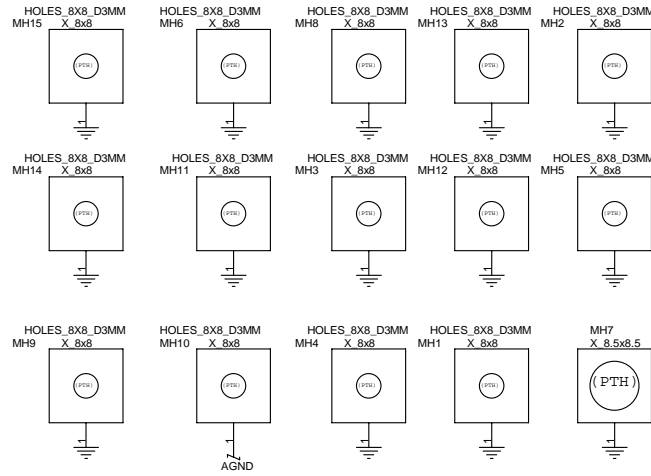
$I_{ocset} * R_{oc} = I_{ocp} * R_{droop}$   
 $R_{191} = R_{oc} = 15A * 8m\ Ohms / 10\ \mu A \sim 12.1K$   
 Where :  
 R<sub>droop</sub> is Intel spec : -8m Ohms  
 I<sub>ocp</sub> is desire over current  
 I<sub>ocset</sub> is recommendation 10uA  
 from R<sub>bias</sub>



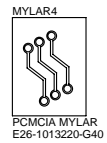
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Title	<b>Graphics Core</b>	
Size	Document Number	Rev
Custom	<b>MS-16371</b>	0B
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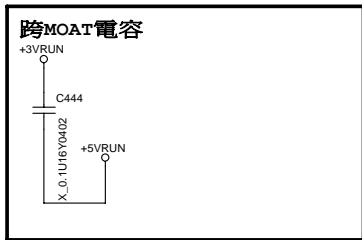
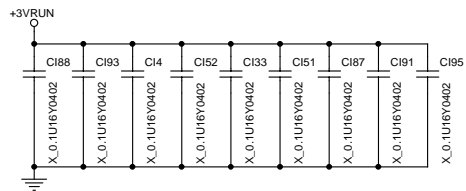
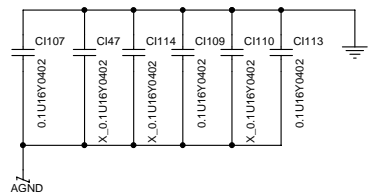
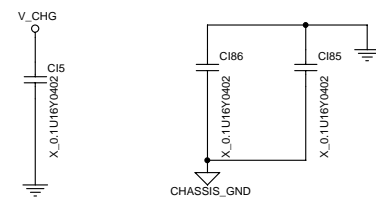
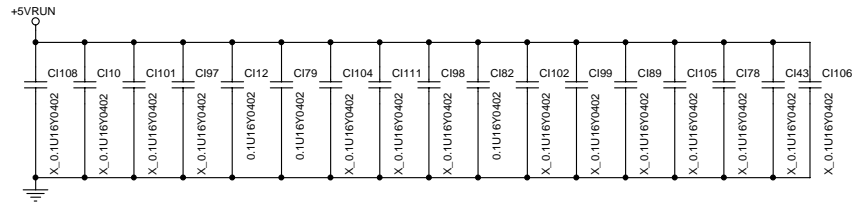
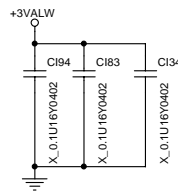
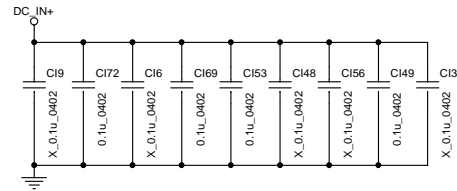
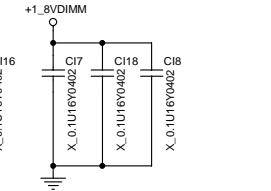
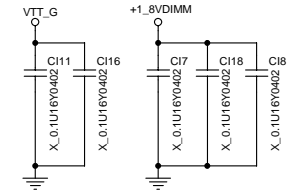
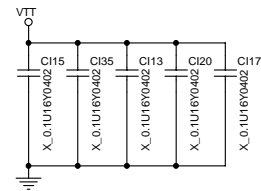
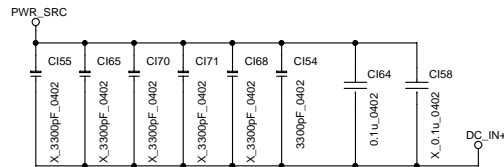
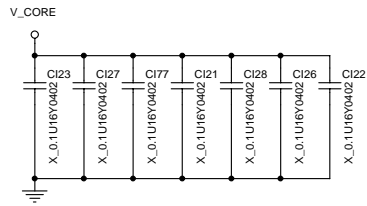
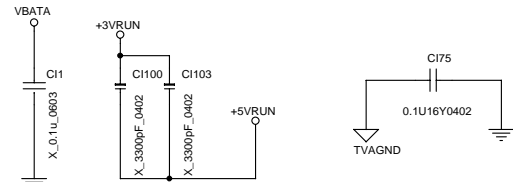
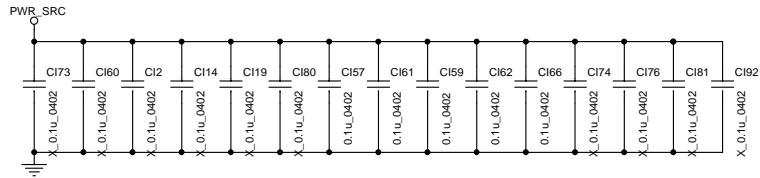
P30-1637110-H73, 瀚宇博德  
 P30-1637110-Y34, 元茂  
 P30-1637110-D05, 昆穎 (定額大陸)



**ESD/EMI CLIP**

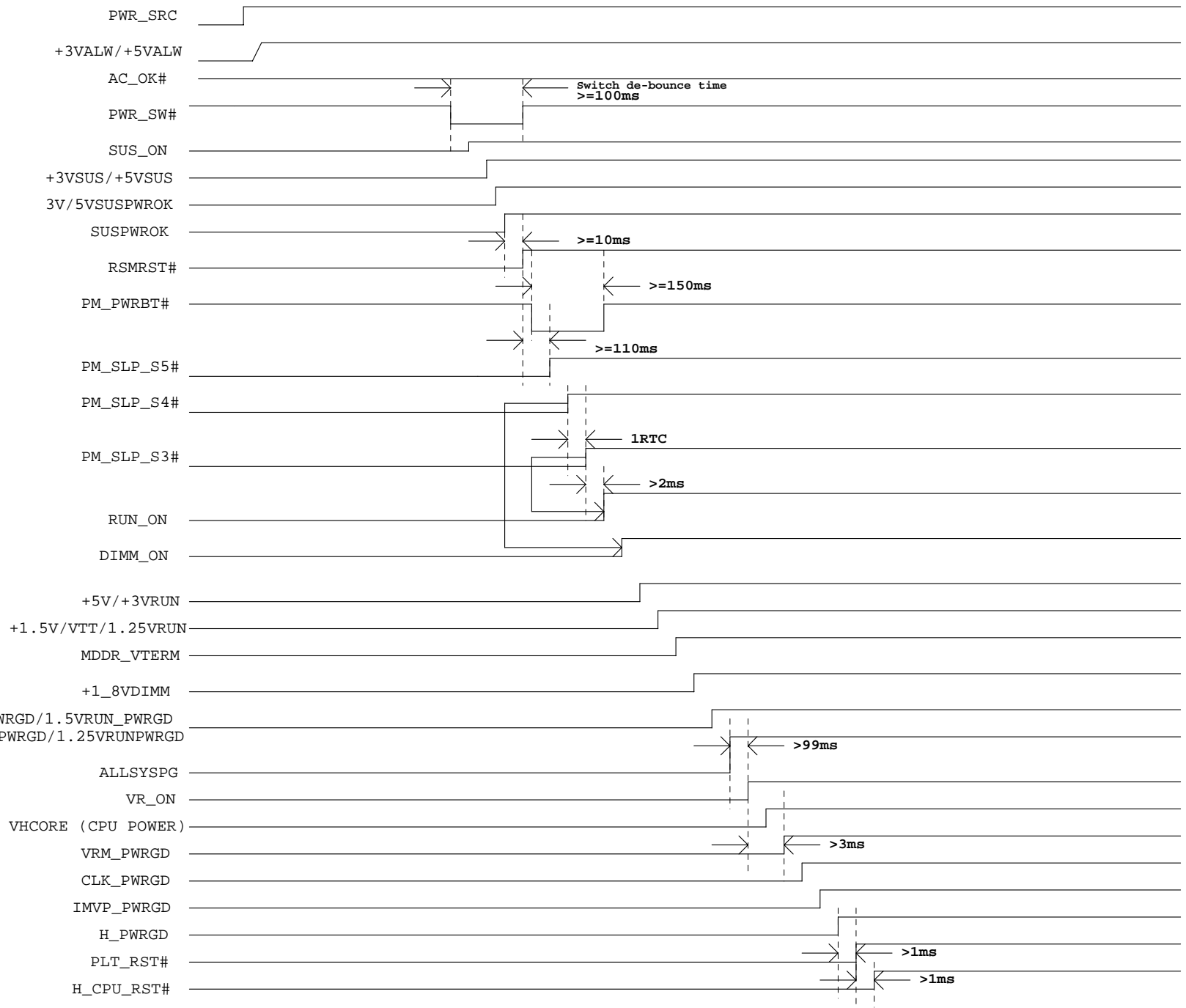


<b>MSI CORPORATION</b>		
Title	<b>Screw</b>	
Size	Document Number	Rev
Cusom	<b>MS-16371</b>	0B
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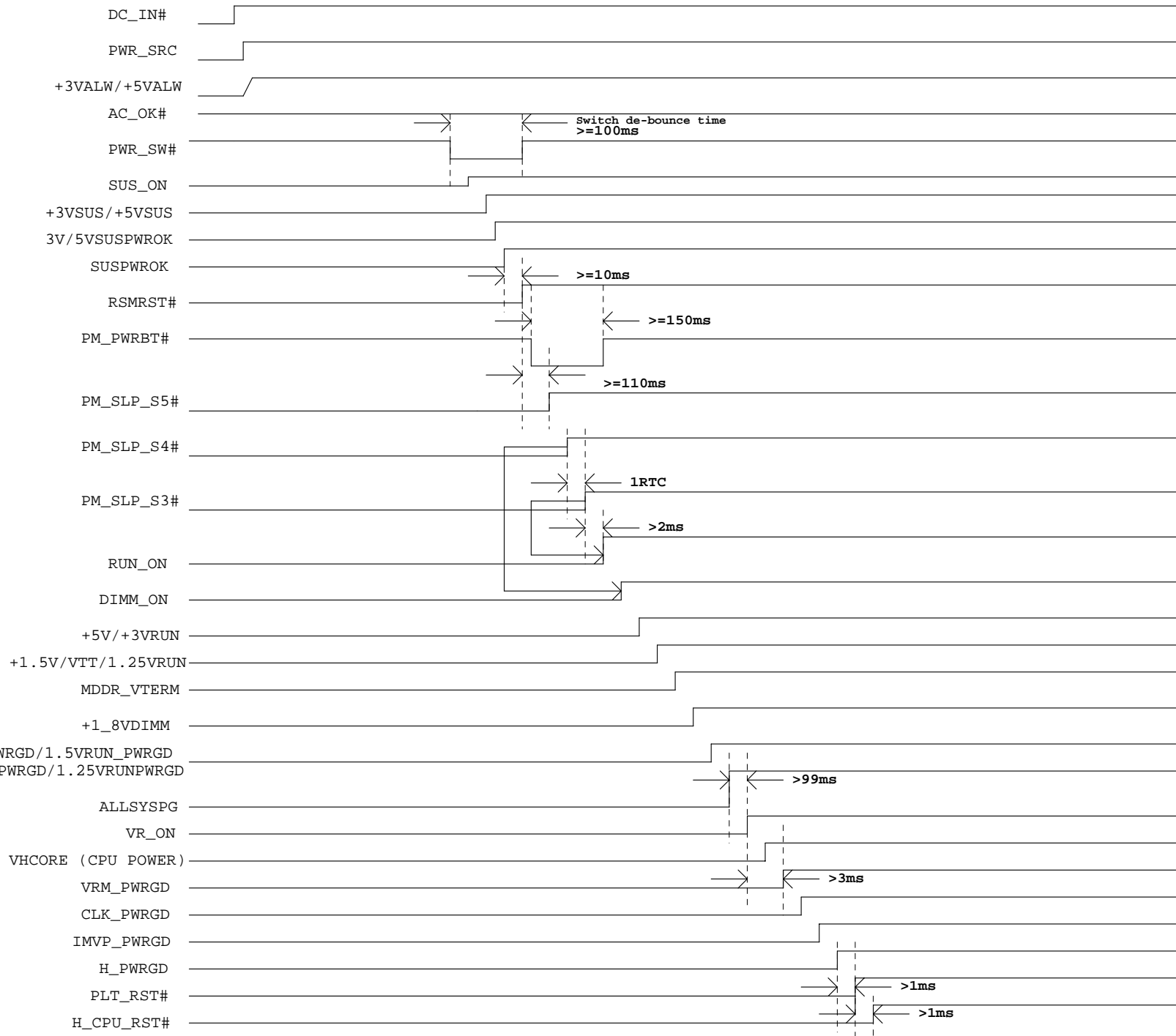


<b>MSI CORPORATION</b>		
Title	<b>EMI</b>	
Size	Document Number	Rev
Custom	<b>MS-16371</b>	0B
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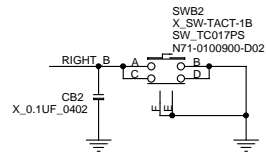
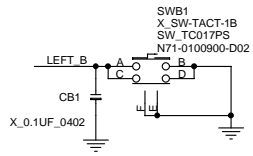
# SANTA ROSA System Power on Sequence Battery MODE (S5->S0)



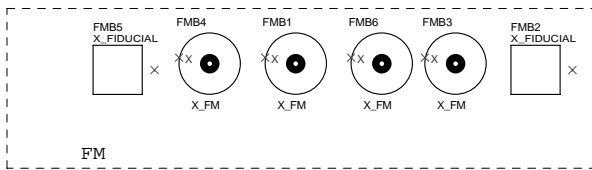
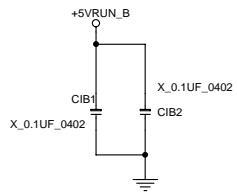
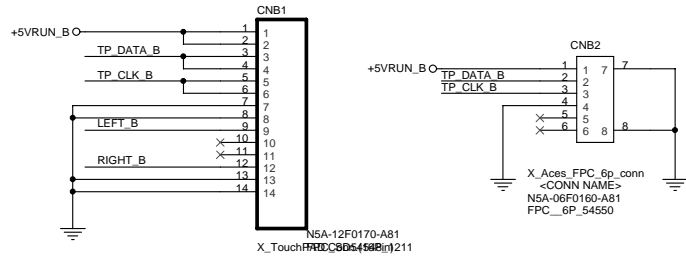
# SANTA ROSA System Power on Sequence (G3->S0)



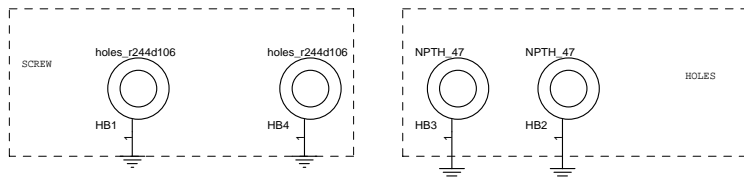




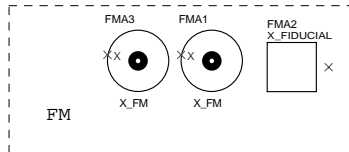
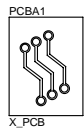
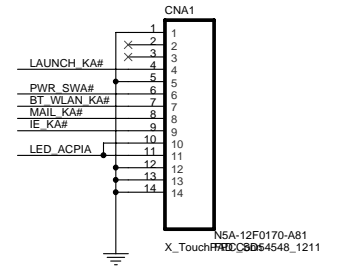
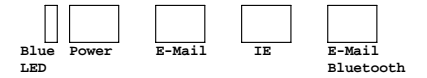
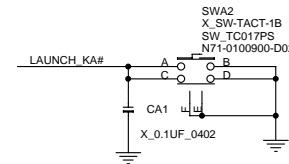
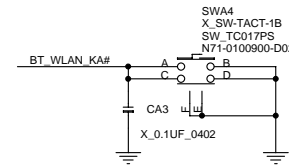
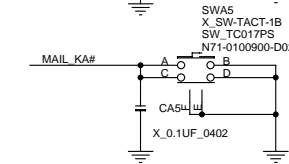
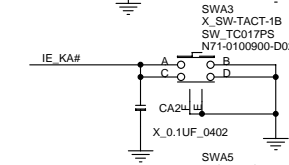
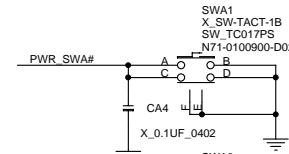
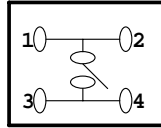
For TM61P-307 pin define



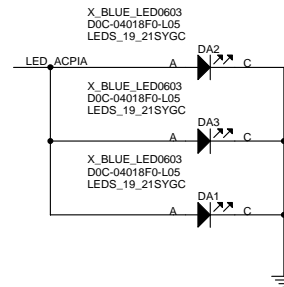
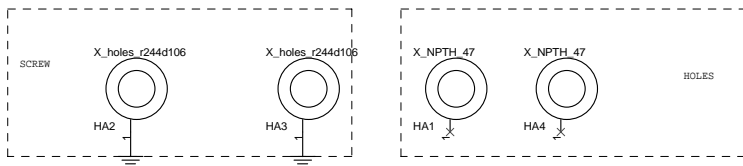
P30-1637B10-H73,瀚宇博德  
 P30-1637B10-Y34,元茂  
 P30-1637B10-D05,昆穎(定穎大陸)



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