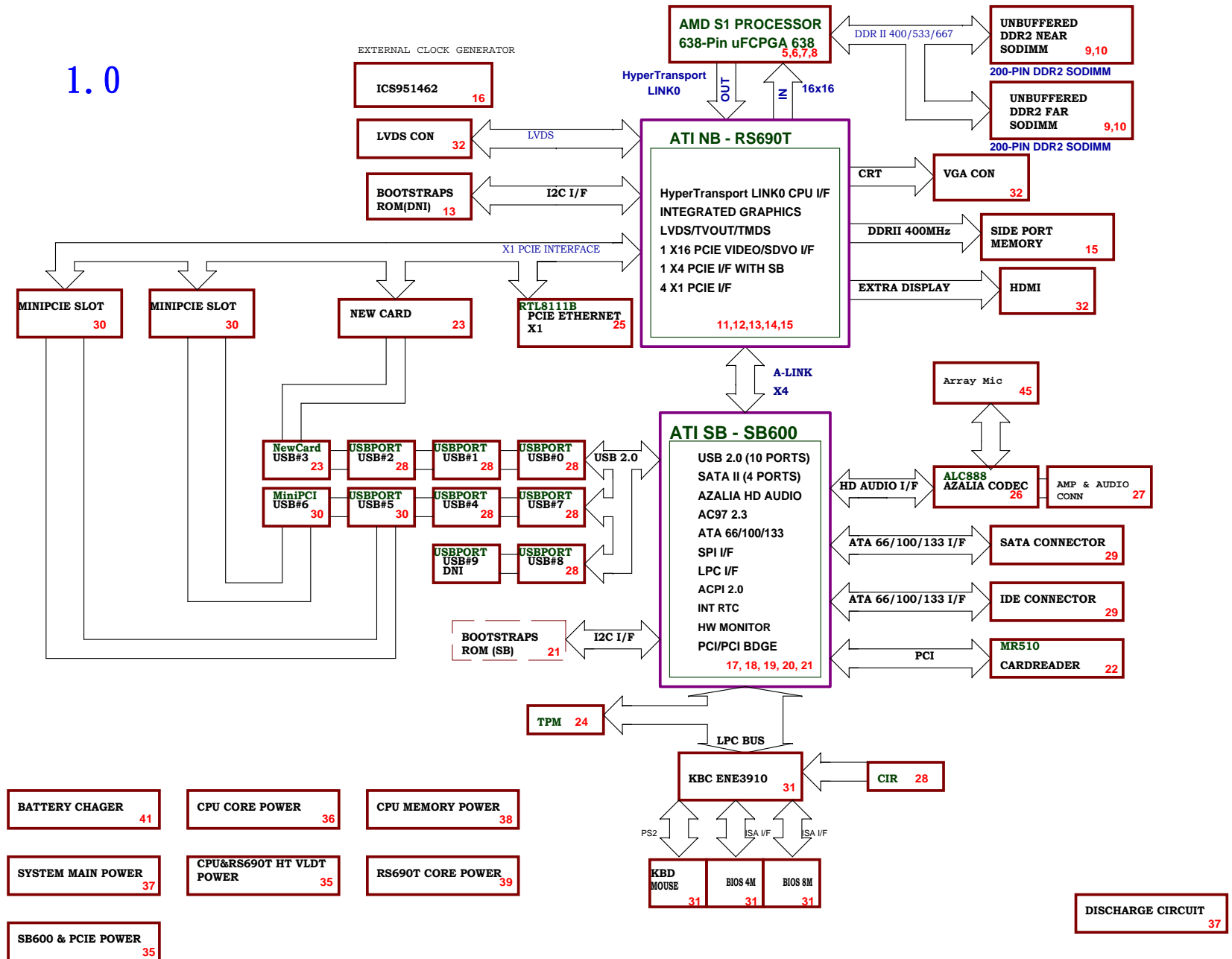
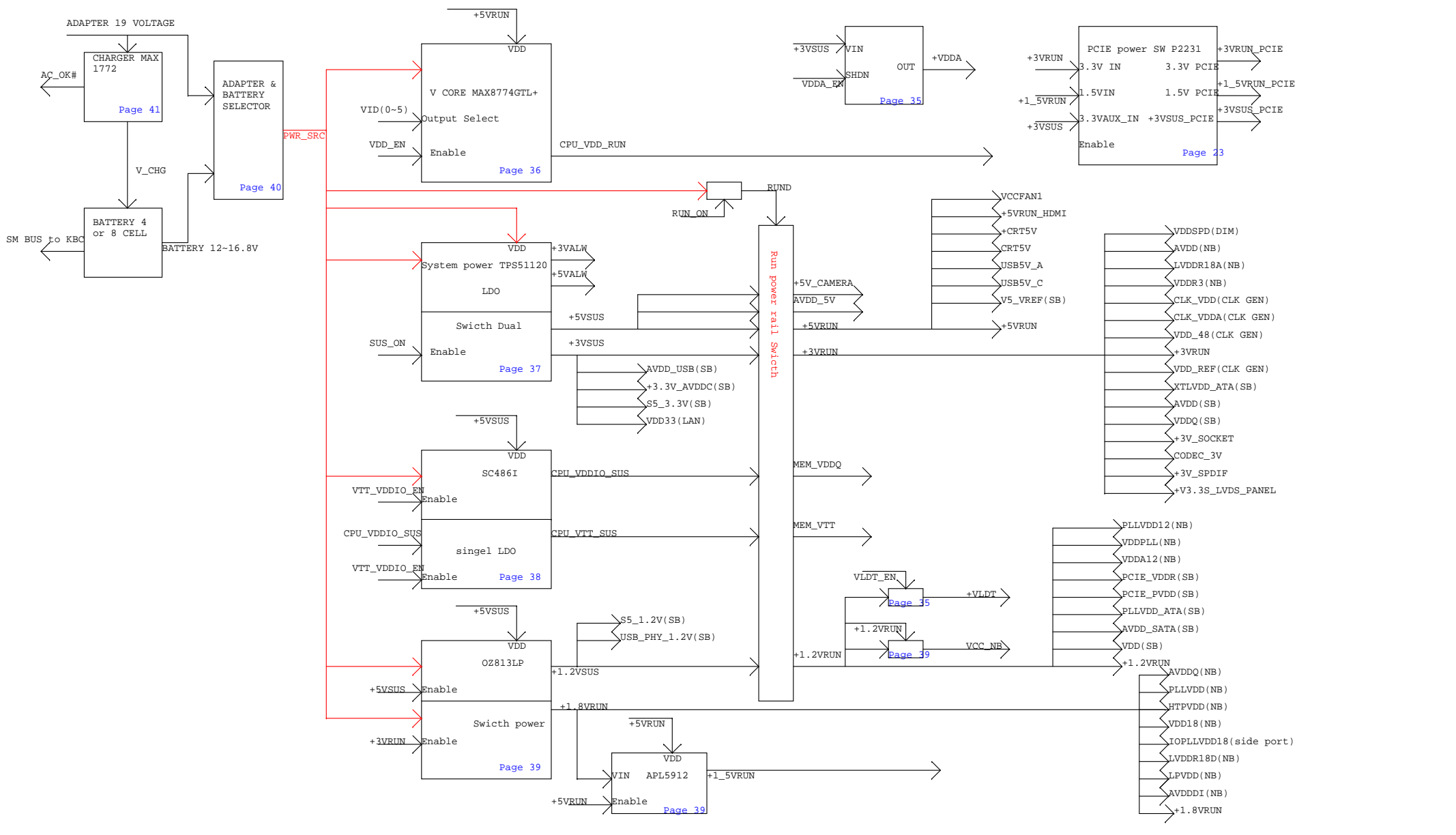
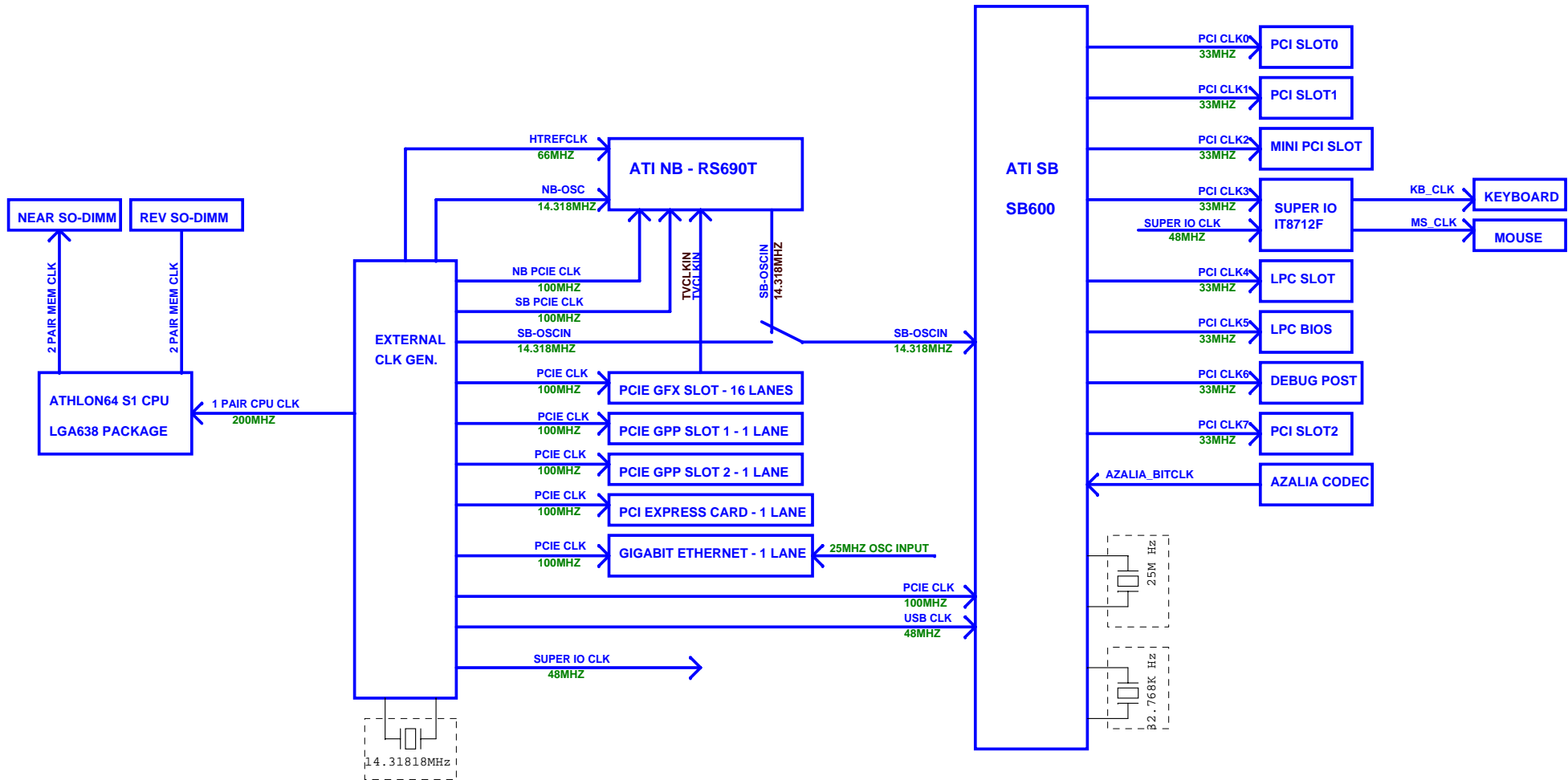


1.0



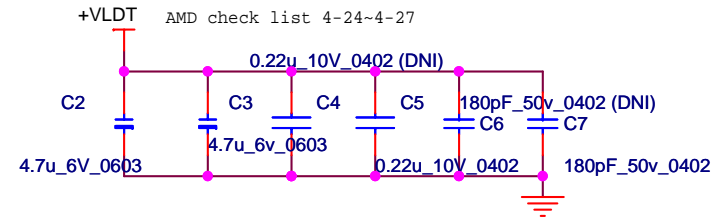
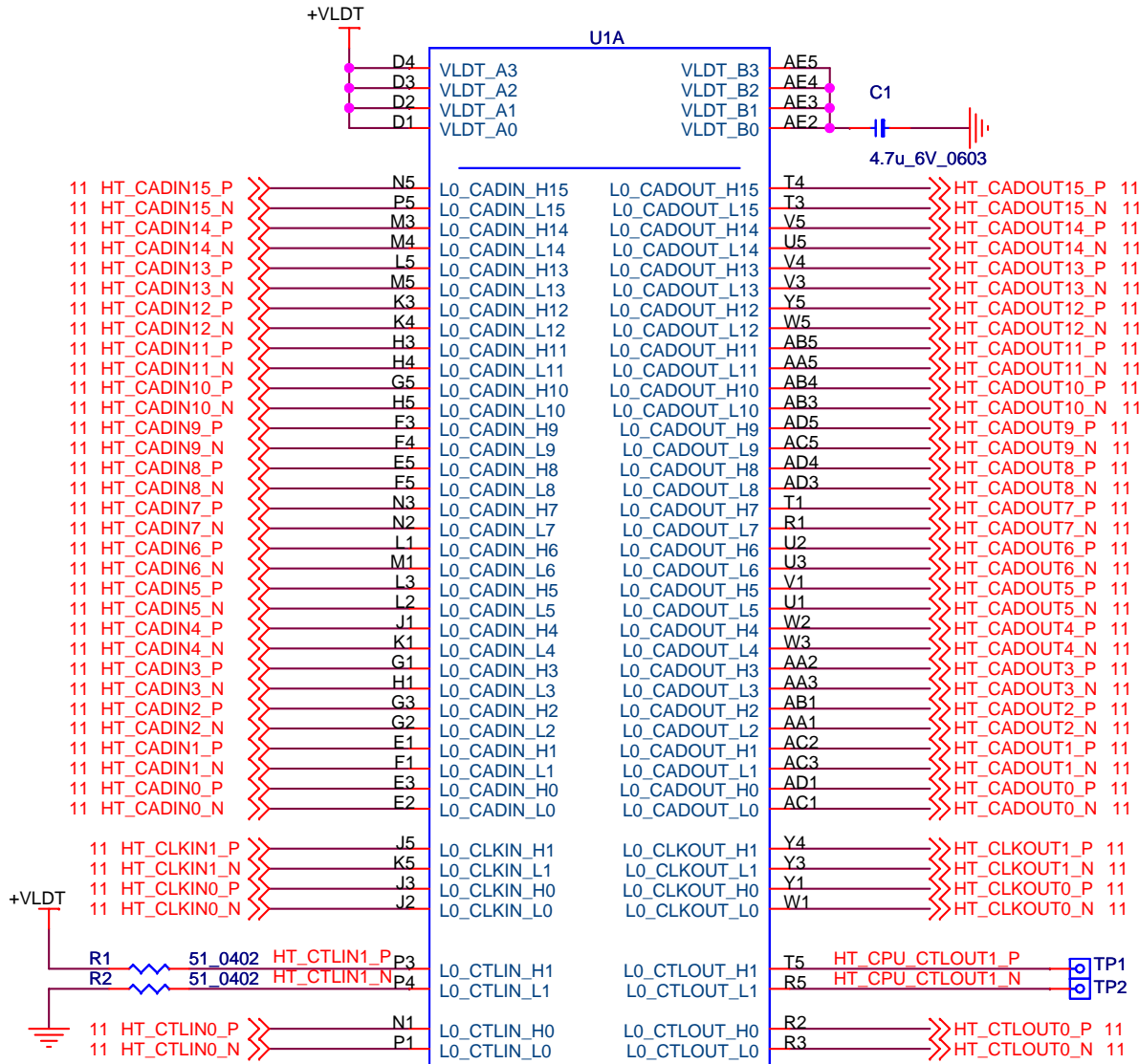






PROCESSOR HYPERTRANSPORT INTERFACE


VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



LAYOUT: Place bypass cap on topside of board
 NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
 PLACE CLOSE TO VLDT0 POWER PINS

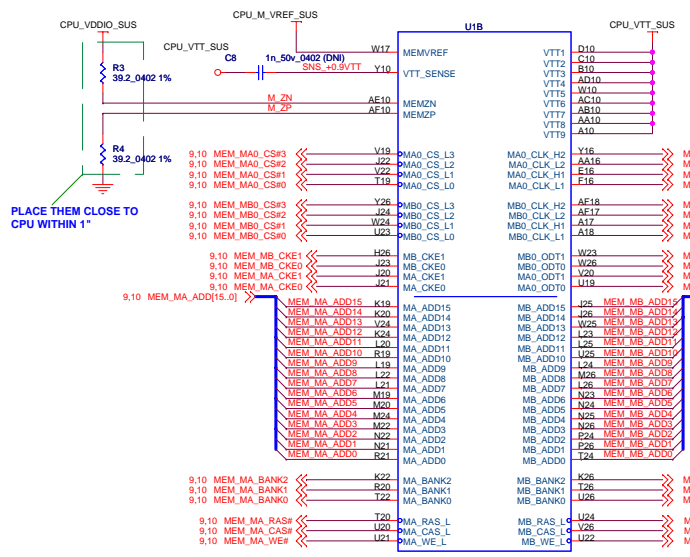


Athlon 64 S1 Processor Socket

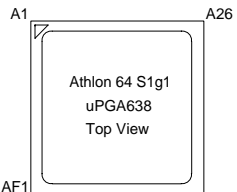
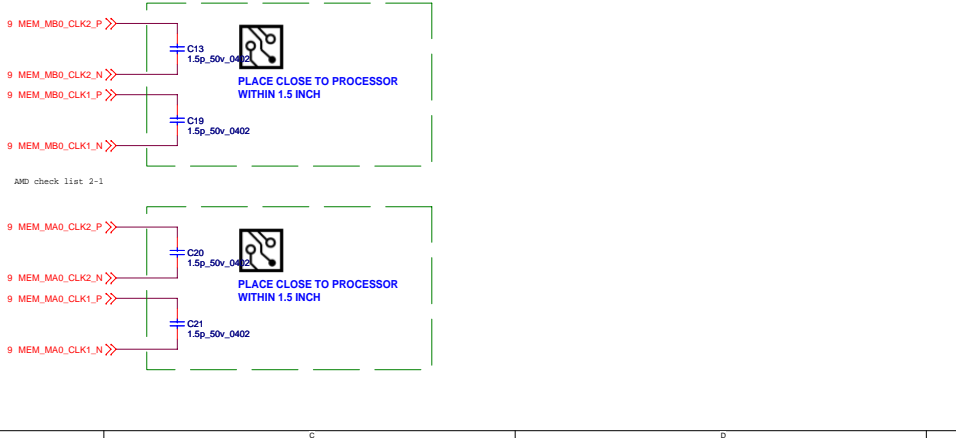
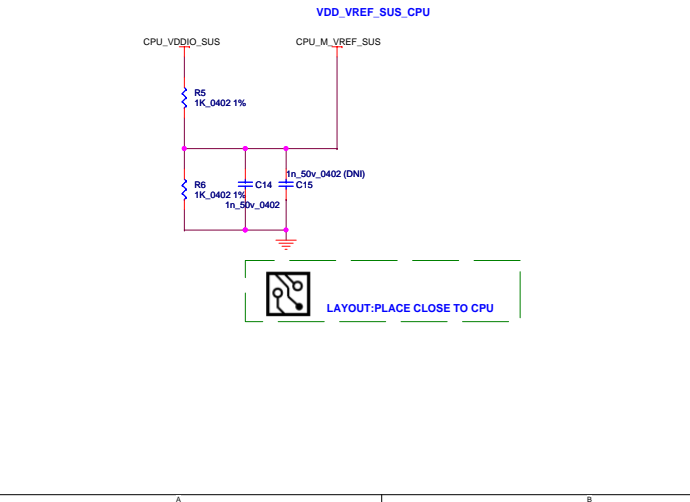
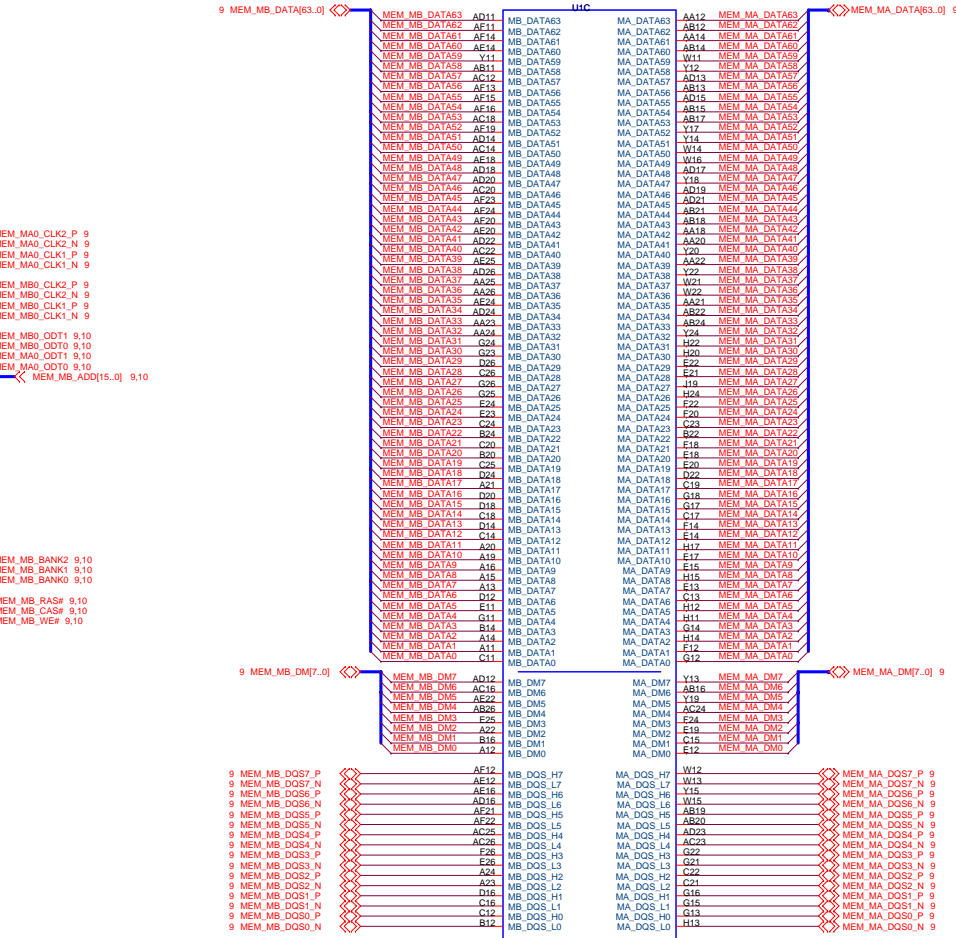
 Link to the Future		MICRO-STAR INT'L CO.,LTD.	
SOCKET S1 HT I/F			
Size	Document Number		Rev
Custom	MS-12221		1.0
Date:	Thursday, February 01, 2007	Sheet	5 of 45

Processor DDR2 Memory Interface

VDD VTT SUS, CPU IS CONNECTED TO THE VDD VTT SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE.



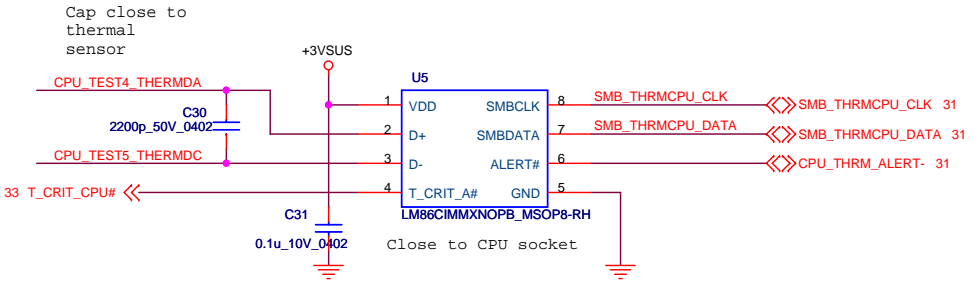
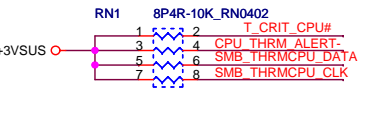
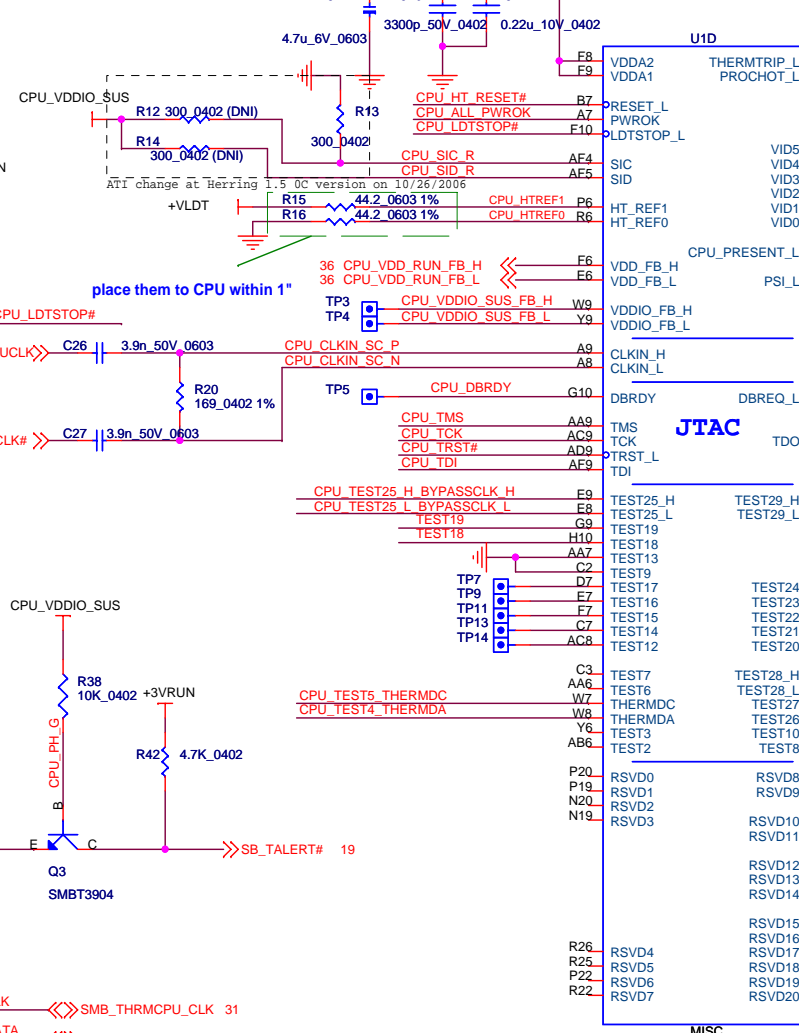
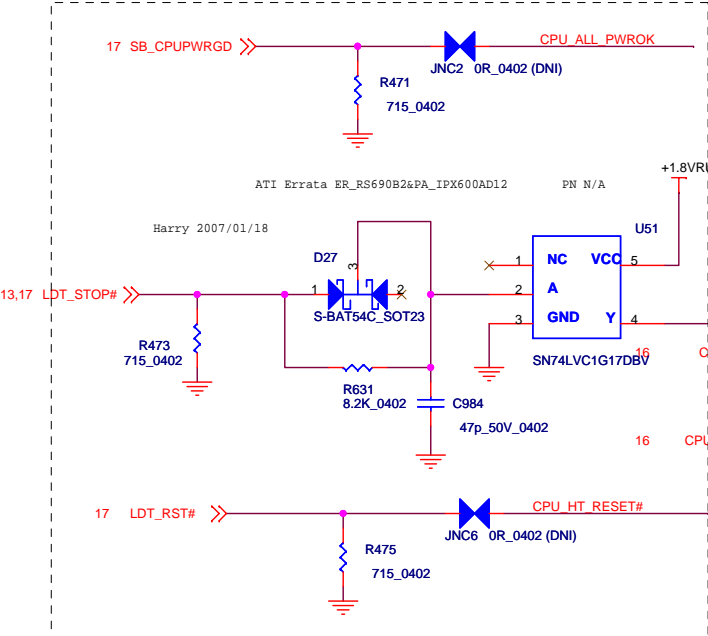
PLACE THEM CLOSE TO CPU WITHIN 1"



LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

ATHLON Control and Debug

CPU_VDDA_2.5_RUN



Component	Value	Notes
TEST26	R225 300_0402	
CPU_DBRDY#	R28 510_0402 (DNI)	
CPU_TMS	R29 510_0402 (DNI)	
CPU_TCK	R30 510_0402 (DNI)	
CPU_TRST#	R31 510_0402 (DNI)	
CPU_TDI	R33 510_0402 (DNI)	
CPU_PRESENT#	R35 1K_0402	
CPU_TEST25_H BYPASSCLK_H	R36 510_0402	
CPU_TEST25_L BYPASSCLK_L	R39 510_0402	
TEST18	R26 300_0402	
TEST19	R27 300_0402	
TEST21	R28 300_0402	

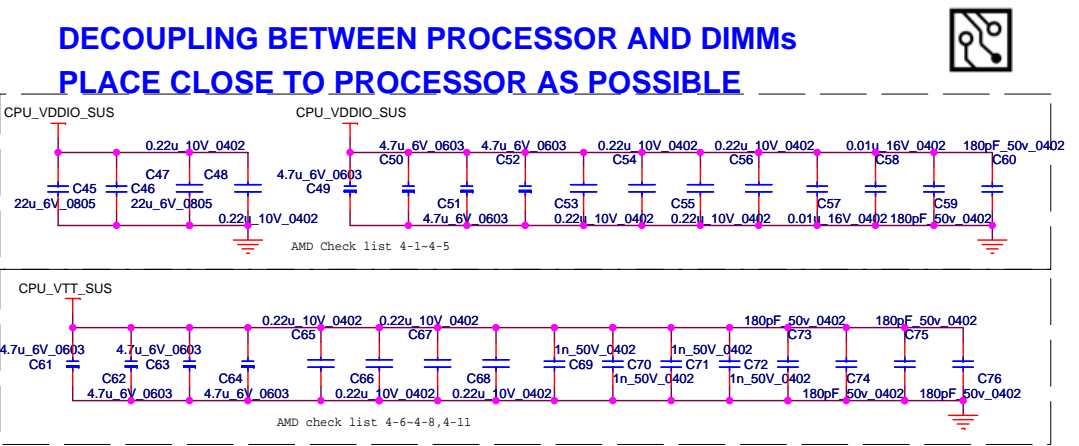
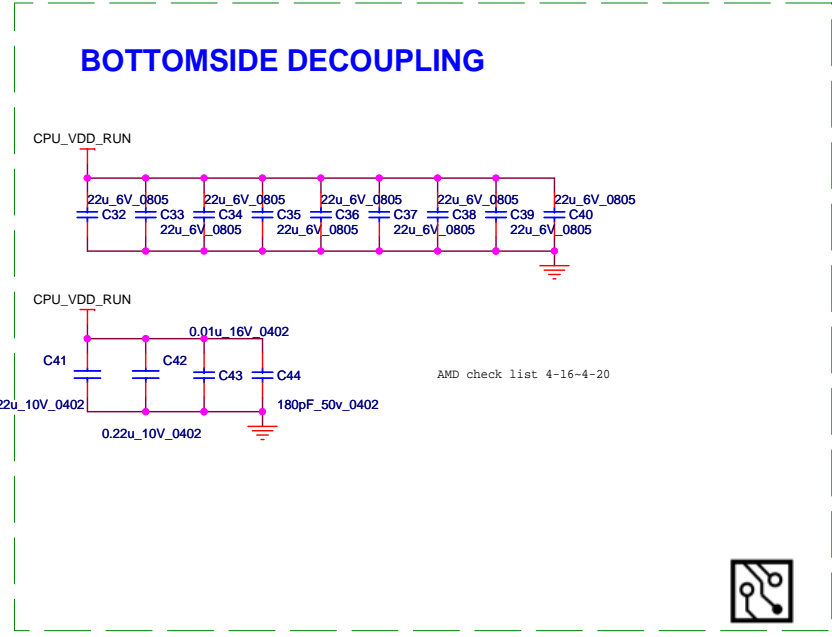
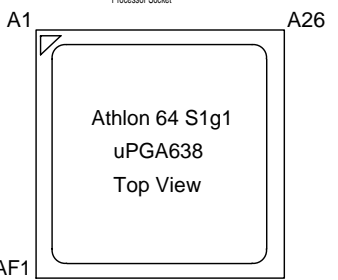
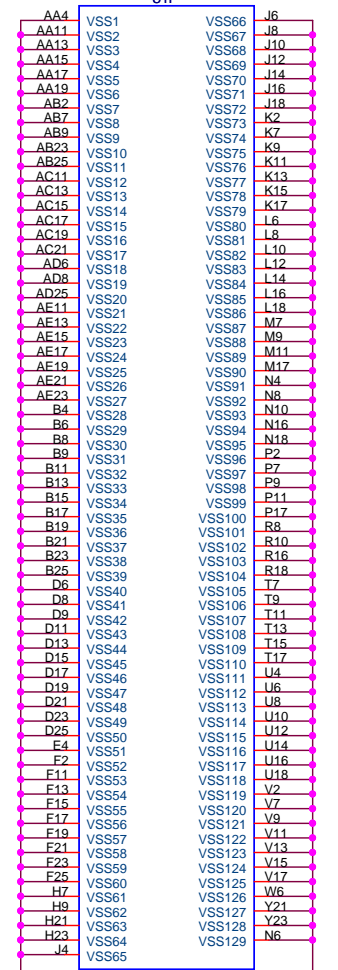
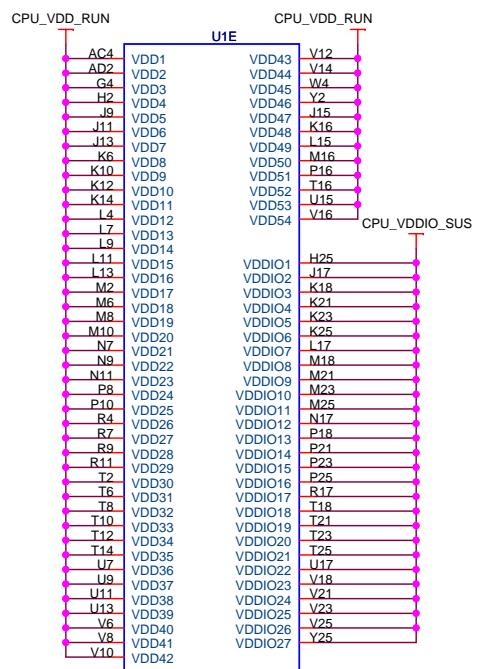
Harry 10/02 ERRATA#133

MSI MICRO-STAR INT'L CO.,LTD.

Title: **SOCKET S1 CTRL**

Size B Document Number: **MS-12221** Rev 1.0

Date: Thursday, February 01, 2007 Sheet 7 of 45



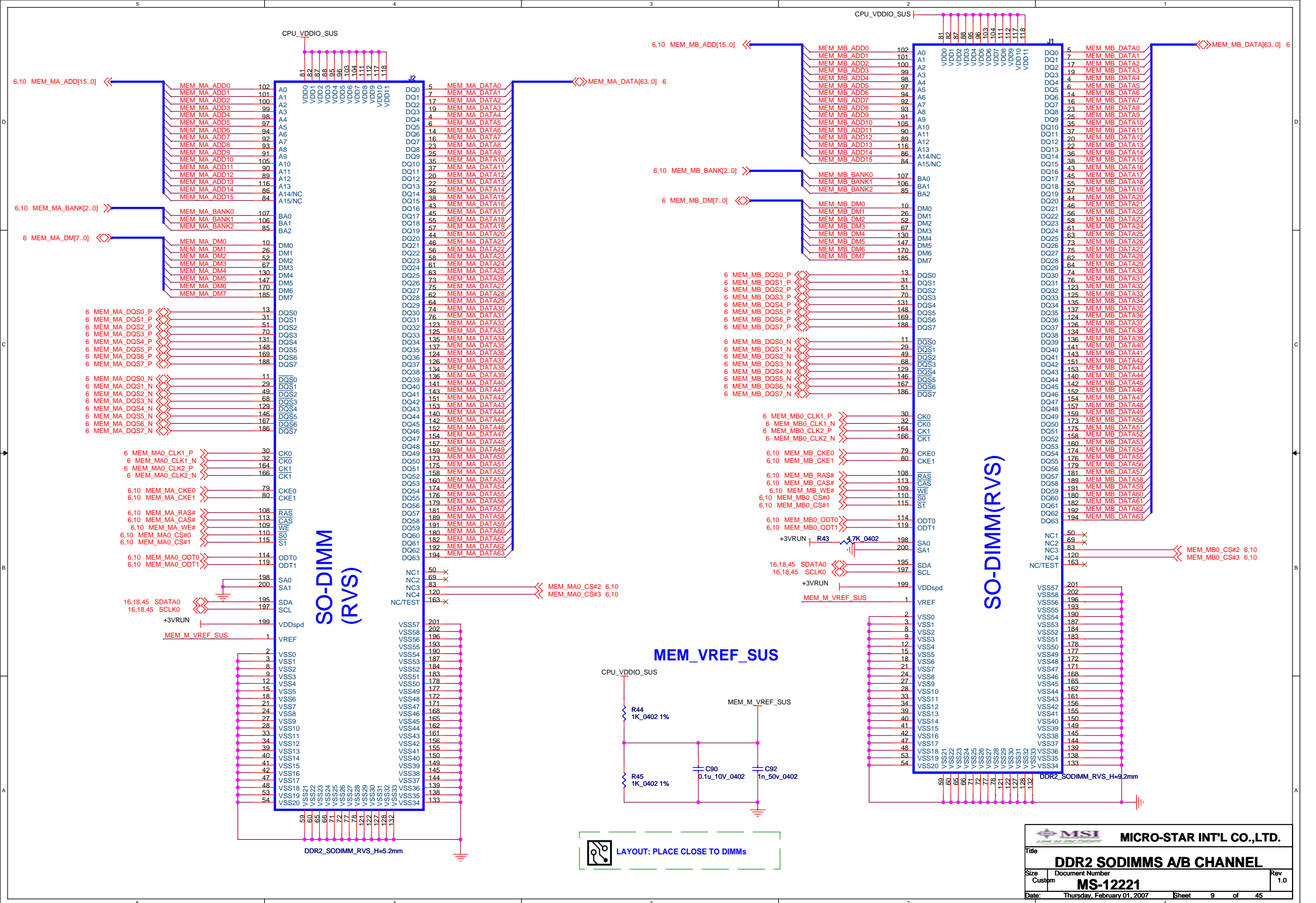
PROCESSOR POWER AND GROUND

MSI MICRO-STAR INT'L CO.,LTD.

Title: **SOCKET S1 PWR & GND**

Size B Document Number: **MS-12221** Rev 1.0

Date: Thursday, February 01, 2007 Sheet 8 of 45



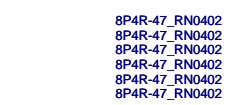
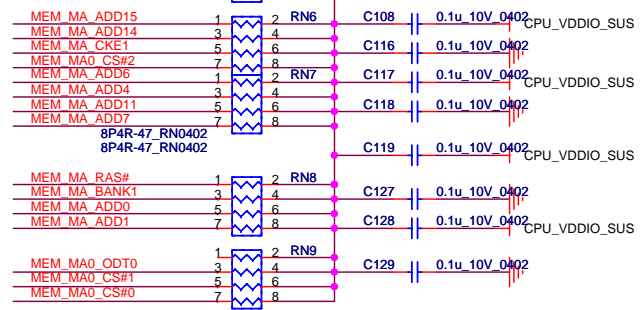
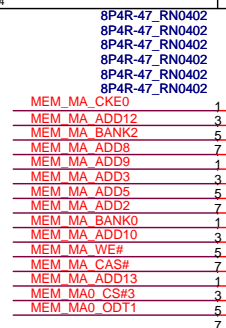
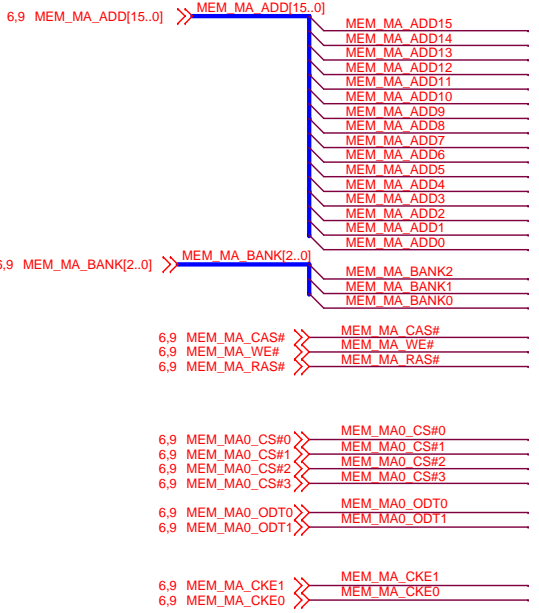
LAYOUT: PLACE CLOSE TO DIMMS

MSI MICRO-STAR INT'L CO.,LTD.

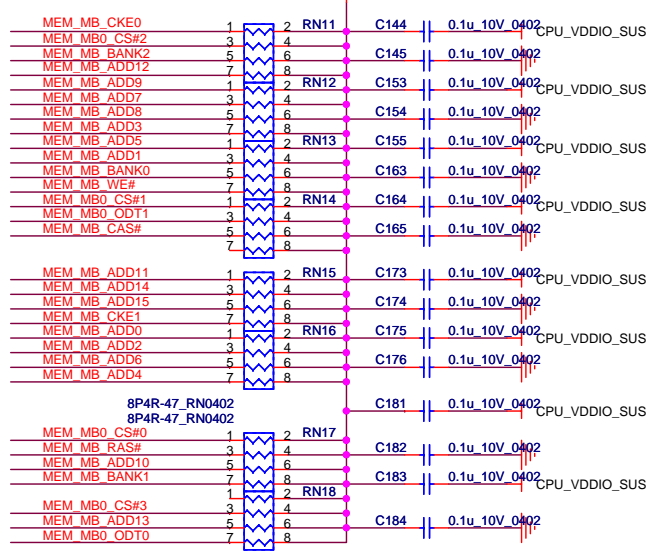
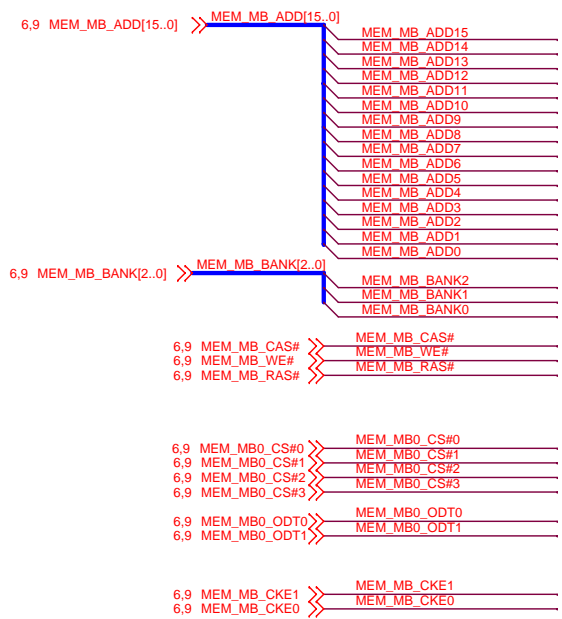
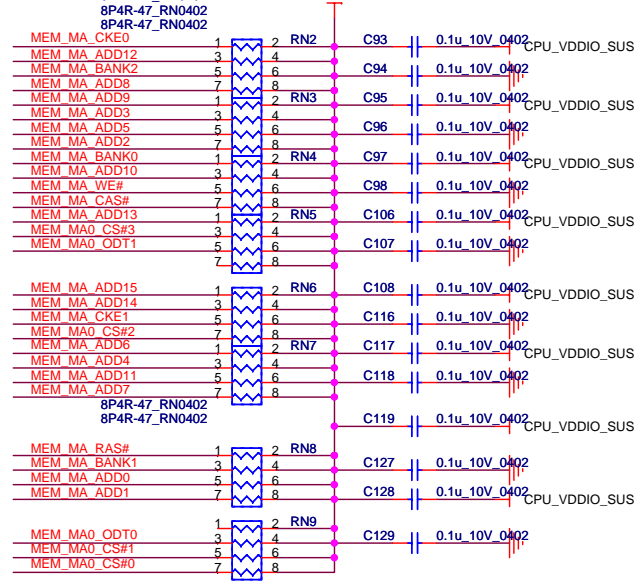
Title: **DDR2 SODIMMS A/B CHANNEL**

Size: Custom Document Number: **MS-12221** Rev: 1.0

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CPU_VTT_SUS



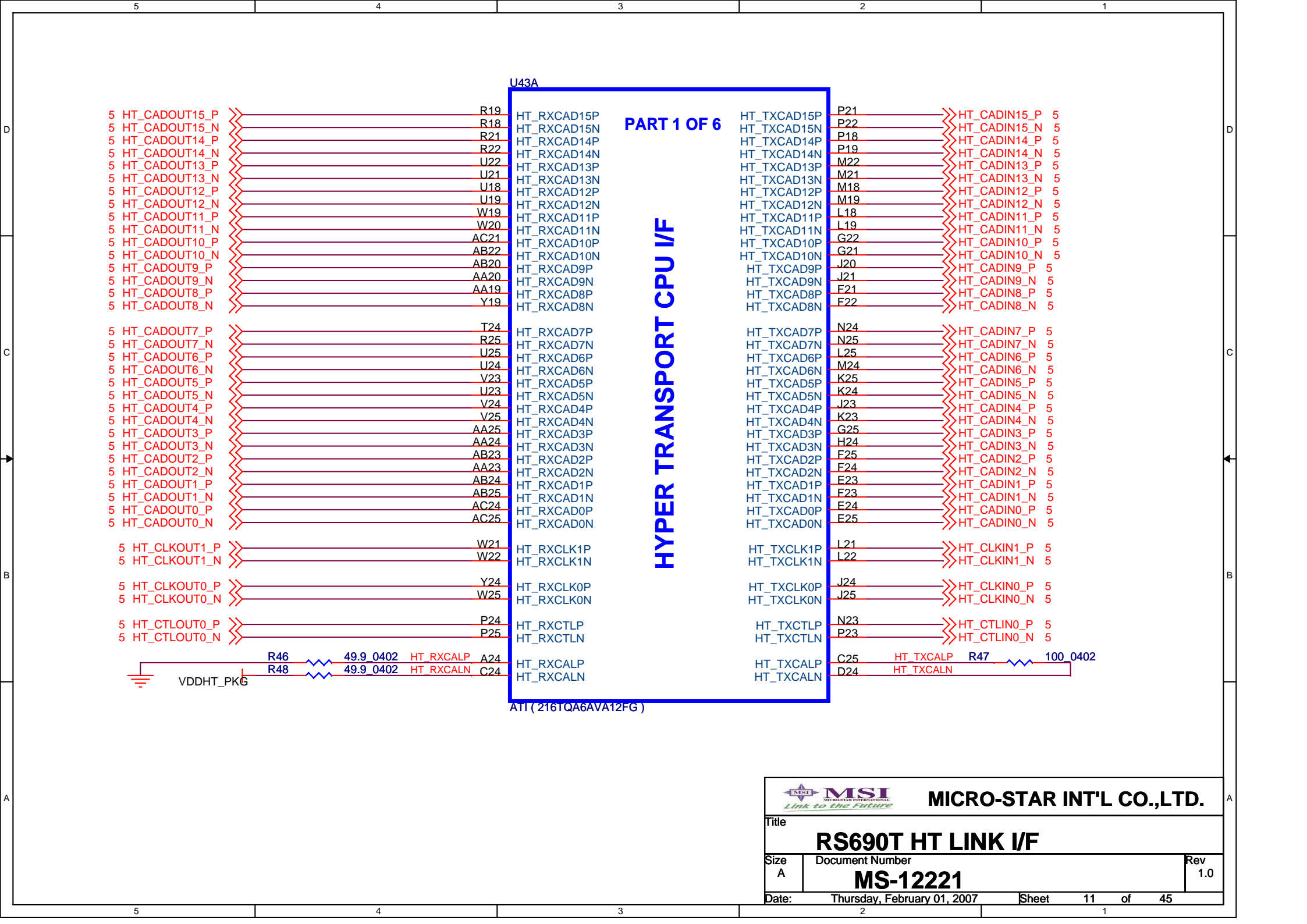
CPU_VTT_SUS

MSI
MICRO-STAR INT'L CO.,LTD.

Title: **DDR2 SODIMMS TERMINATIONS**

Size: Custom Document Number: **MS-12221** Rev: 1.0

Date: Thursday, February 01, 2007 Sheet 10 of 45




PART 1 OF 6

HYPER TRANSPORT CPU I/F

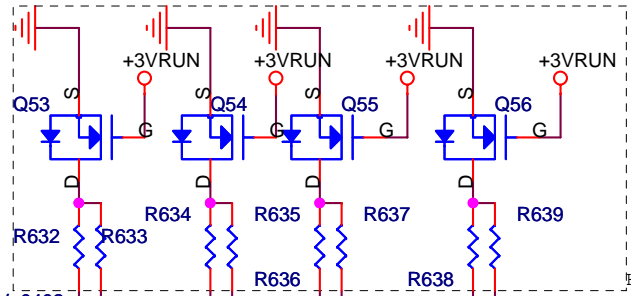
U43A

ATI (216TQA6AVA12FG)

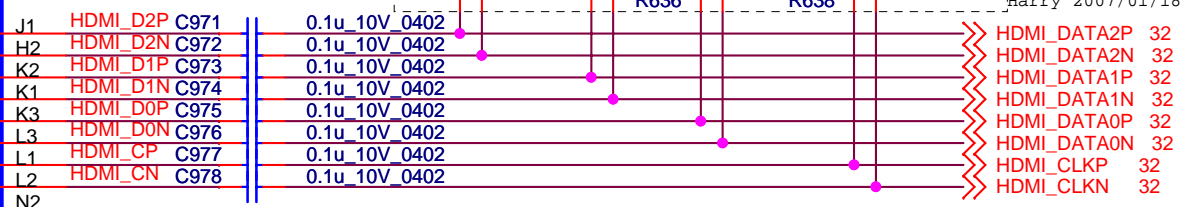
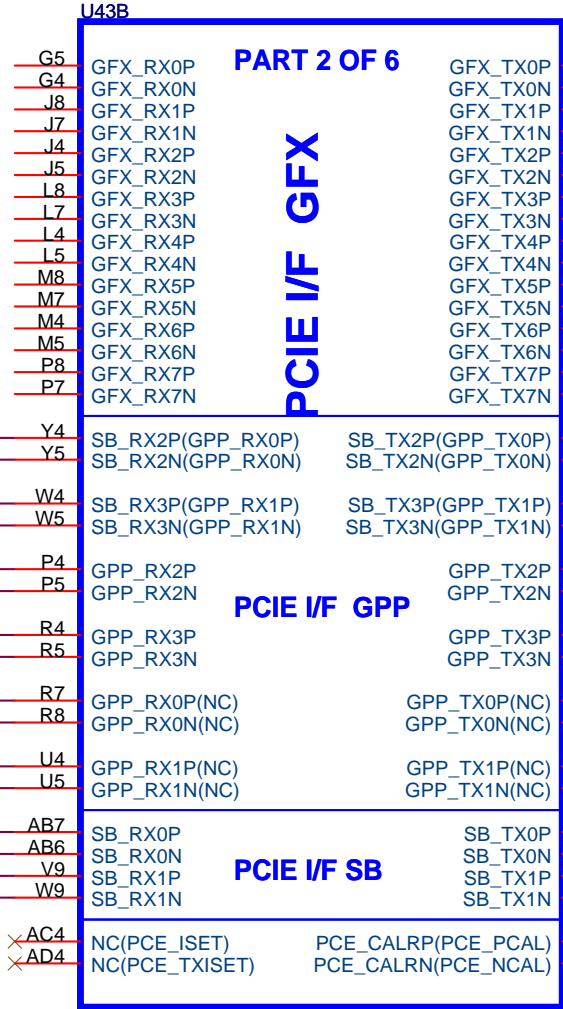
 MICRO-STAR INT'L CO.,LTD.		
Title		
RS690T HT LINK I/F		
Size	Document Number	Rev
A	MS-12221	1.0
Date:	Thursday, February 01, 2007	Sheet 11 of 45

Errata PA_IGPGENF5

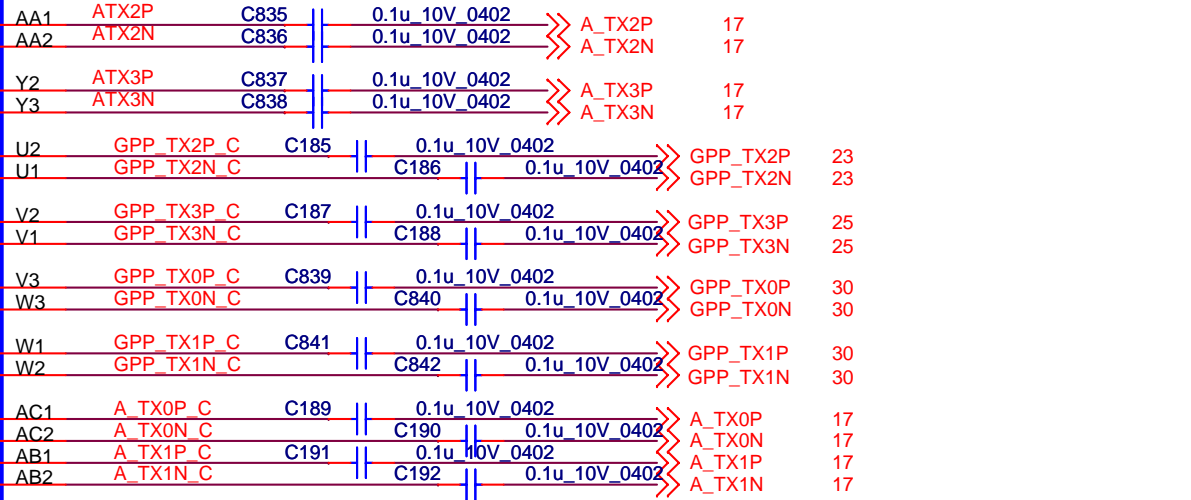
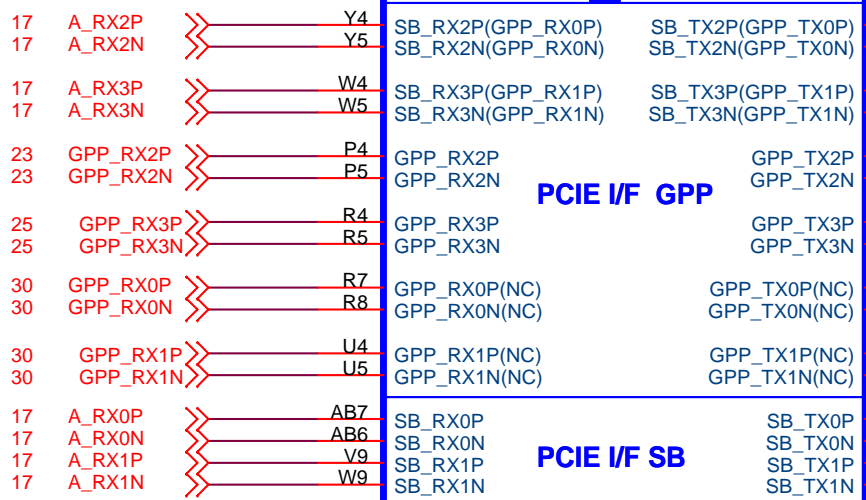
- 715_0402 N-2N7002_SOT23
- 715_0402 N-2N7002_SOT23
- 715_0402 N-2N7002_SOT23
- 715_0402 N-2N7002_SOT23
- 715_0402 N-2N7002_SOT23
- 715_0402 N-2N7002_SOT23



Harry 2007/01/18



Place these Caps close to HDMI connect HDMI I/F



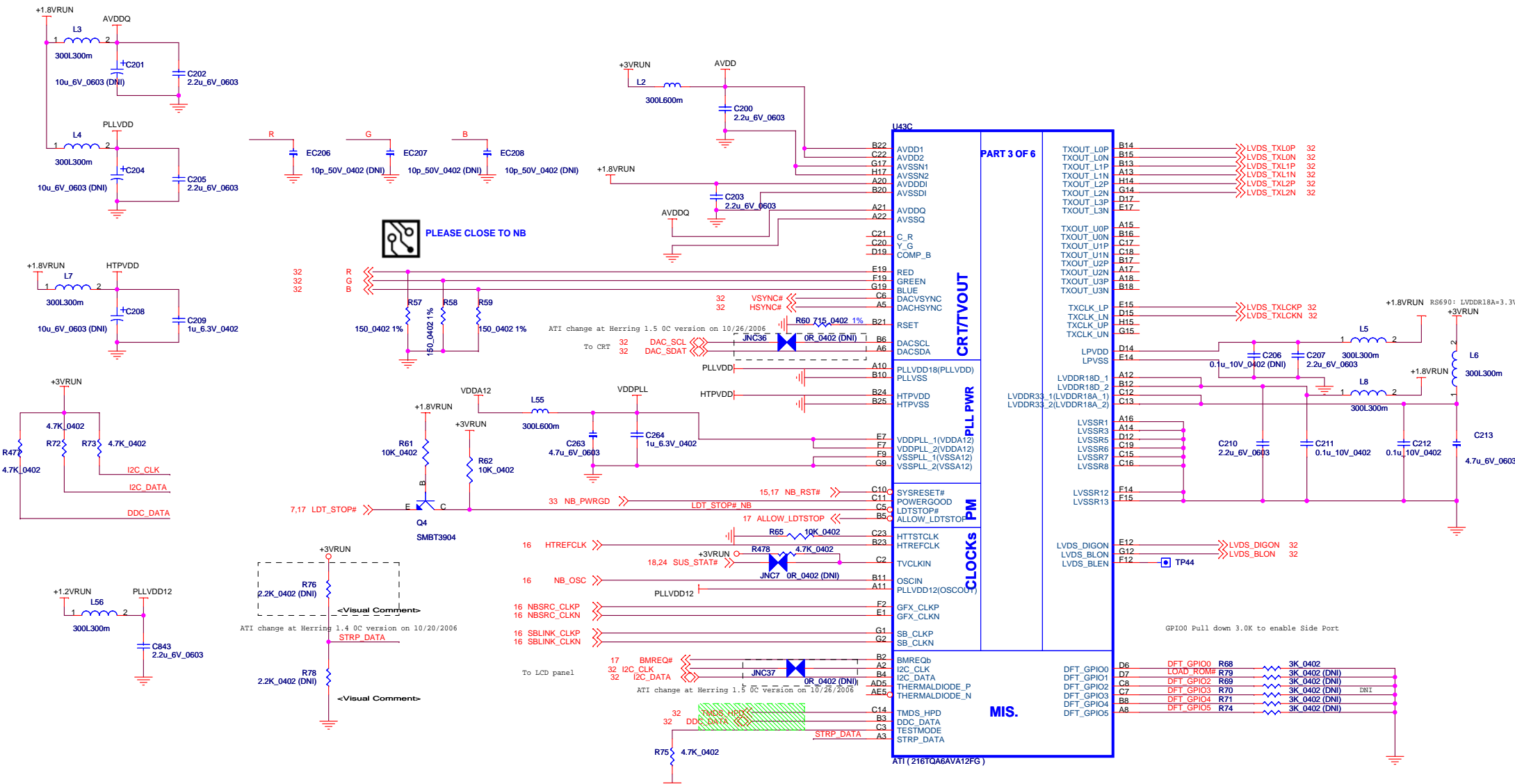
R50 5620hm
R52 2K0hm

MICRO-STAR INT'L CO.,LTD.

Title: **RS690T PCI-E LINK&HDMI I/F**

Size A	Document Number MS-12221	Rev 1.0
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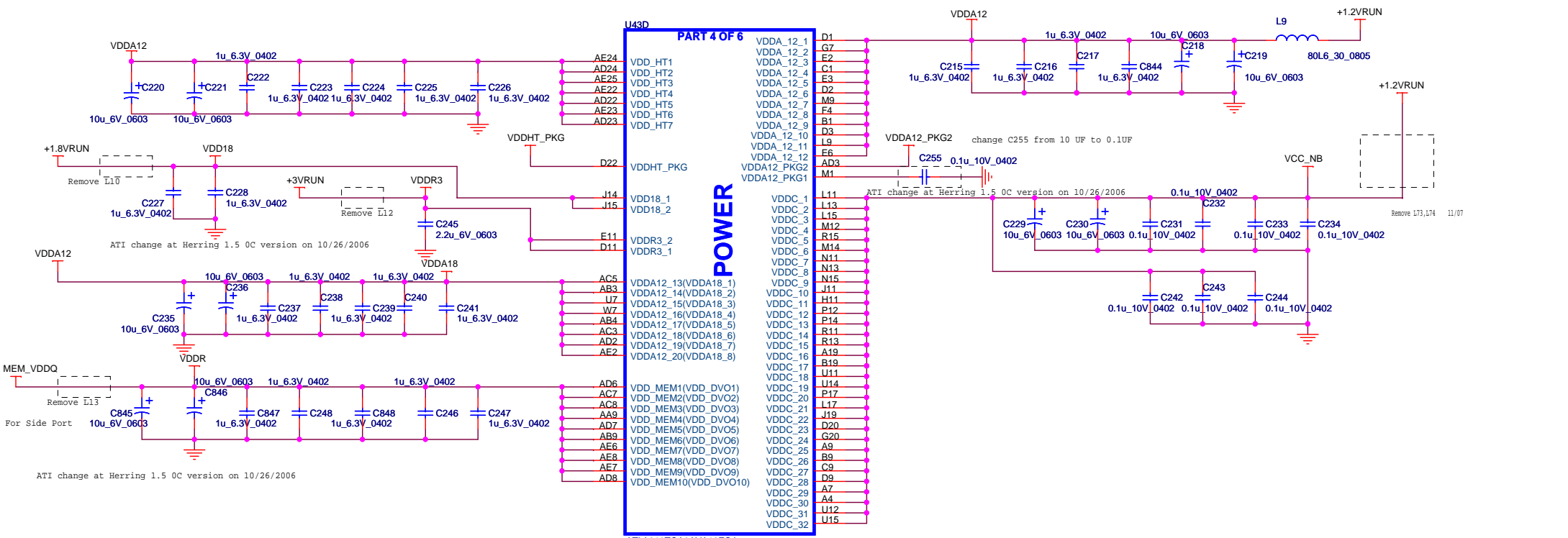
Date: Thursday, February 01, 2007 Sheet 12 of 45



	RS485/RS690	RS690 only (NC for RS485)		
	DFT_GPIO1	DFT_GPIO0	DFT_GPIO[4:2]	DFT_GPIO5
PULL HIGH (internally pulled high)	Bypass the loading of EEPROM straps and use Hardware default values DEFAULT	Memory side port not available	These pin straps are used to configure PCI-E GPP mode: 111: register defined (register default to Config E) DEFAULT 110: 4-0-0-0 Config A 101: 4-4 Config B 100: 4-2-2 Config C 011: 4-2-1-1 Config D 010: 4-1-1-1 Config E	Enable debug bus via the memory IO pads, if available in the package use default values DEFAULT
PULL LOW	I2C Master can load strap values from EEPROM if connected, or use default values if not connected	Memory side port available DEFAULT	others: register defined (register default to Config E)	use the memory data bus to output the debug bus

LOAD_ROM#: LOAD ROM STRAP ENABLE

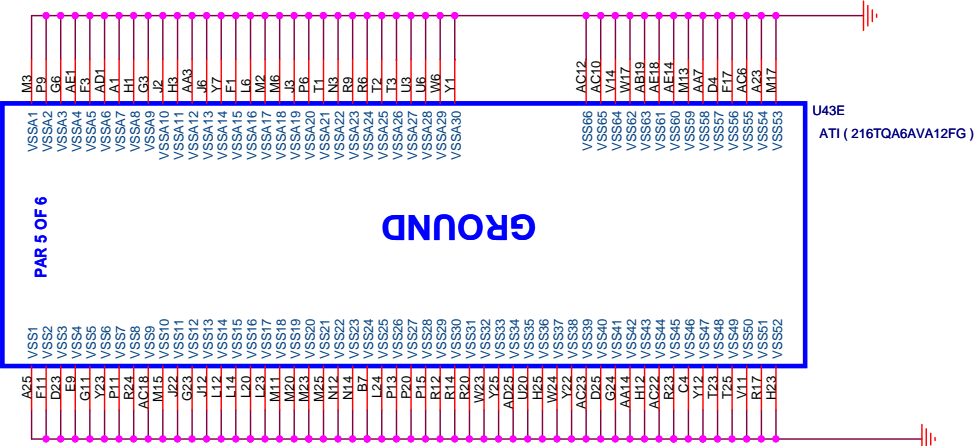
High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE



PART 4 OF 6

POWER


ATI (216TQA6AVA12FG)

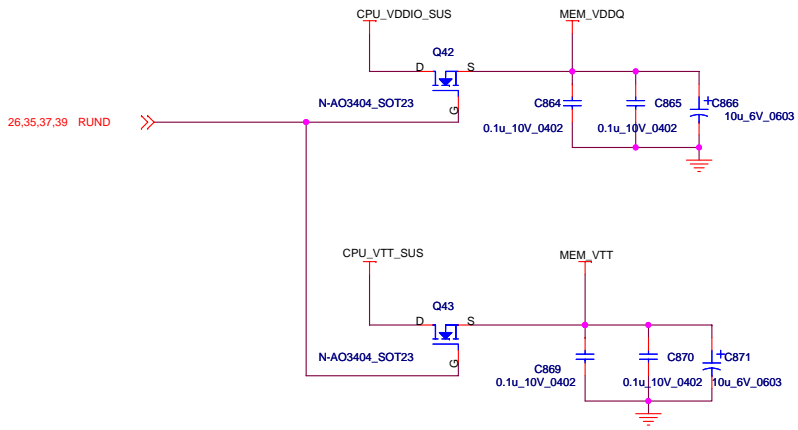
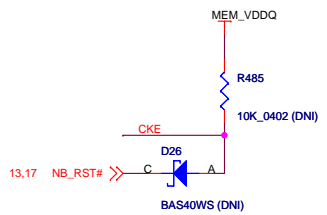
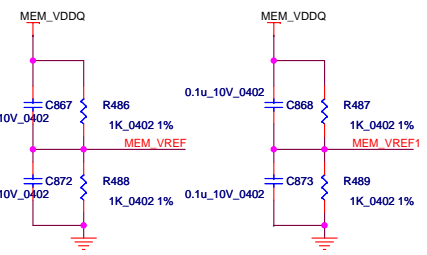
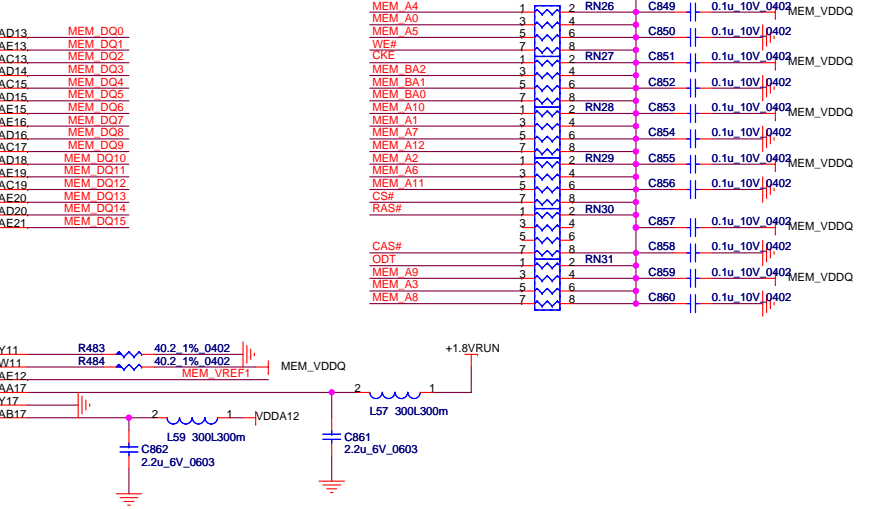
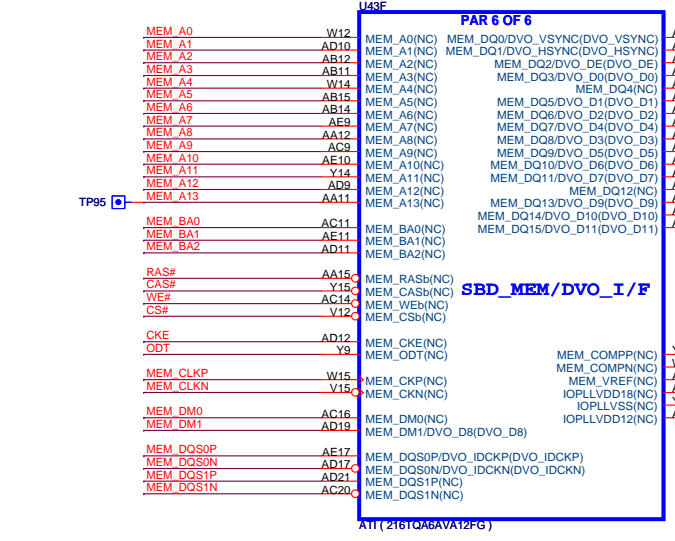
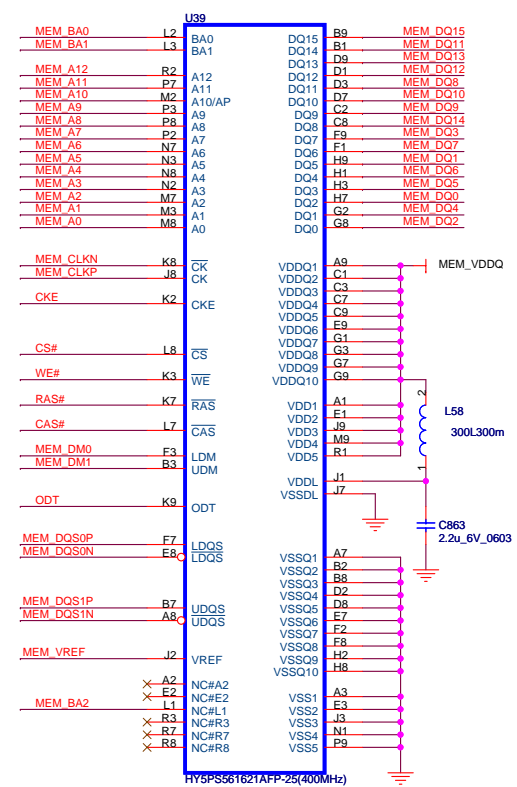


PAR 5 OF 6

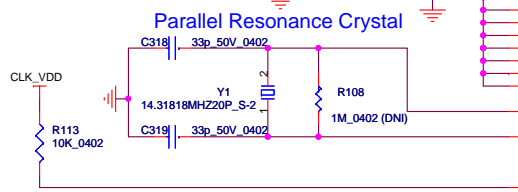
GROUND

U43E
ATI (216TQA6AVA12FG)

		MICRO-STAR INT'L CO.,LTD.	
Title			
RS690T POWER & GND			
Size	Document Number		Rev
B	MS-12221		1.0
Date:	Thursday, February 01, 2007	Sheet	14 of 45



- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U11
- 2- PUT DECOUPLING CAPS CLOSE TO U11 POWER PIN



$I_{oh} = 5 \cdot I_{ref} (2.32mA)$
 $V_{oh} = 0.71V @ 60 \text{ ohm}$



PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB600

	SB600
C325 to C332	0.1uF
R165	562 Ohm 1%
R166	2.05K 1%
R167	0 Ohm
R179	10K

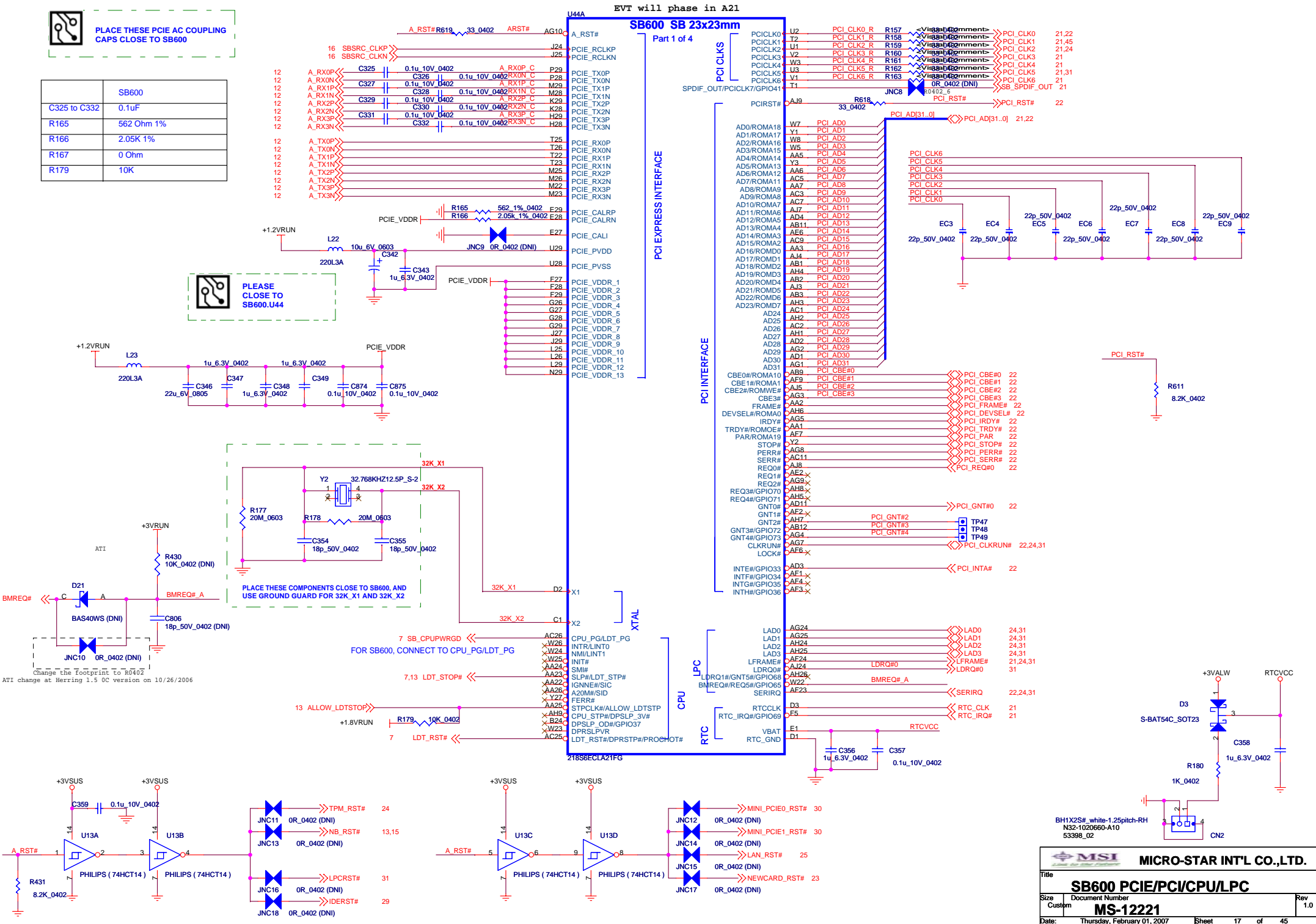


PLEASE CLOSE TO SB600,U44

EVT will phase in A21

SB600 SB 23x23mm

Part 1 of 4

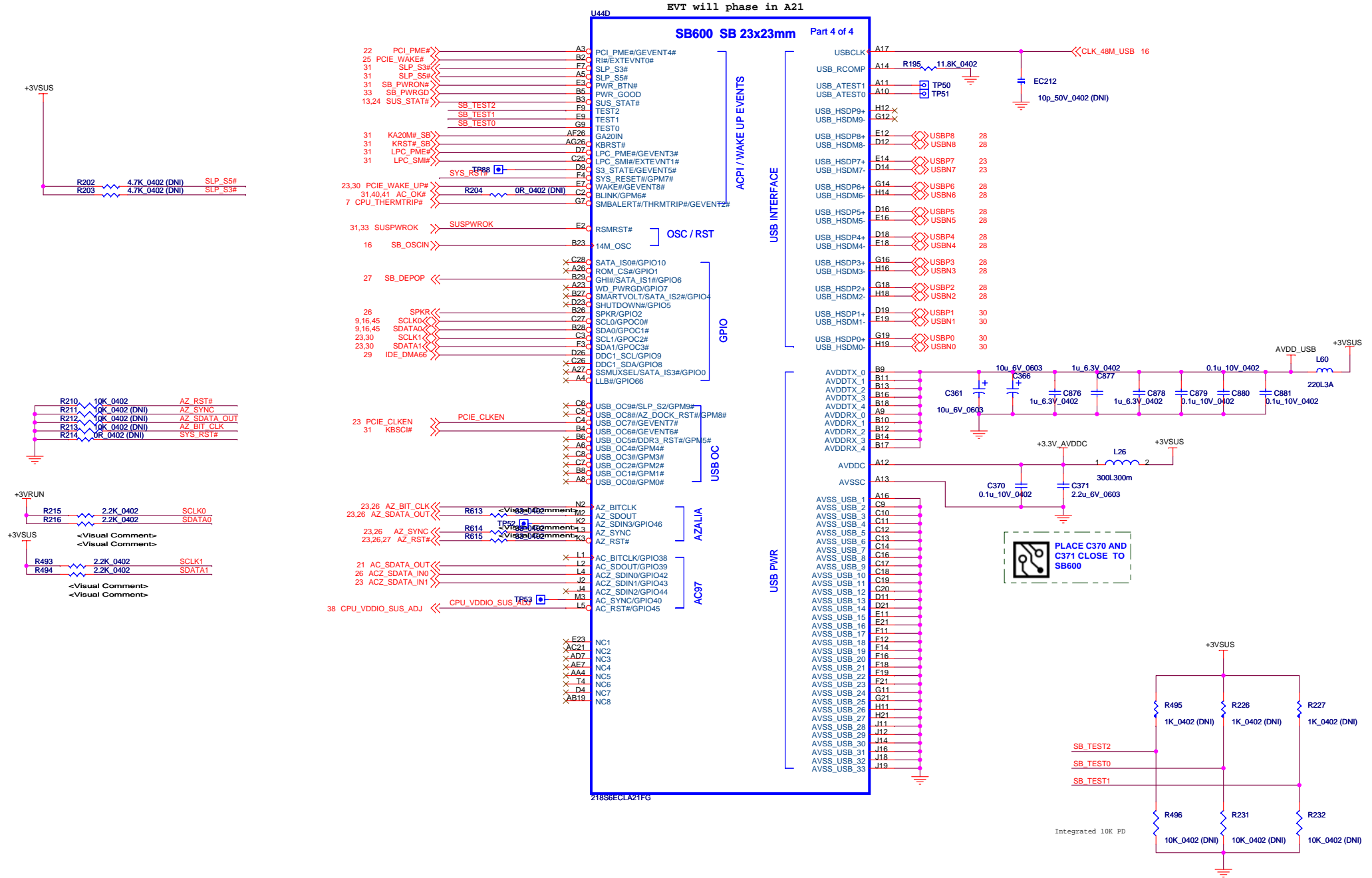


MSI MICRO-STAR INT'L CO.,LTD.

Title: **SB600 PCIE/PCI/CPU/LPC**

Size: Custom Document Number: **MS-12221** Rev: 1.0

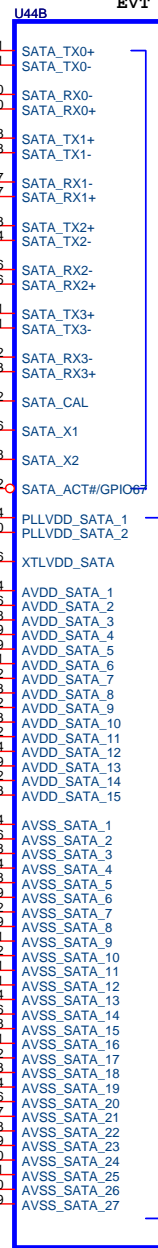
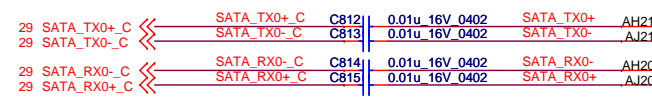
Date: Thursday, February 01, 2007 Sheet: 17 of 45



EVT will phase in A21

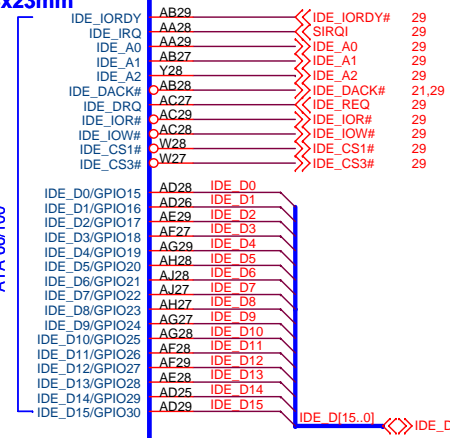
SB600 SB 23x23mm

Part 2 of 4



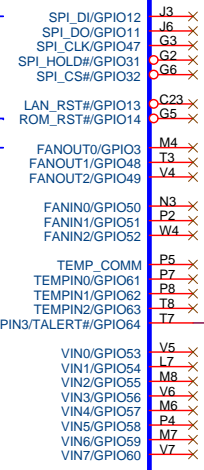
SERIAL ATA

SERIAL ATA POWER



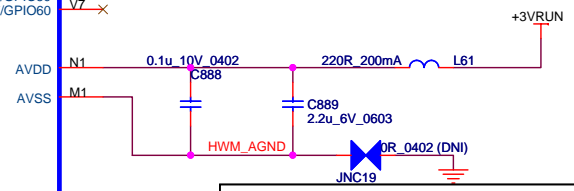
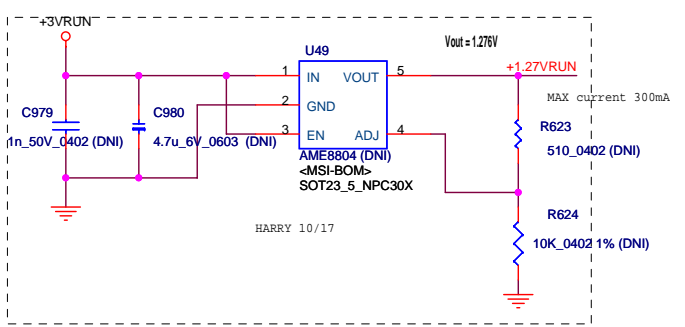
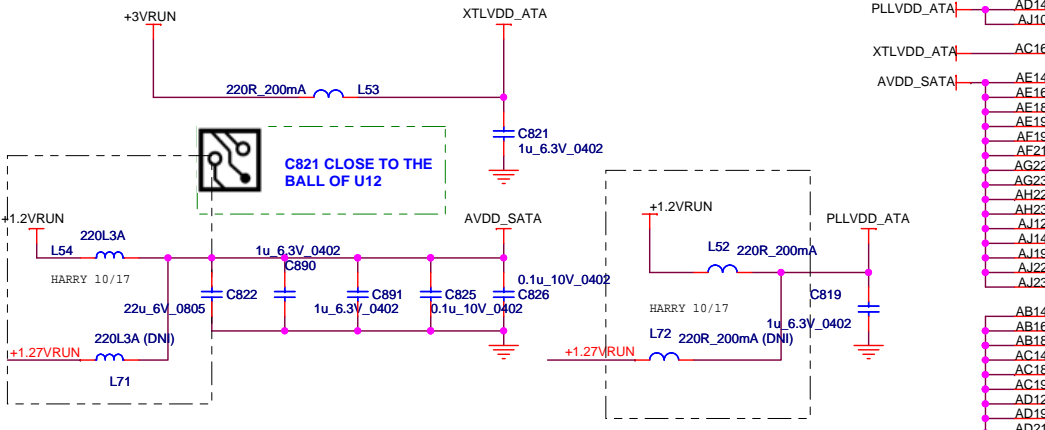
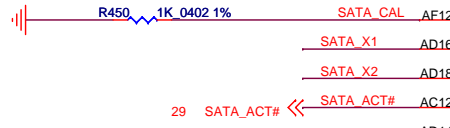
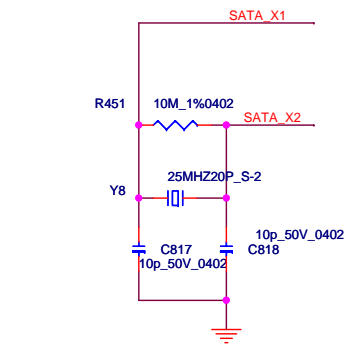
SPI ROM

HW MONITOR



GPIO 50,51,52,61,62,63. BOIS need to programming to GPIO output or Pull Down

MICRO-STAR INT'L CO.,LTD.
 Title: **SB600 SATA/IDE/HWM/SPI**
 Size B Document Number: **MS-12221** Rev 1.0
 Date: Thursday, February 01, 2007 Sheet 19 of 45

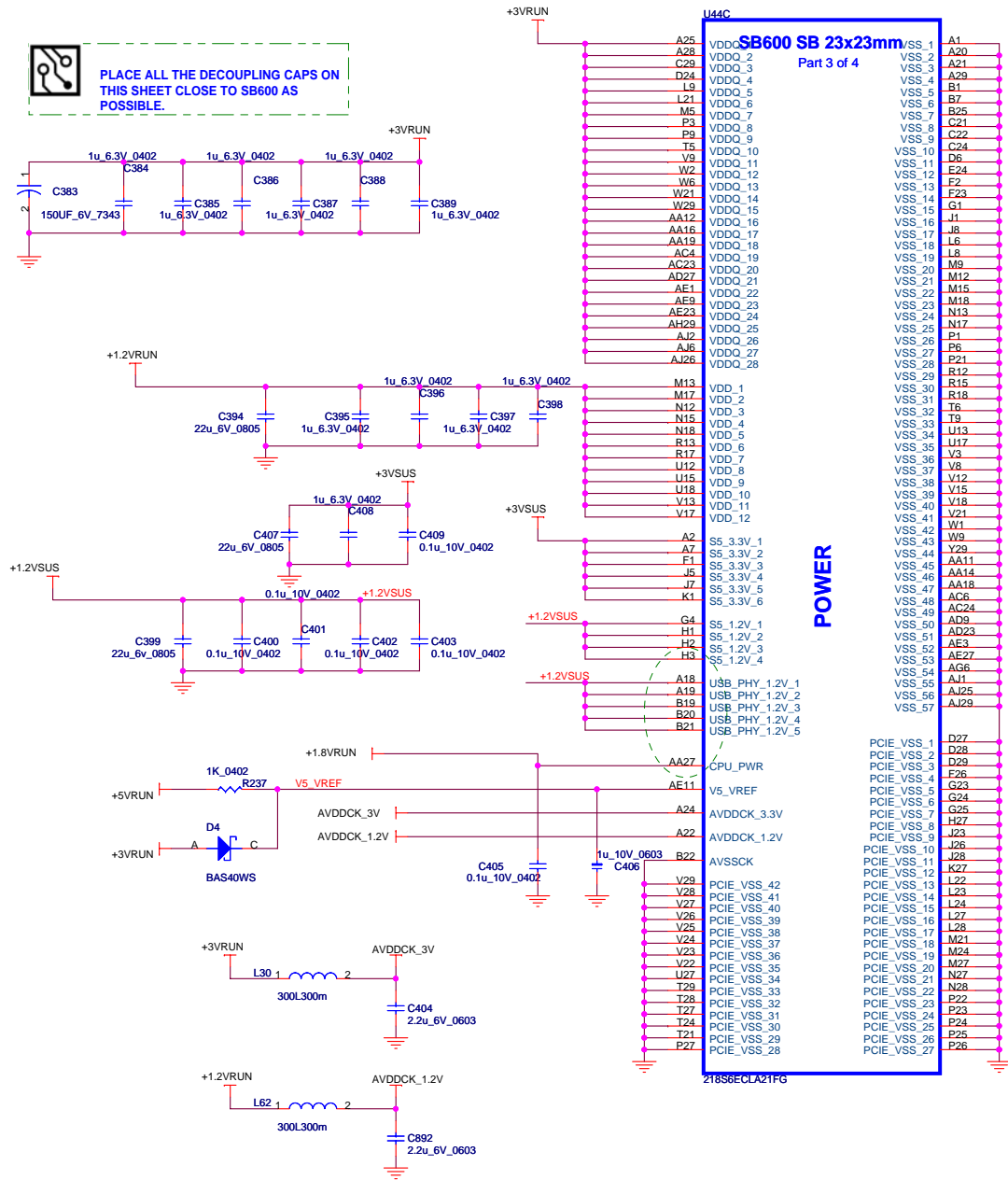


21856ECLA21FG

EVT will phase in A21



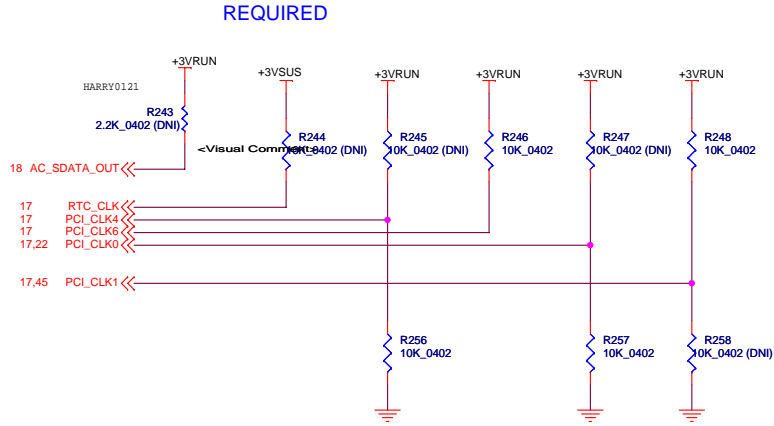
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB600 AS POSSIBLE.



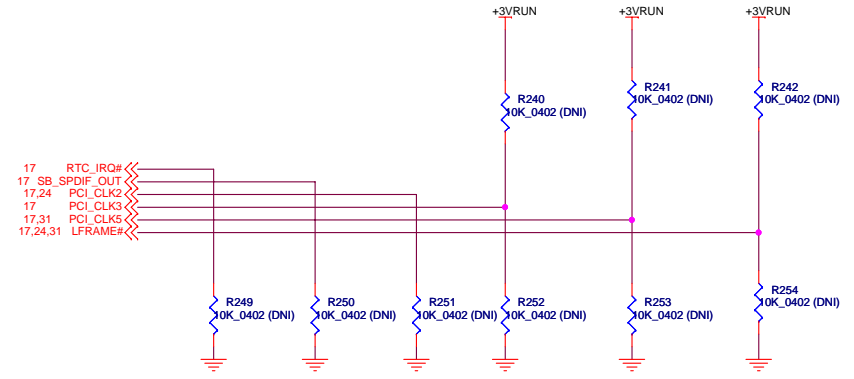
POWER

REQUIRED STRAPS

NPTE: FOR SB460, EXTERNAL PU/PD ARE REQUIRED



SB600 HAS 15K INTERNAL PU FOR PCI_AD[31:23]

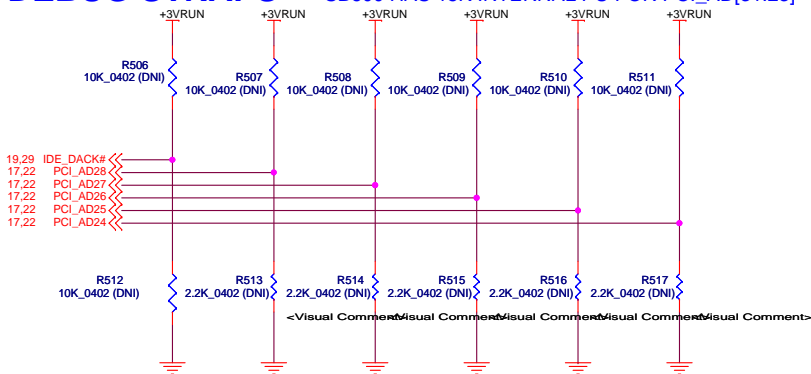


SB600						
	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, L = LPC ROM L, L = FWH ROM DEFAULT	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

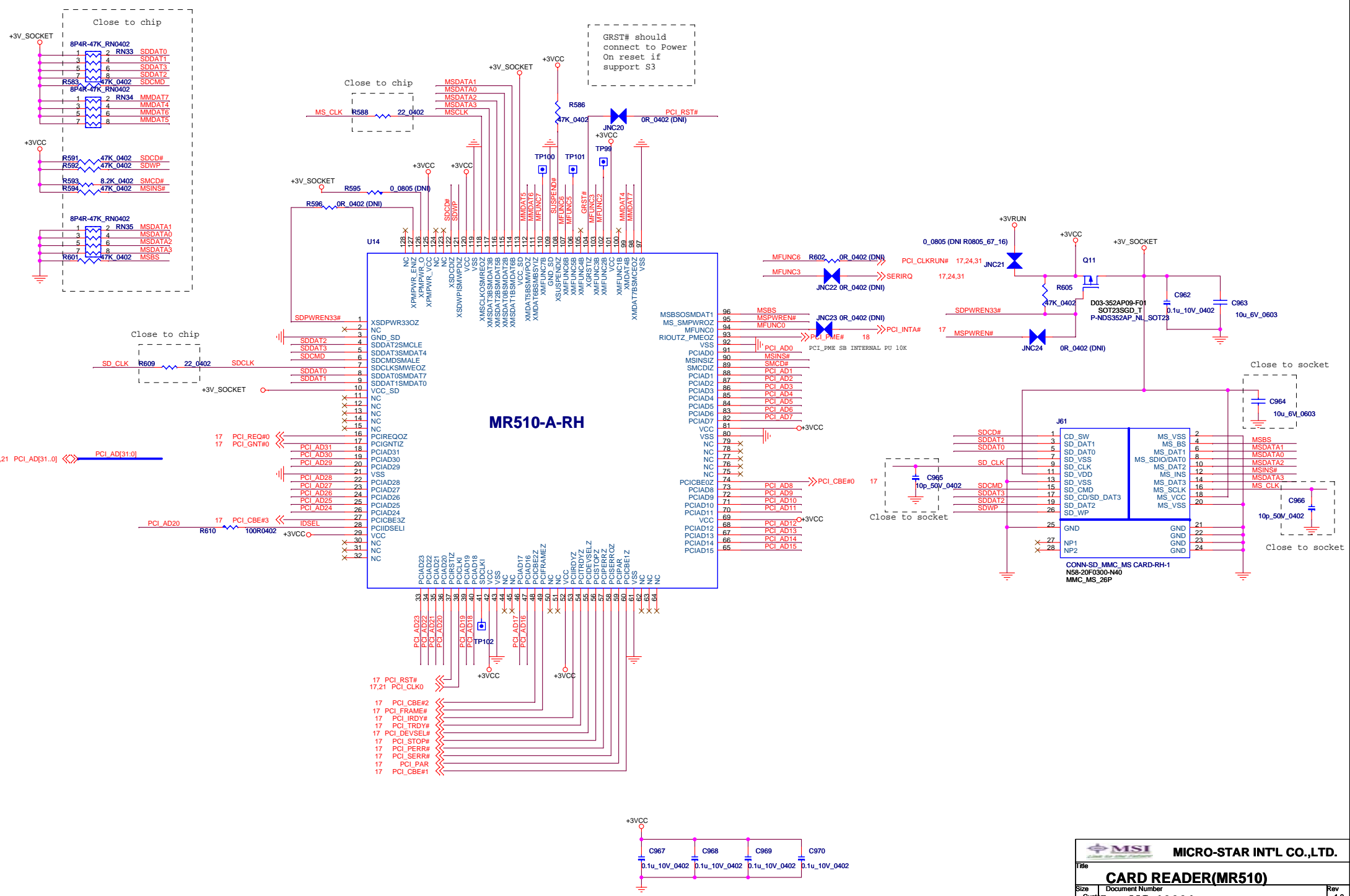
DEBUG STRAPS

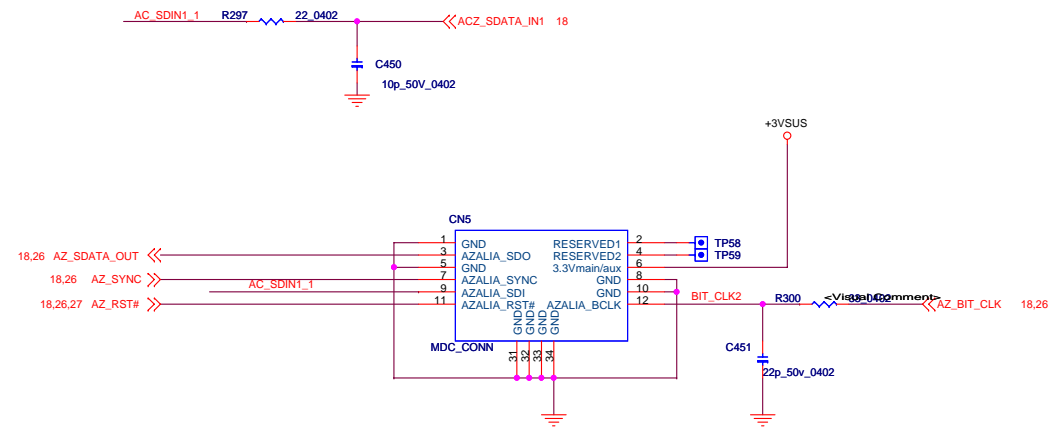
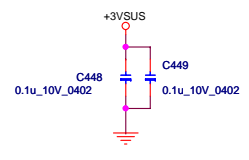
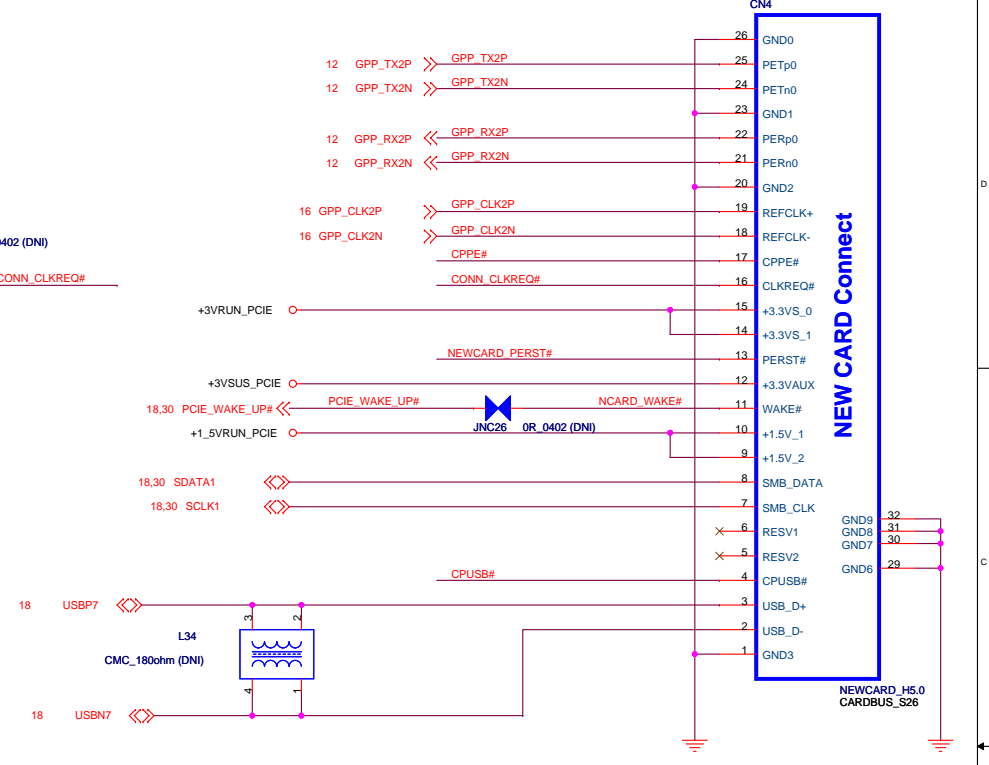
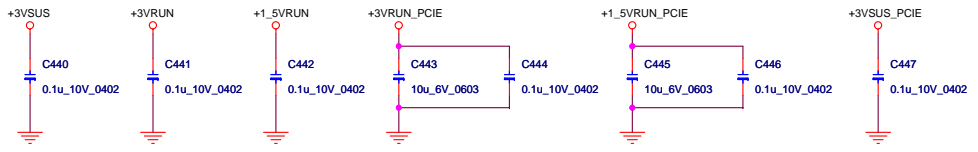
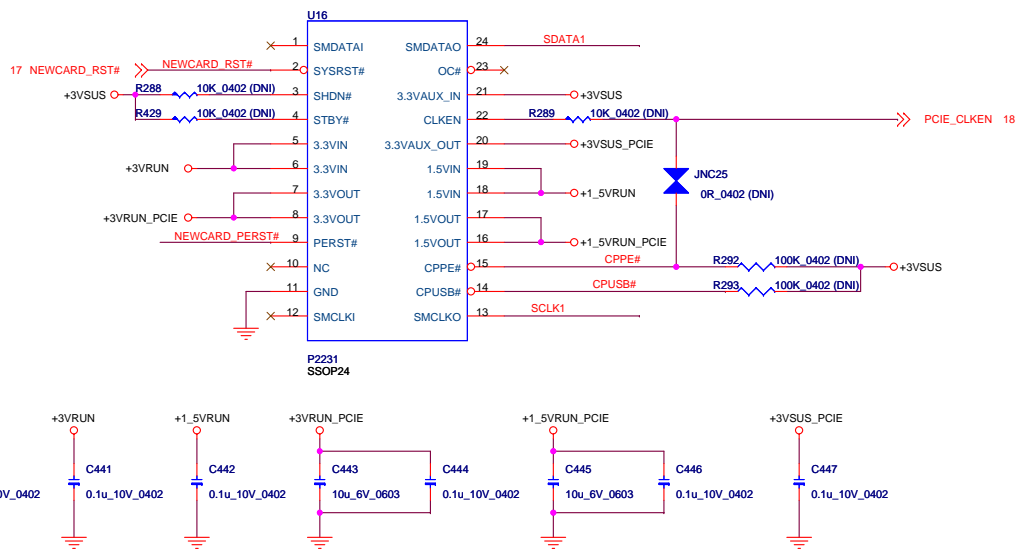
SB600 HAS 15K INTERNAL PU FOR PCI_AD[31:23]

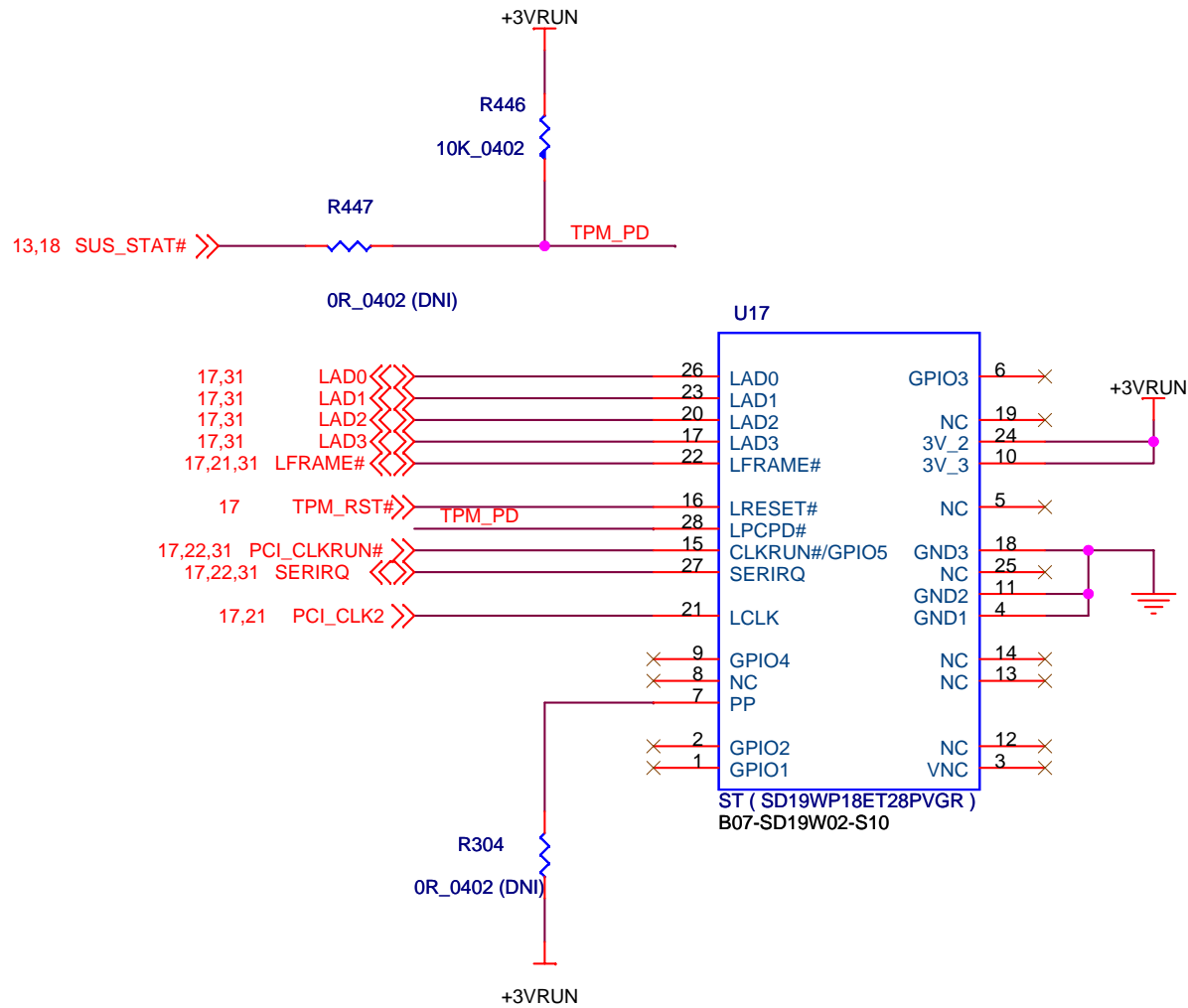



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS

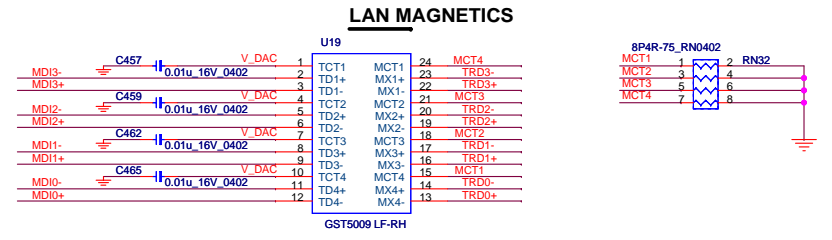
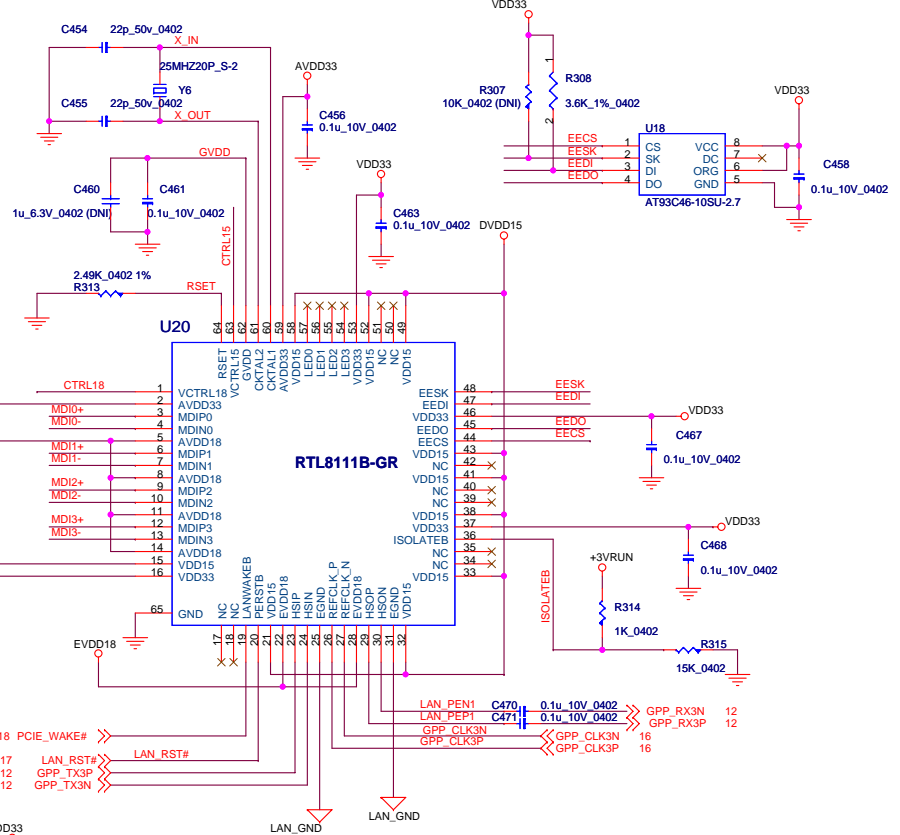




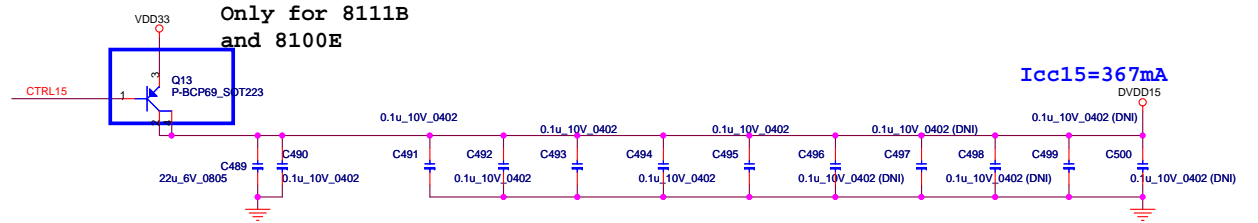
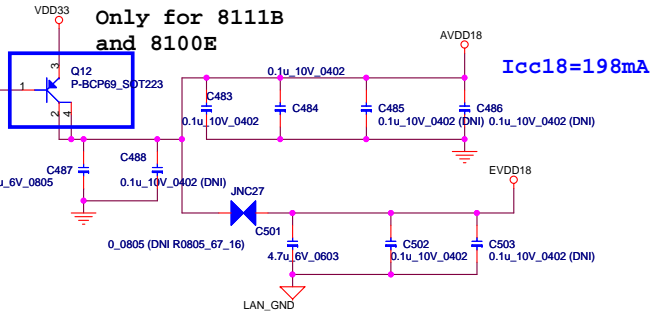


 MICRO-STAR INT'L CO.,LTD.	
Title	
TPM (ST19WP18-TPM-C)	
Size	Document Number
A	MS-12221
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24	45

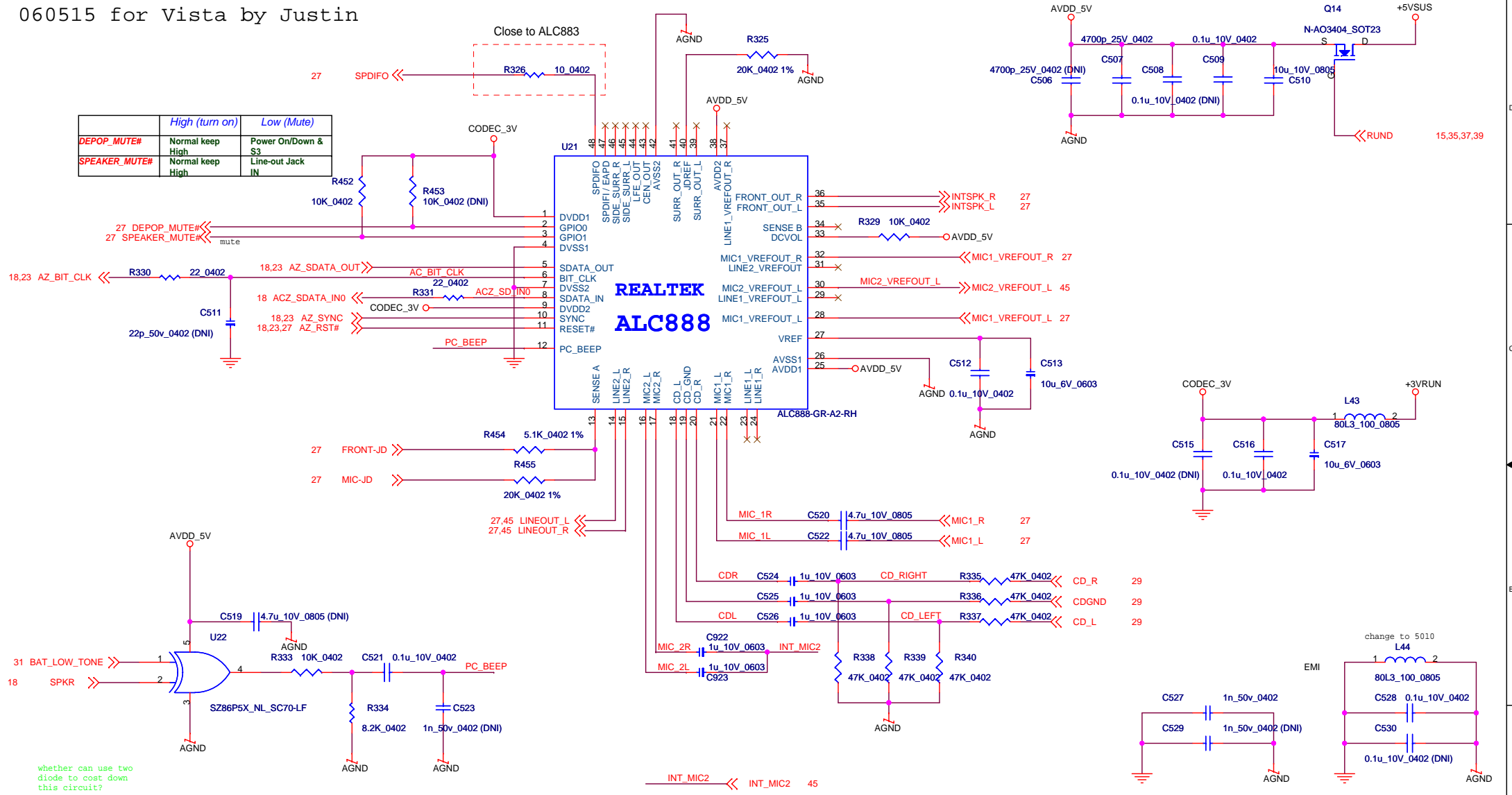
DNI component check with Realtek's reference design OK



$I_{cc33} = 103\text{mA}$
 $\text{Total (LAN)} = I_{cc33} + I_{cc18} + I_{cc15}$
 $= 103 + 198 + 367$
 $= 668\text{mA}$



	High (turn on)	Low (Mute)
DEPOP_MUTE#	Normal keep High	Power On/Down & S3
SPEAKER_MUTE#	Normal keep High	Line-out Jack IN

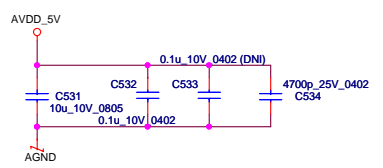


MSI
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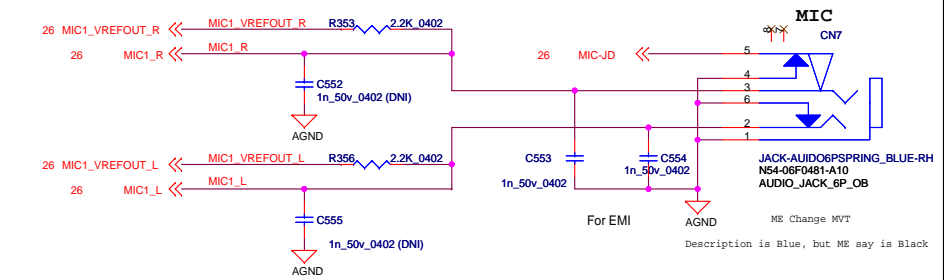
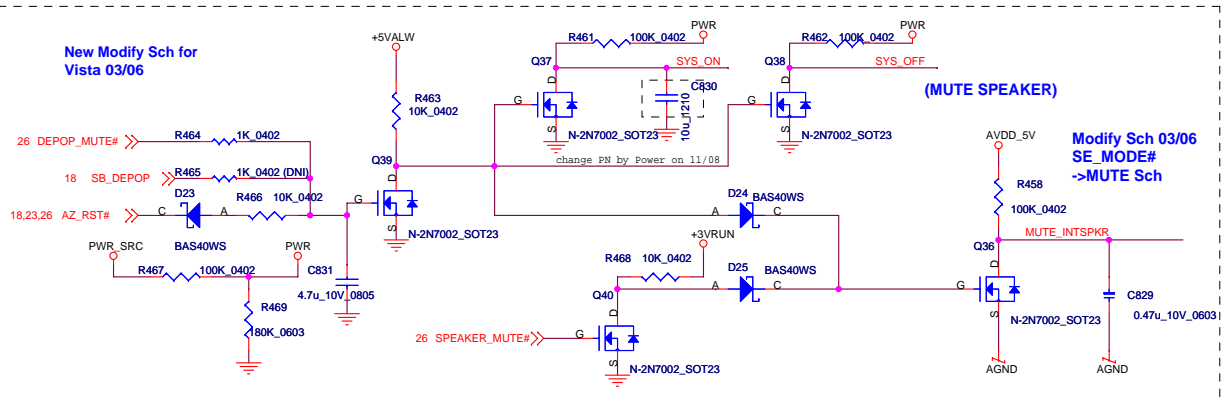
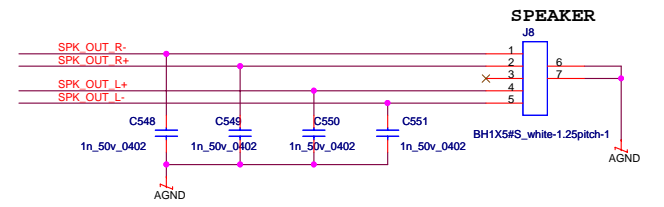
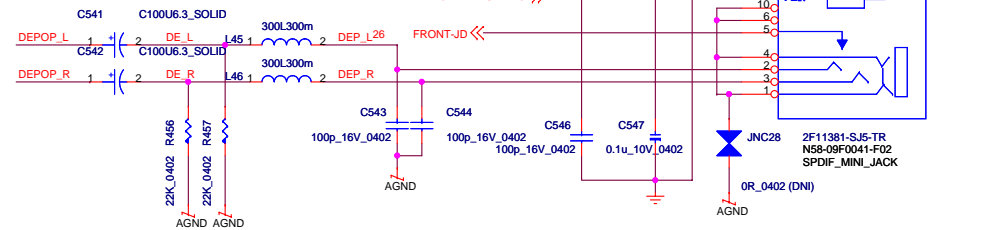
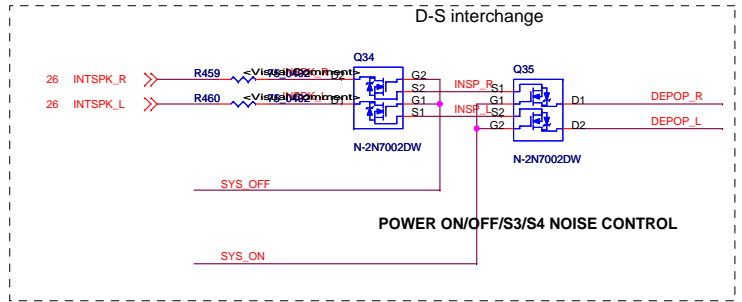
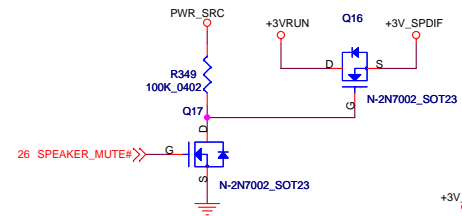
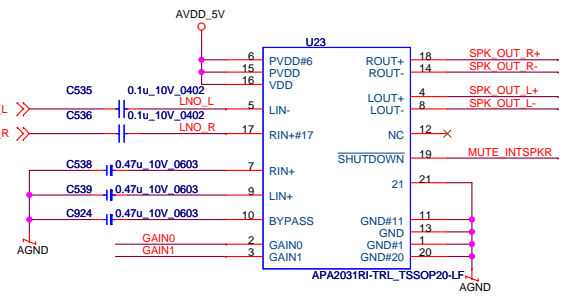
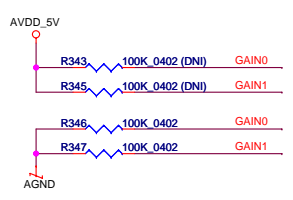
Title: **AUDIO(ALC888)**

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	GAIN0	GAIN1	SE/BTL#
6dB	0	0	0
10dB	0	1	0
15.6dB	1	0	0
21.6dB	1	1	0
4.3dB	X	X	1



Mobile Configuration:

(3 external jacks, 1 internal Mic, 2 sets stereo internal speaker)

Pin Assignment	Location	Re-tasking
FRONT (pin-35/36)	SPDIF jack, AMP	SPDIF output, AMP output (Int.SPKR), ?
SURR (pin-39/41)	X	X
CEN/LFE (pin-43/44)	X	X
SIDESURR (pin-45/46)	X	X
LINE1 (pin-23/24)	Line-in jack	Line input, ?
MIC1 (pin-21/22)	MIC-in jack	Mic input, ?
MIC2 (pin-16/17)	Int.MIC	Int.Mic input

Close To Power Source
POWER ON/OFF/S3/S4 NOISE CONTROL

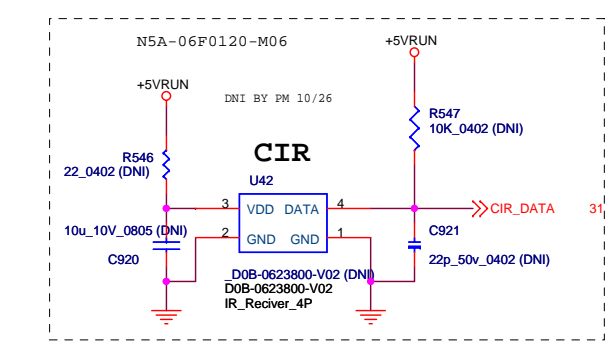
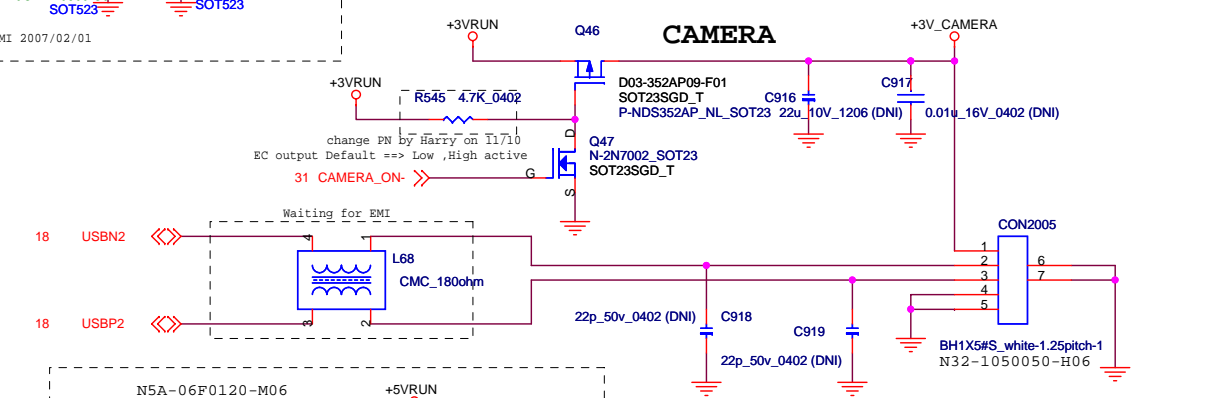
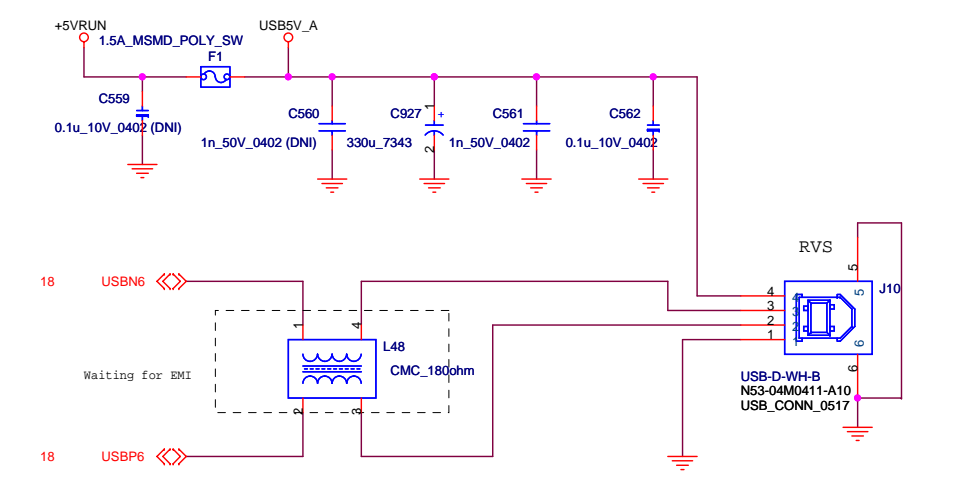
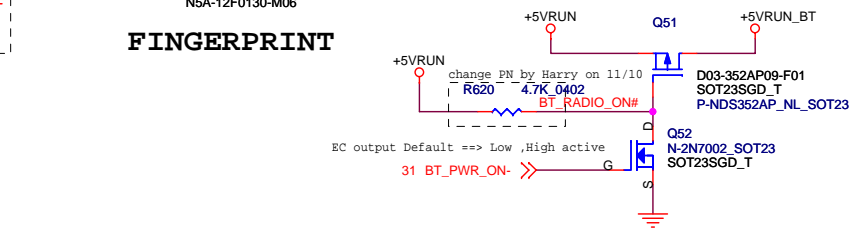
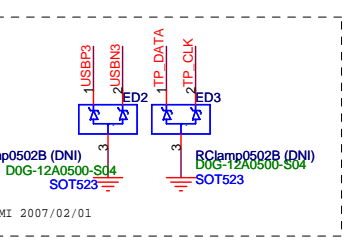
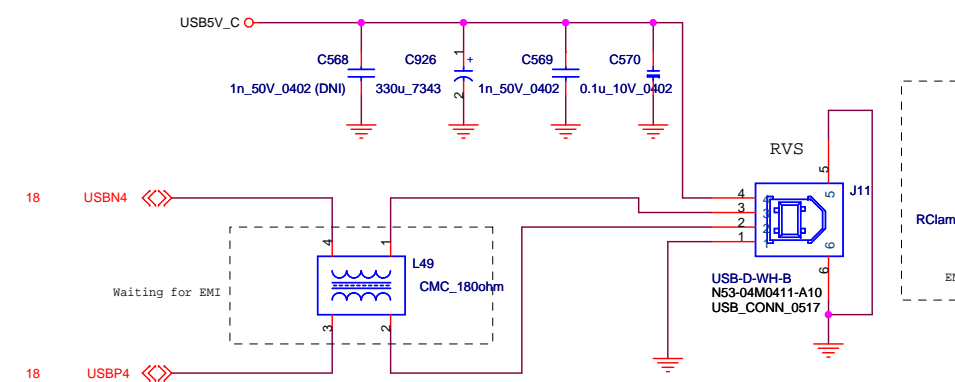
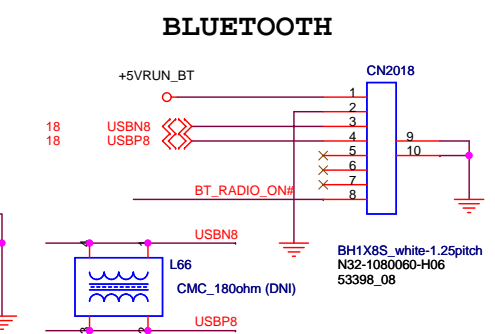
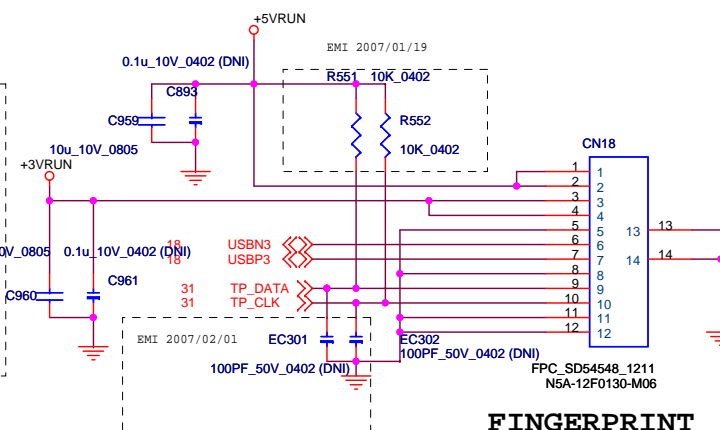
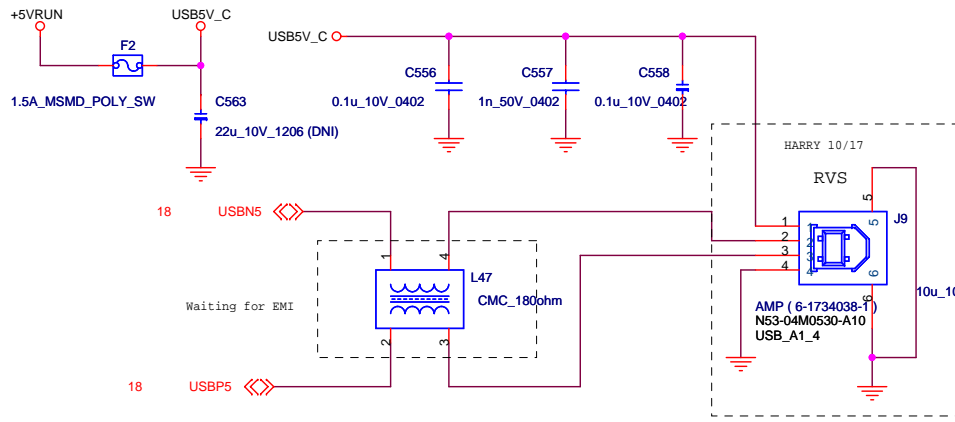
POWER ON/OFF/S3/S4 NOISE CONTROL

MSI MICRO-STAR INT'L CO.,LTD.

Title: **AMP & SPK & MIC & SPK**

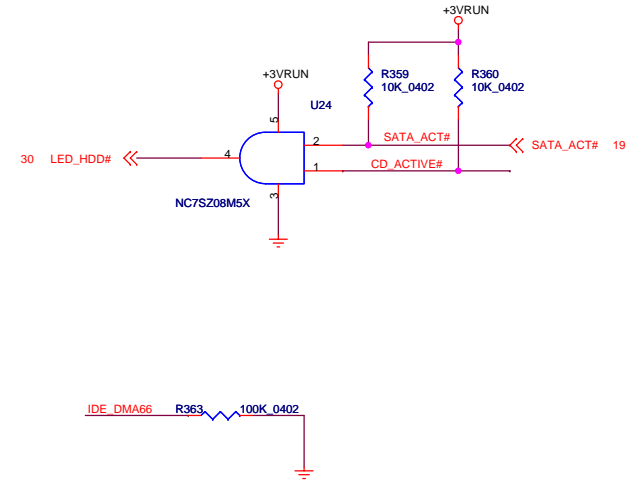
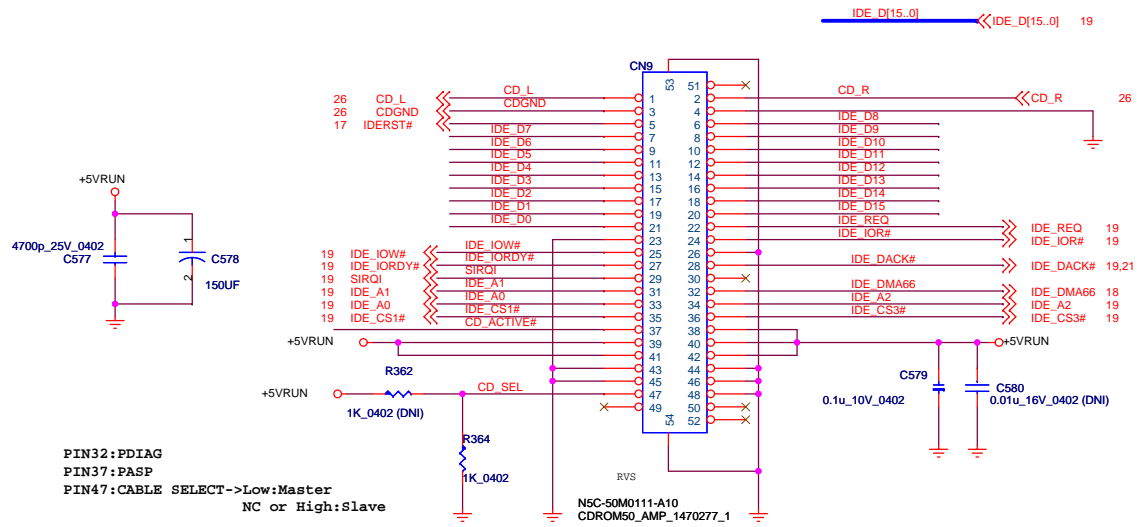
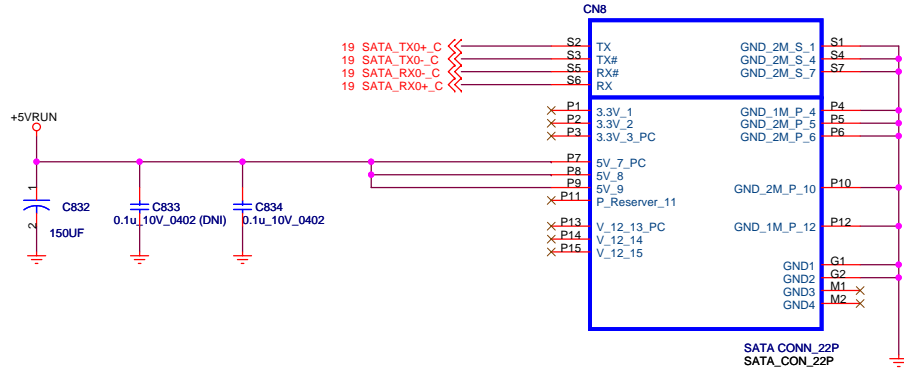
Size: Custom Document Number: **MS-12221** Rev: 1.0

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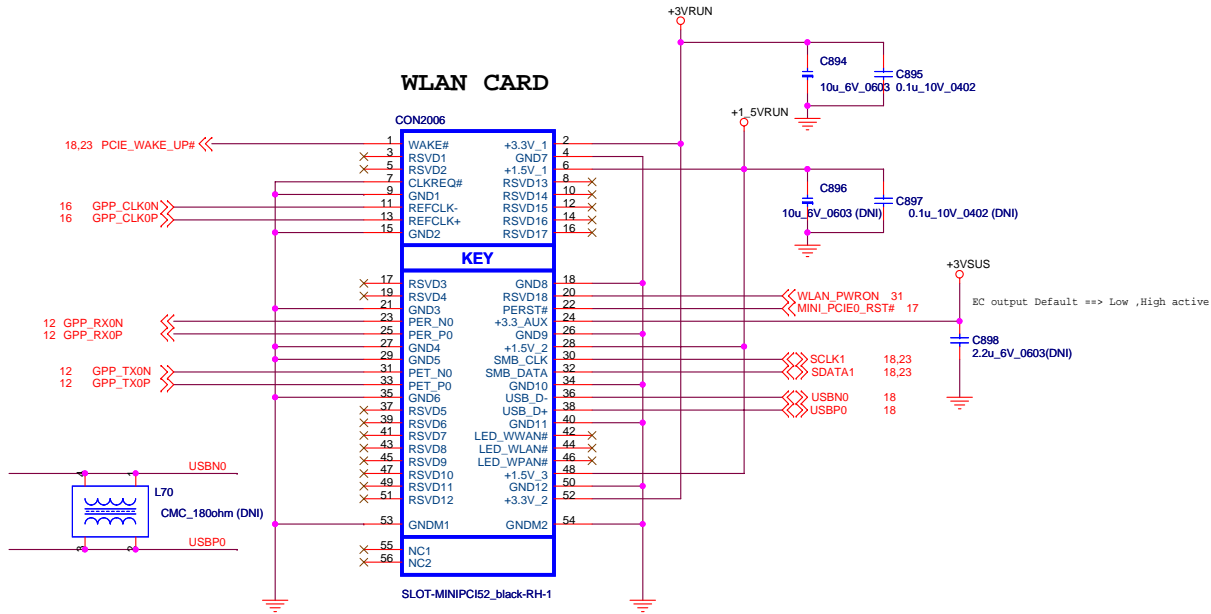
MSI MICRO-STAR INT'L CO.,LTD.		
USB,CIR,BT,FP,CAMERA		
Size B	Document Number	Rev 1.0
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2.5"HD DRIVE

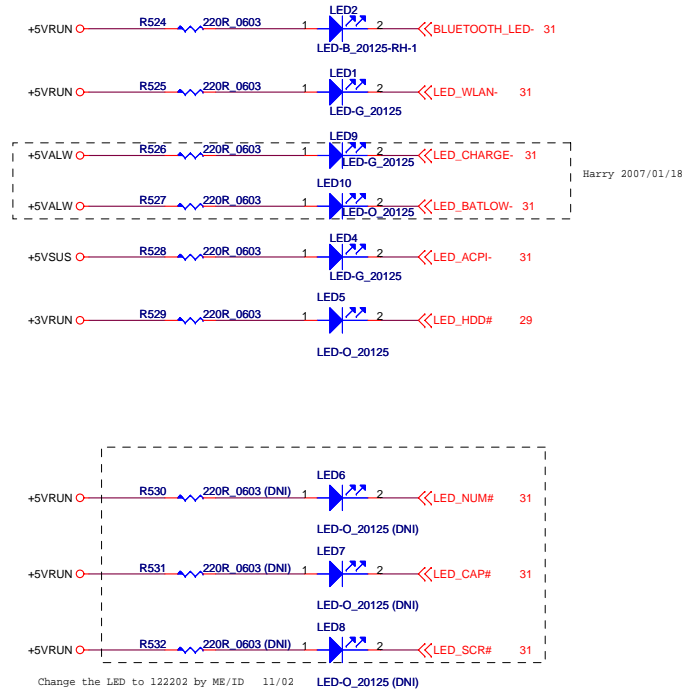


PIN32:PDIAG
PIN37:PASP
PIN47:CABLE SELECT->Low:Master
NC or High:slave

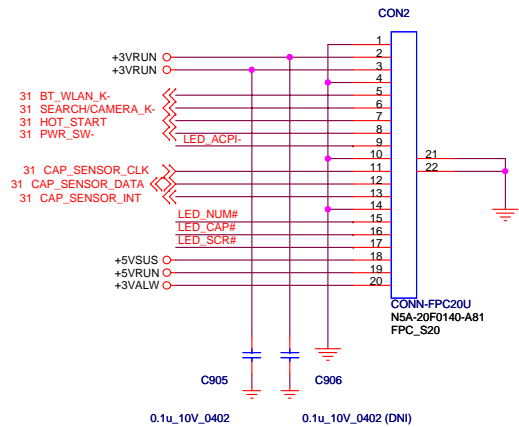
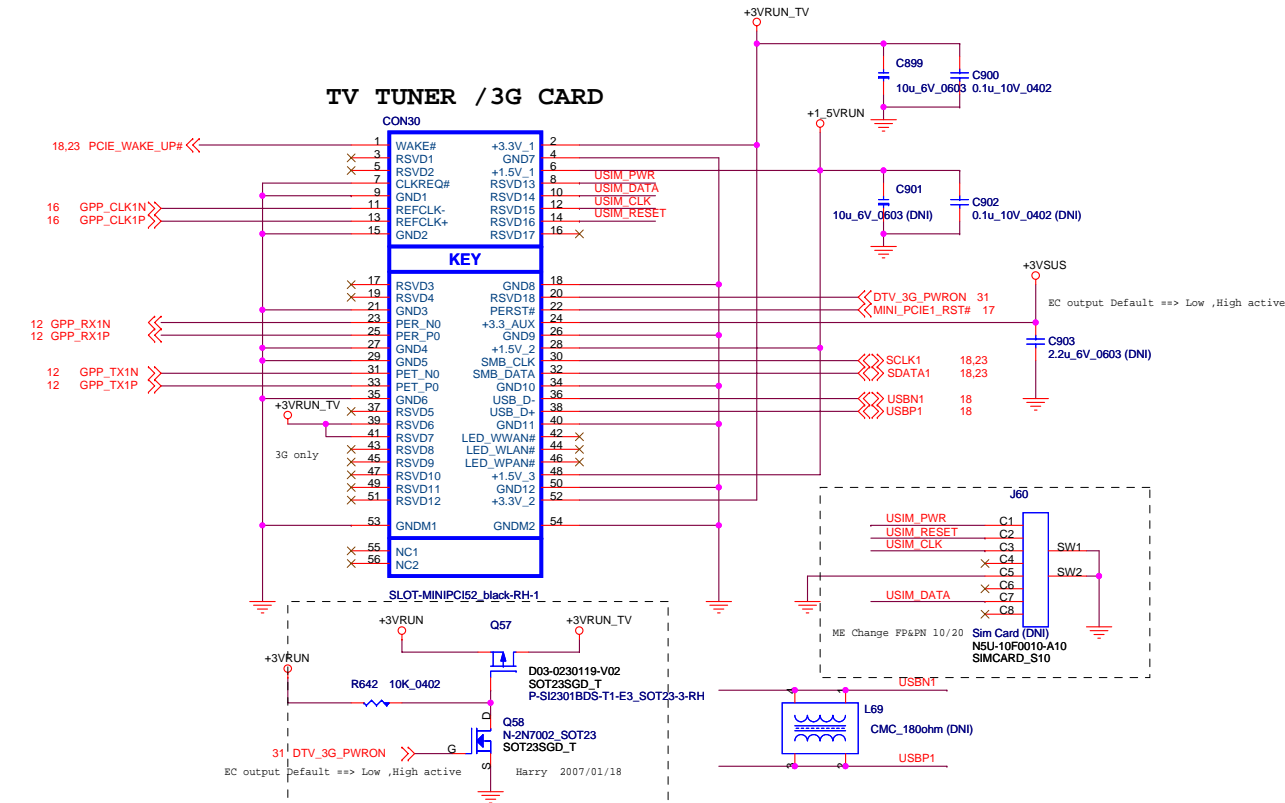
WLAN CARD

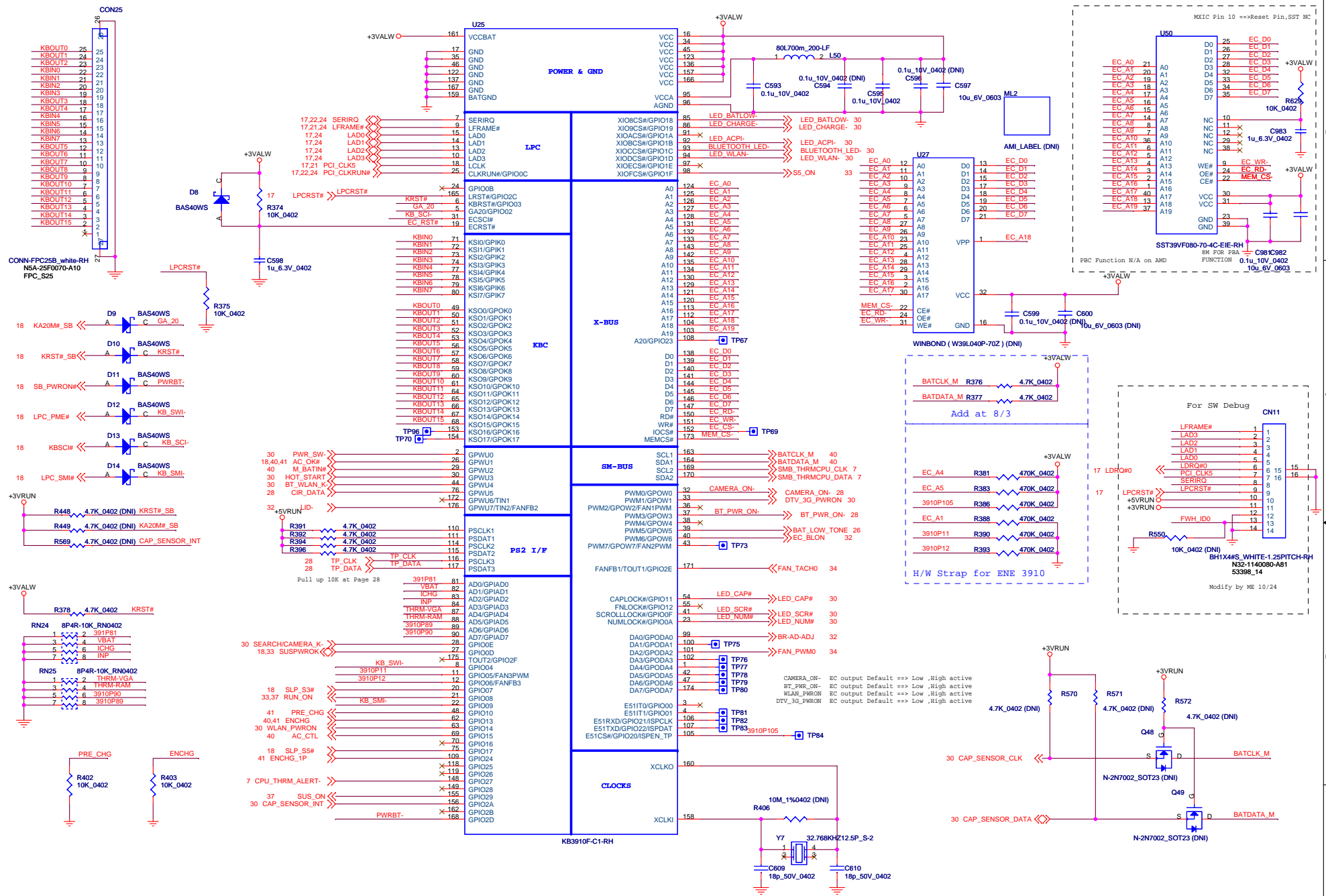


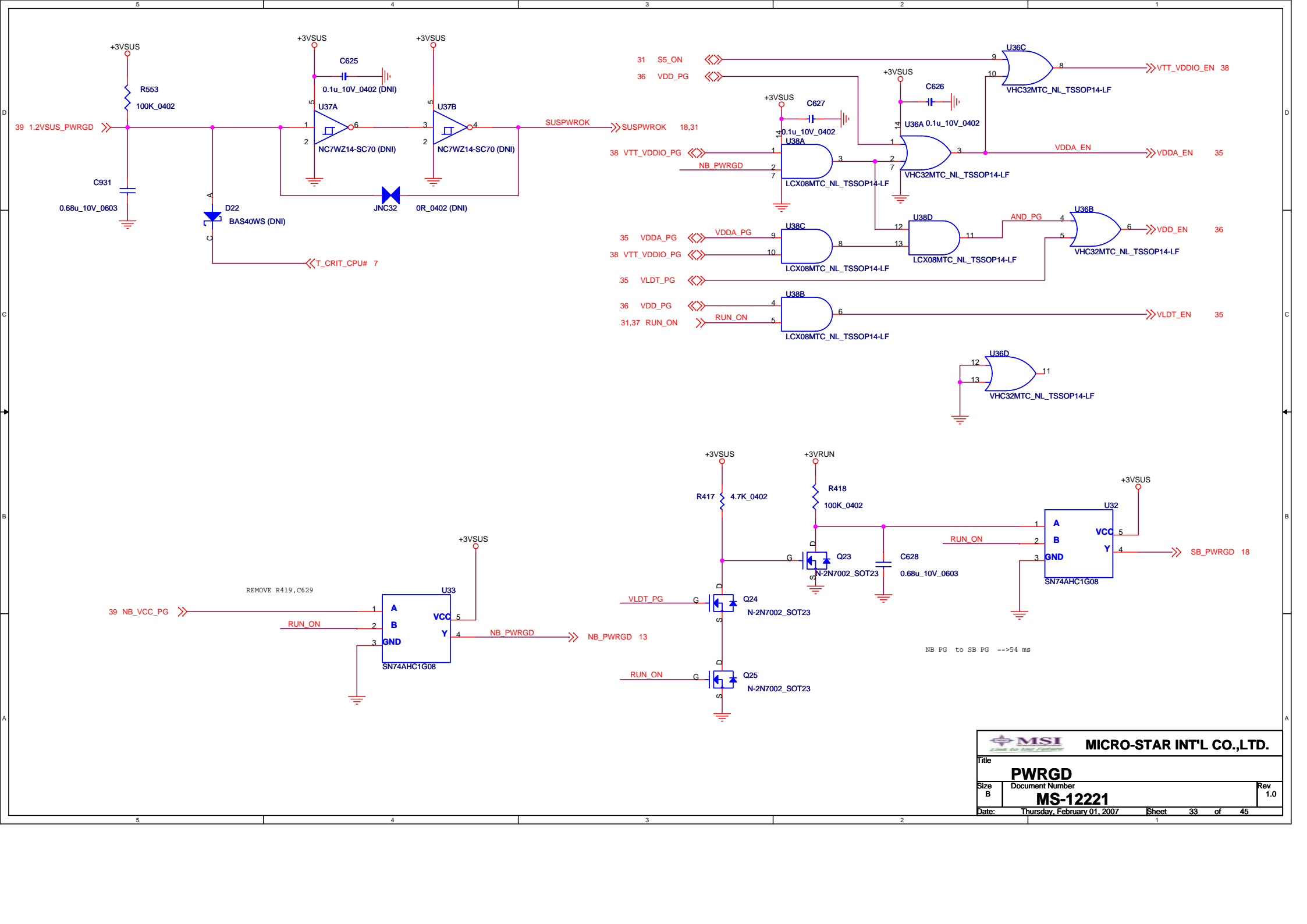
Main PCB




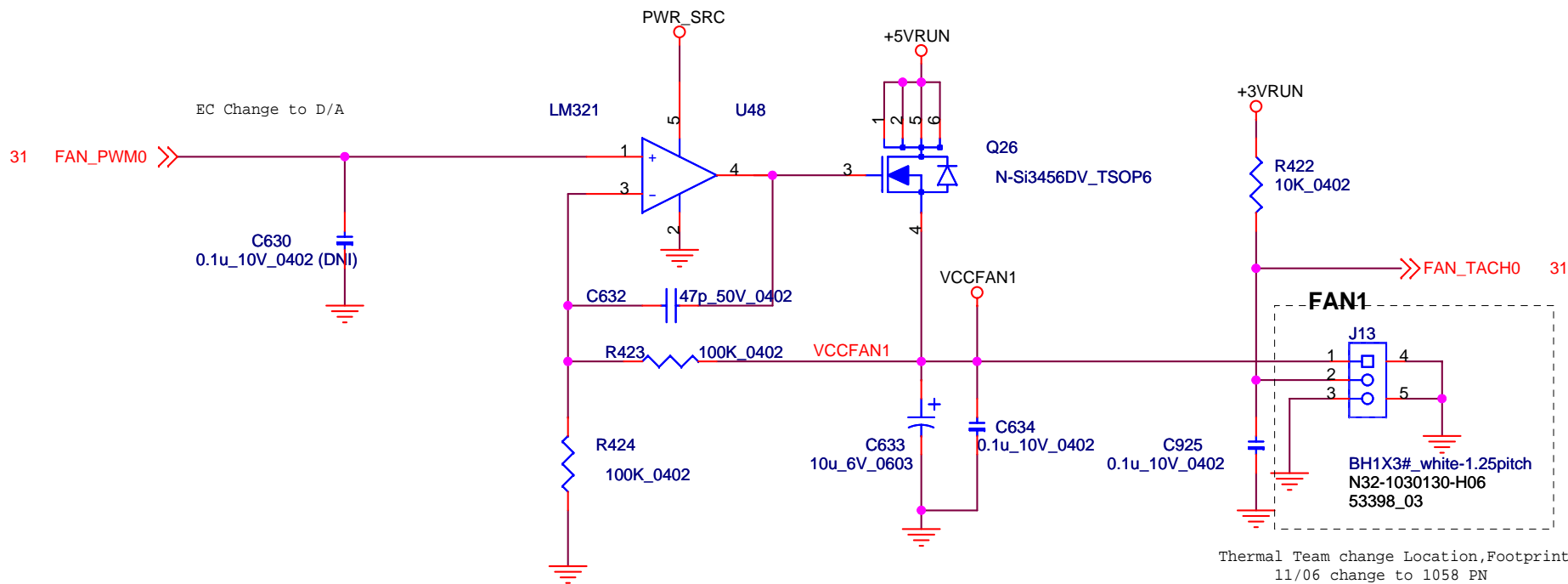
TV TUNER /3G CARD








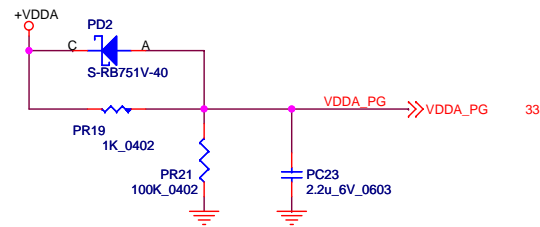
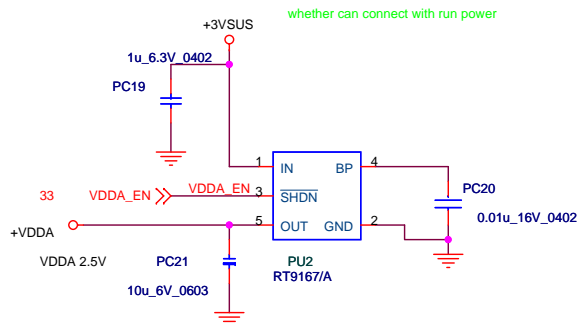
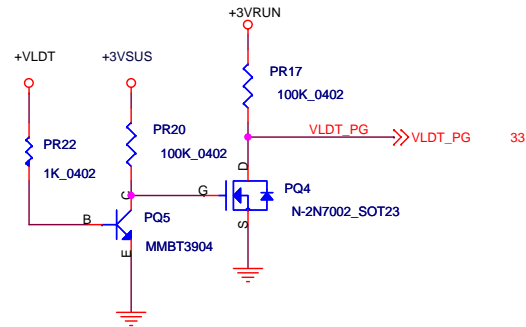
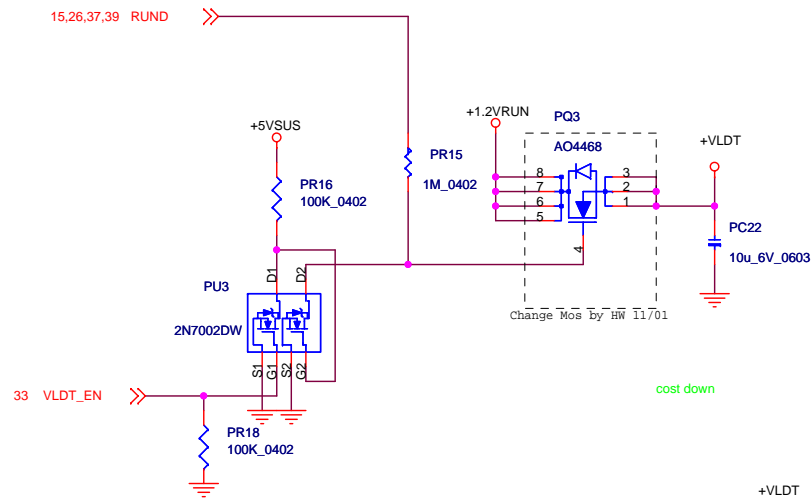
 MICRO-STAR INT'L CO.,LTD.	
Title	
PWRGD	
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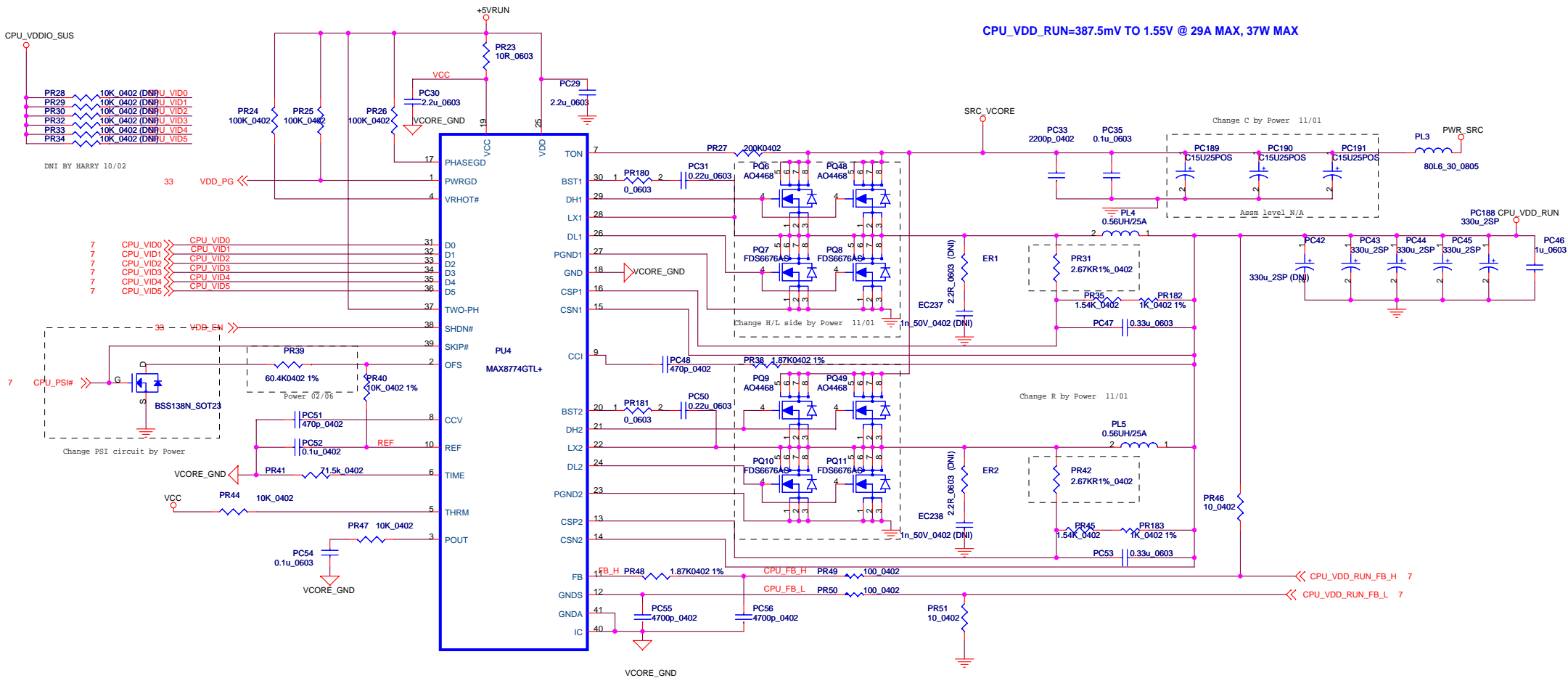
Thermal Team change Location, Footprint and PN
11/06 change to 1058 PN

FOR EMI

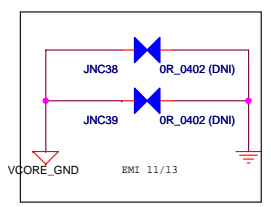
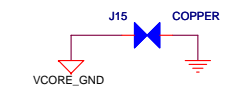
 MSI <small>MICRO-STAR INTERNATIONAL</small> <i>Link to the Future</i>		MICRO-STAR INT'L CO.,LTD.	
Title			
FAN			
Size	Document Number		Rev
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 MICRO-STAR INT'L CO.,LTD.	
Title M 1.2V VDDA 2.5V VLDT	
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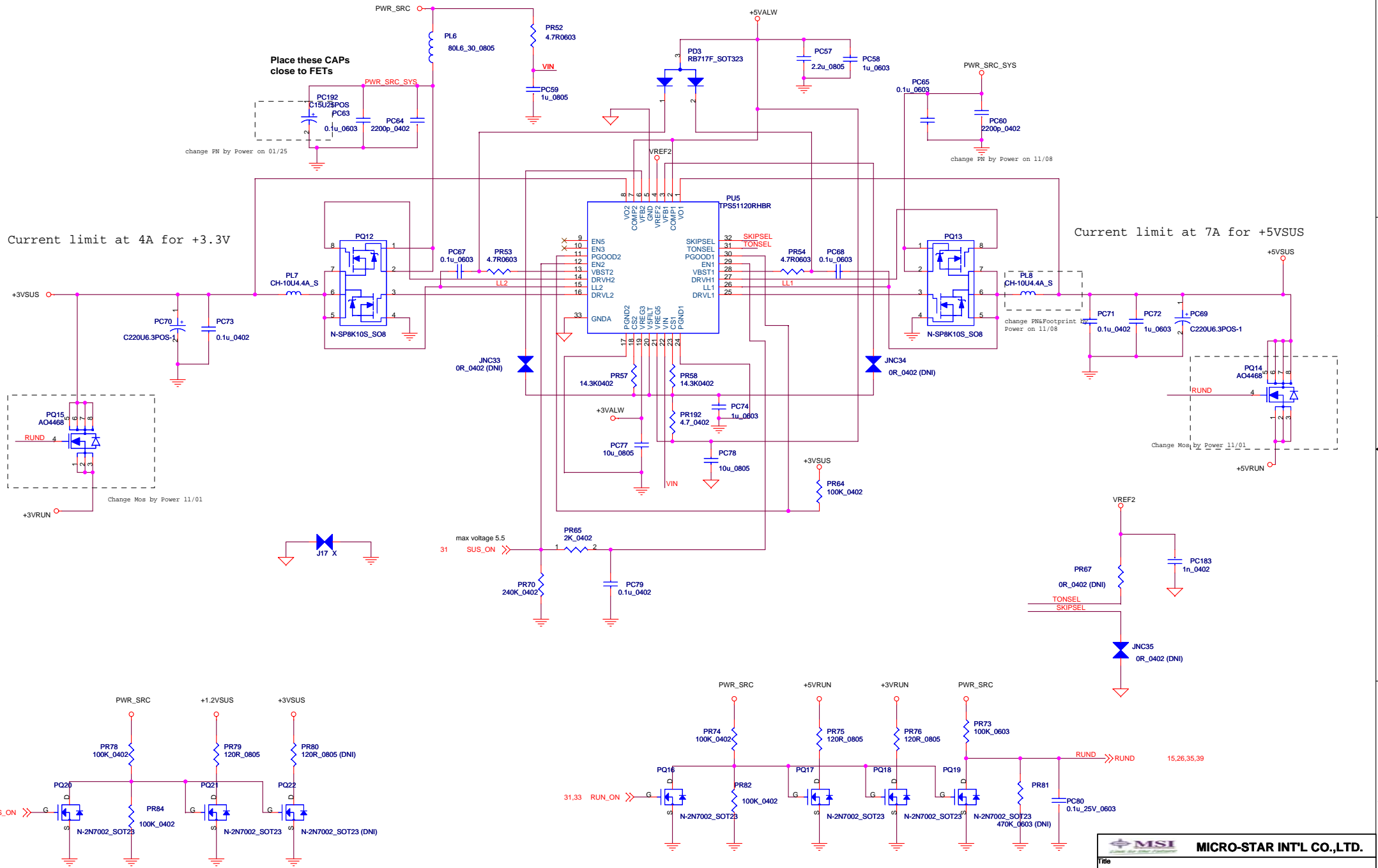
CPU_VDD_RUN=387.5mV TO 1.55V @ 29A MAX, 37W MAX




 MICRO-STAR INT'L CO.,LTD.		
Title VCORE		
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Current limit at 4A for +3.3V

Current limit at 7A for +5VSUS



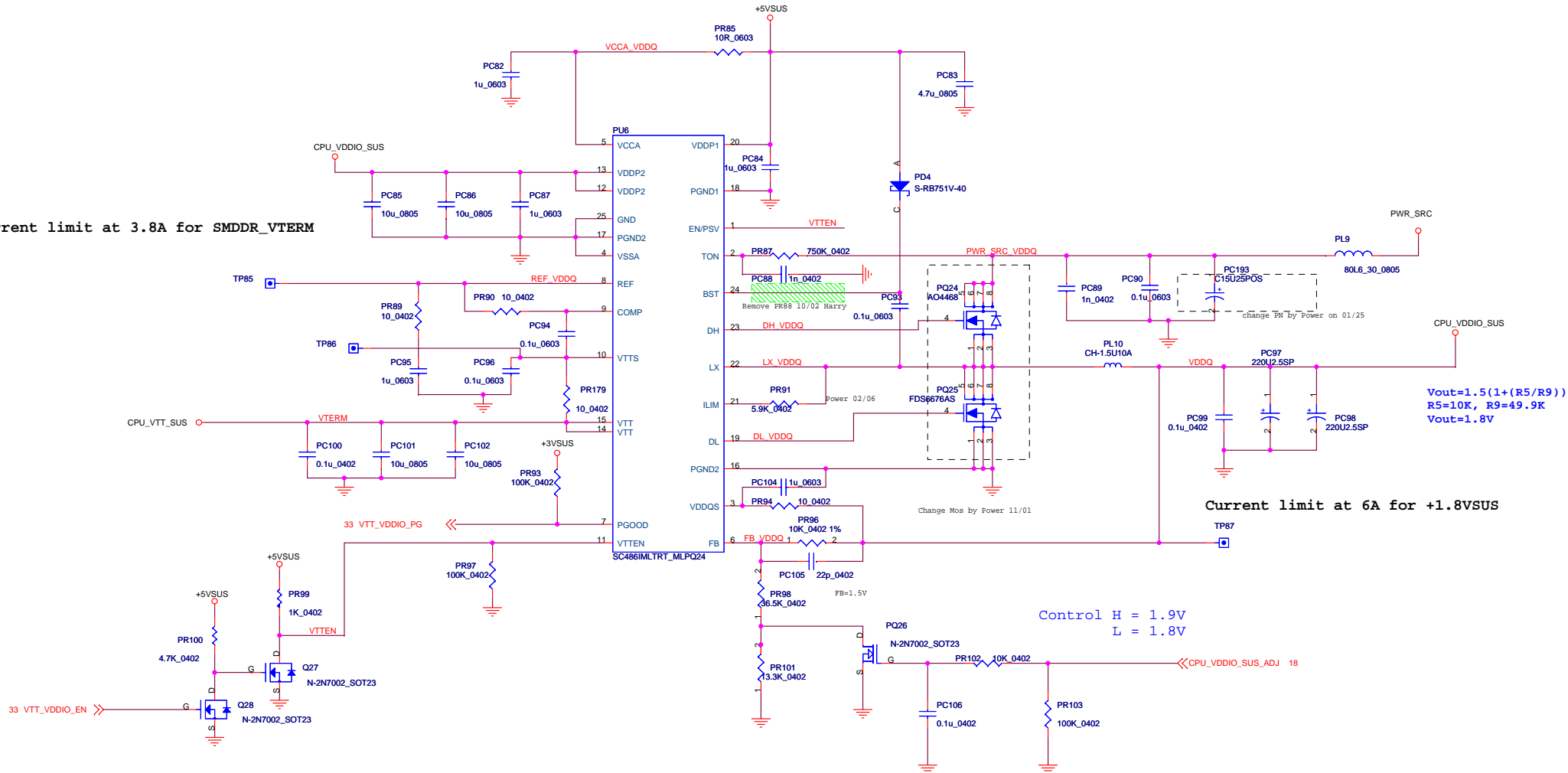
		MICRO-STAR INT'L CO.,LTD.	
SYSTEM POWER 3/5V 2.5VSUS			
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Current limit at 3.8A for SMDR_VTERM

Current limit at 6A for +1.8VSUS

Control H = 1.9V
L = 1.8V

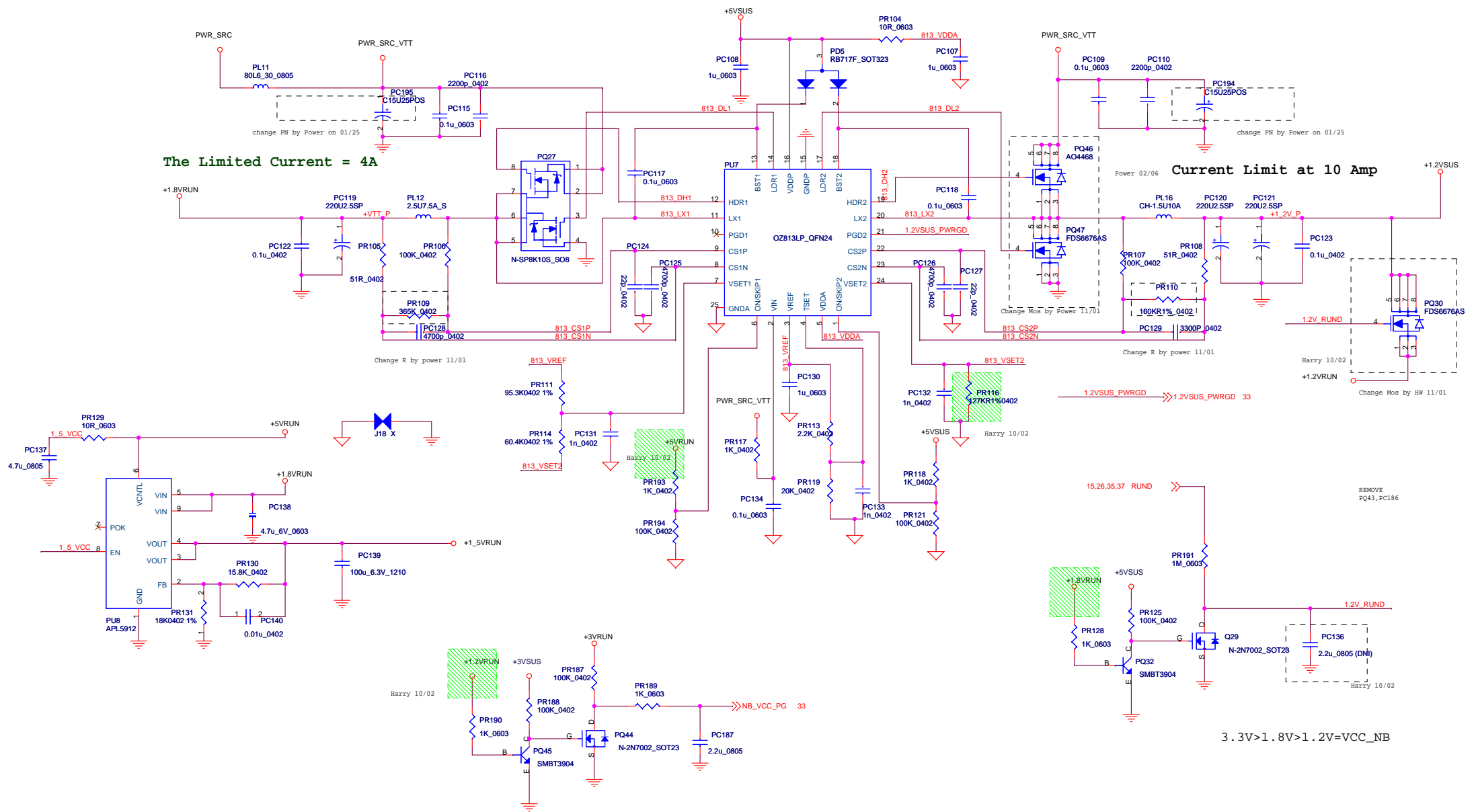
$V_{out} = 1.5(1 + (R5/R9))$
 $R5 = 10K, R9 = 49.9K$
 $V_{out} = 1.8V$




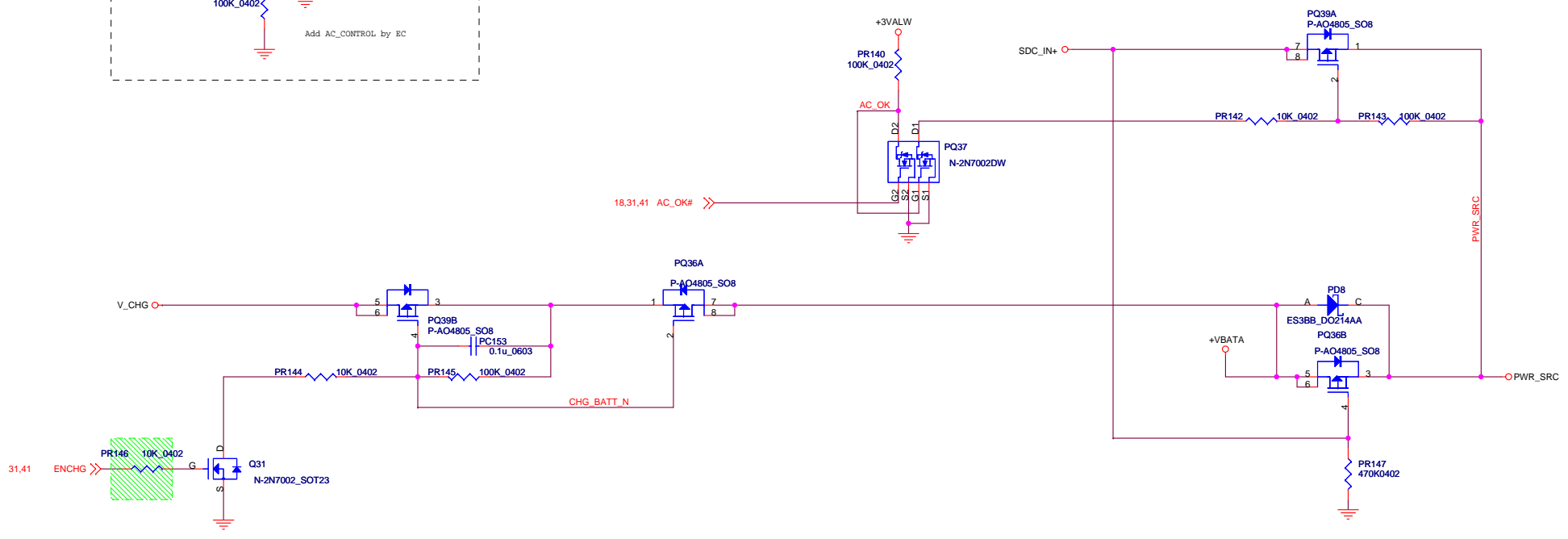
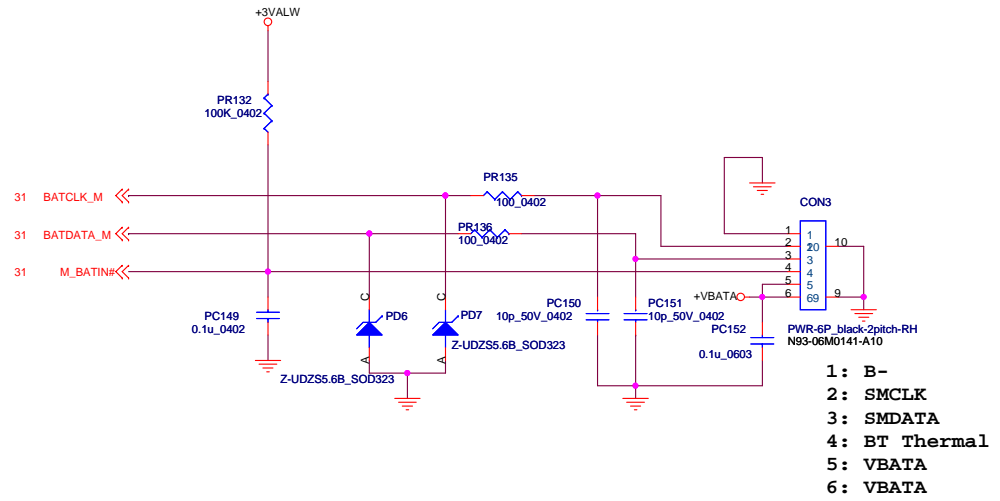
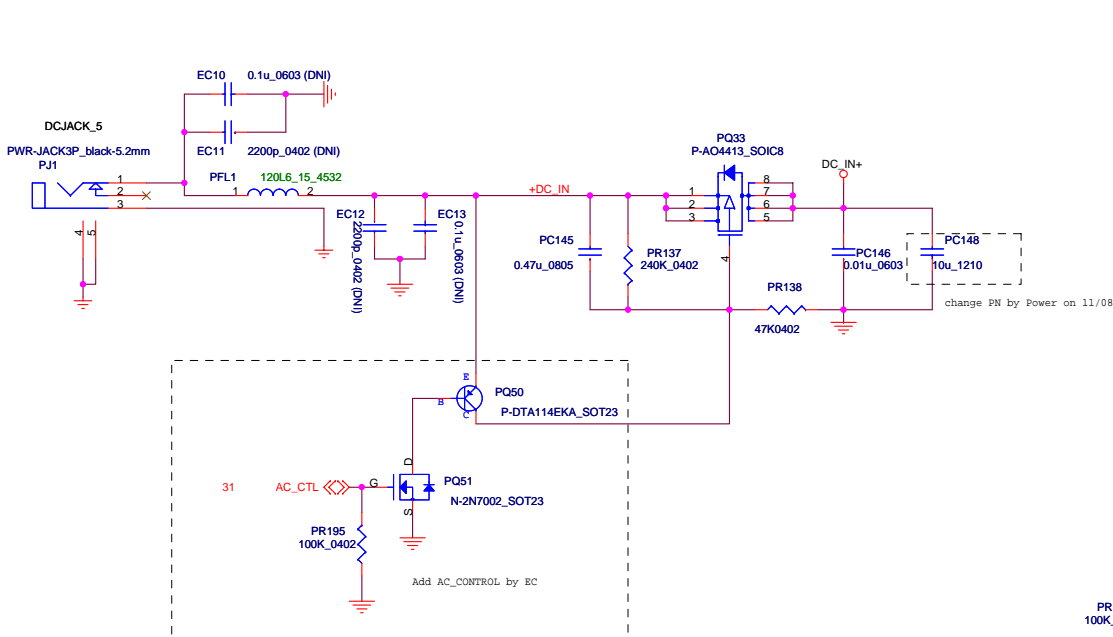
 MICRO-STAR INT'L CO.,LTD.	
Title DDR2 1.8V VTT 0.9V	
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The Limited Current = 4A

Current Limit at 10 Amp

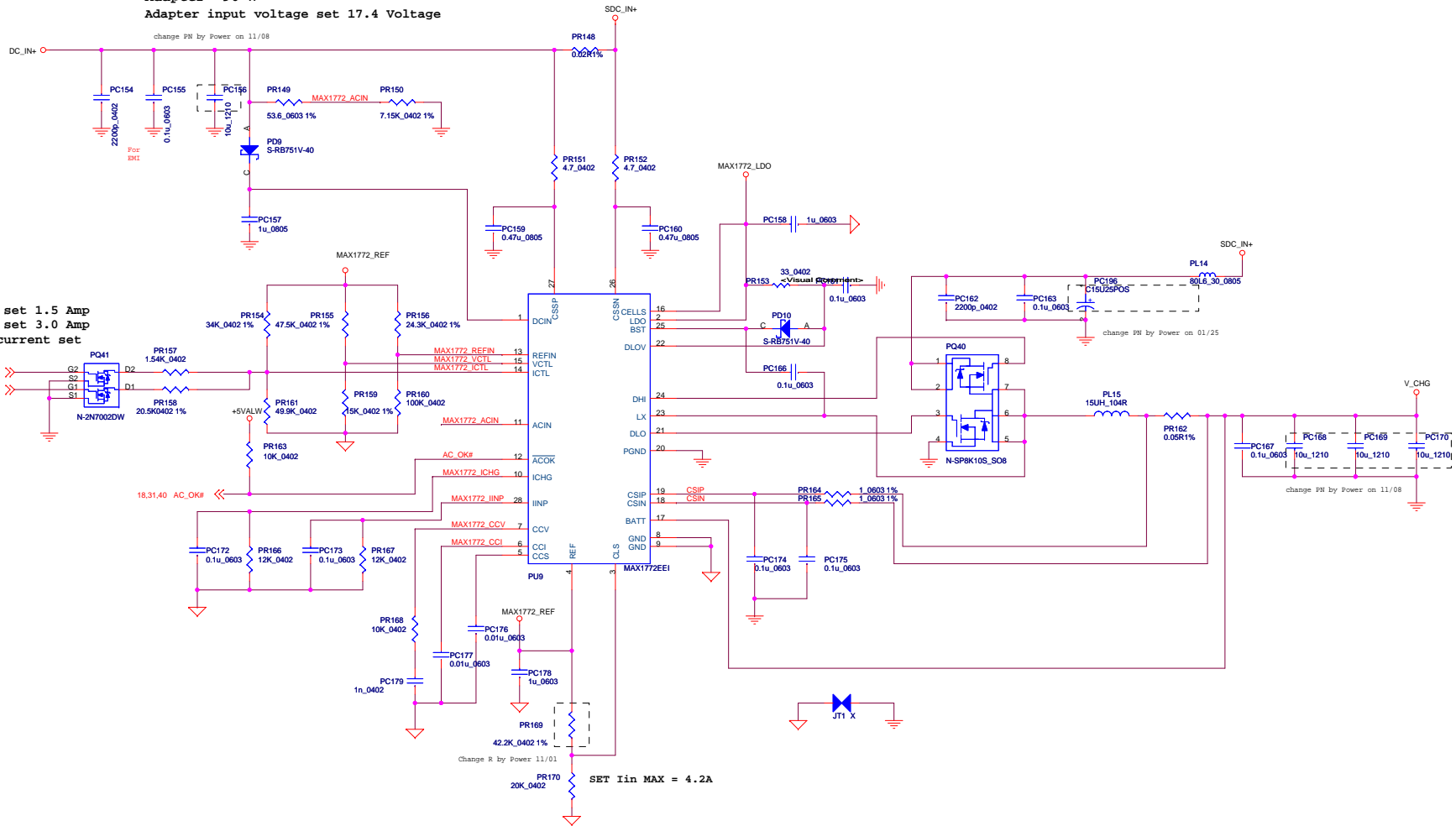


 MICRO-STAR INT'L CO.,LTD.	
Title VCC NB 1.2VSUS 1.5VRUN 1.8VRUN	
Size	Document Number
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Title Battery Select	
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Adapter = 90 W
 Adapter input voltage set 17.4 Voltage



4S1P: Charge current set 1.5 Amp
 4S2P: Charge current set 3.0 Amp
 Pre-charger: Charge current set 200mA

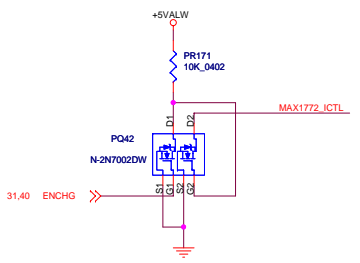
31 PRE_CHG
 31 ENCHG_1P

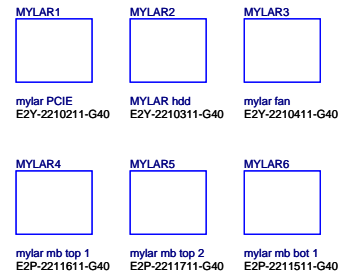
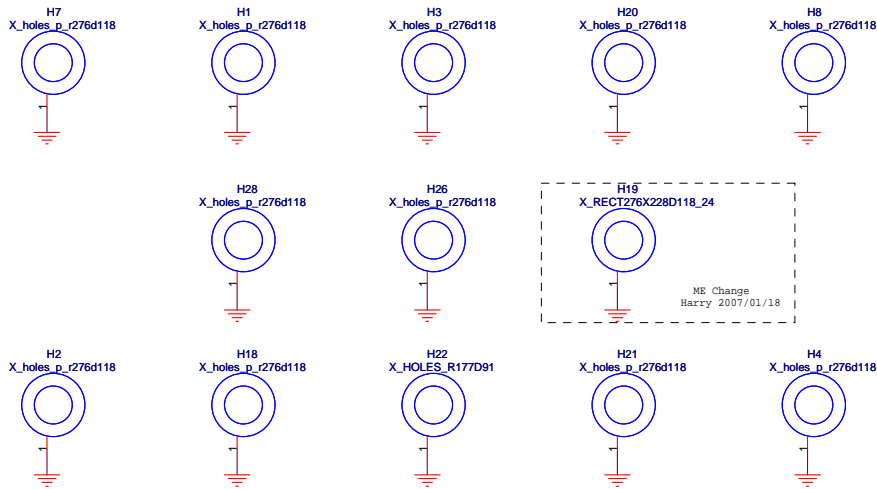
18.3140 AC_OK#

Change R by Power 11/01
 SET I_{in} MAX = 4.2A

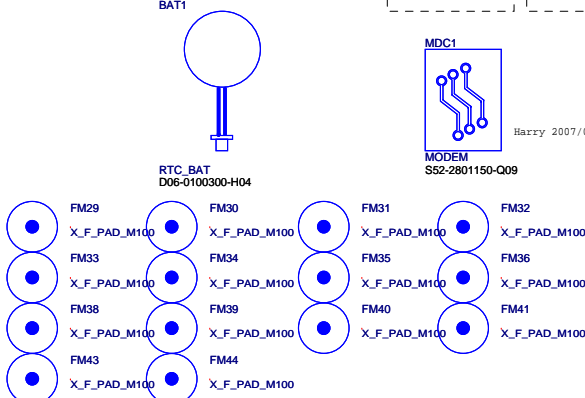
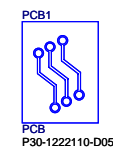
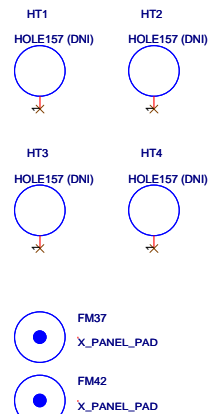
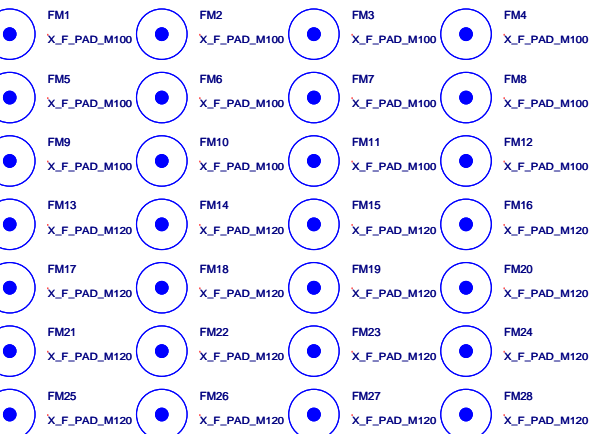
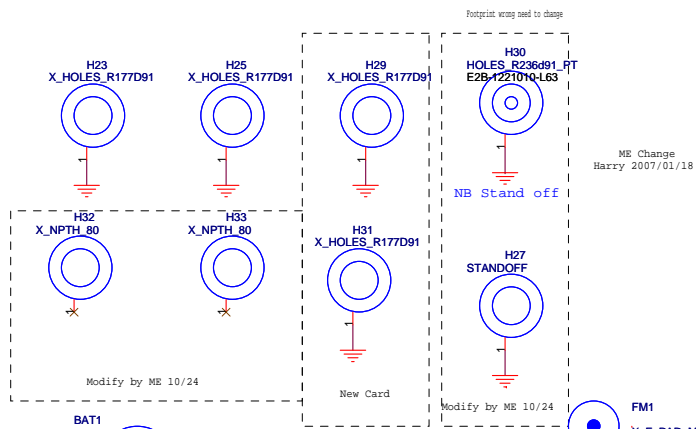
ENCHG-1P	PRE_CHG	ENCHG	
0	1	1	Pre-charge
1	0	1	4S1P-Fast charge
X	X	0	STOP CHARGE

Define on 4S2P charge current

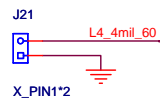
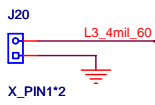




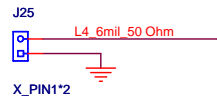
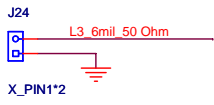
CPU HEATSINK



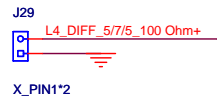
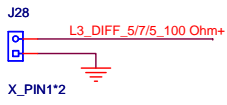
MICRO-STAR INT'L CO.,LTD.		
Title ME Parts		
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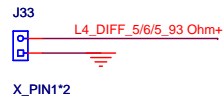
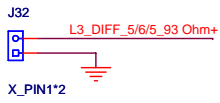
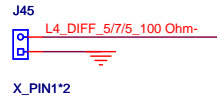
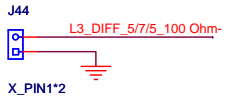
Normal Signal 60 Ohm



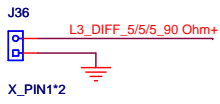
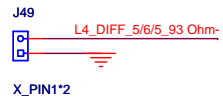
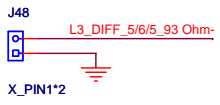
RGB Signal 50 Ohm



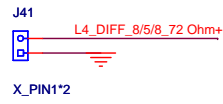
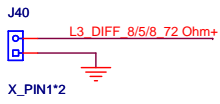
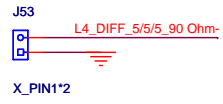
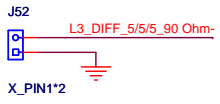
Differential Pair 100 Ohm



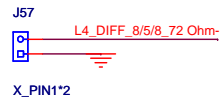
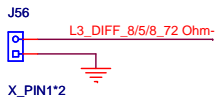
Differential Pair 93 Ohm




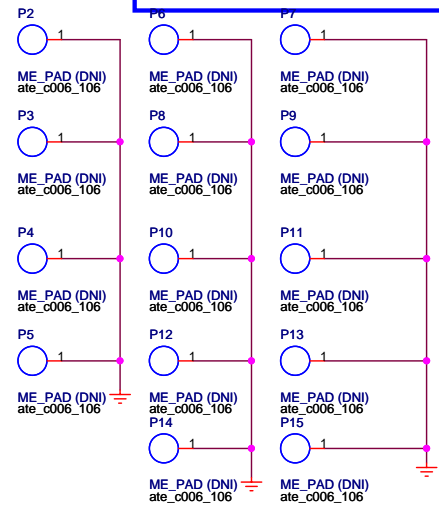
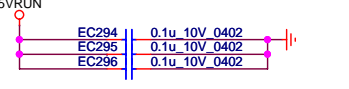
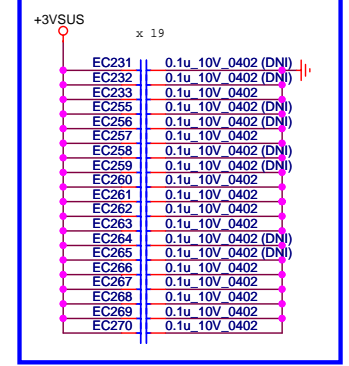
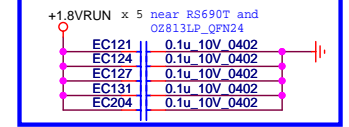
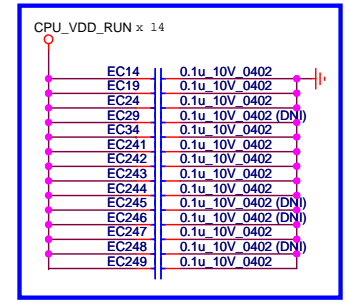
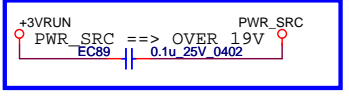
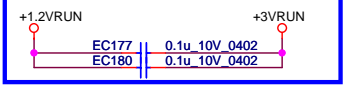
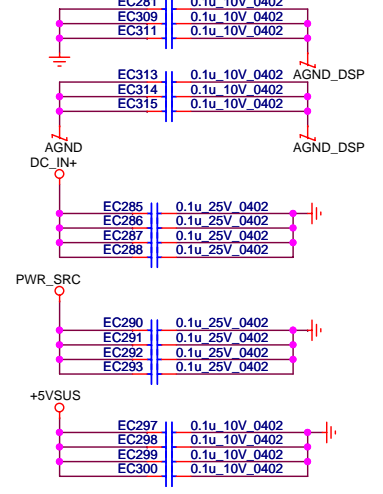
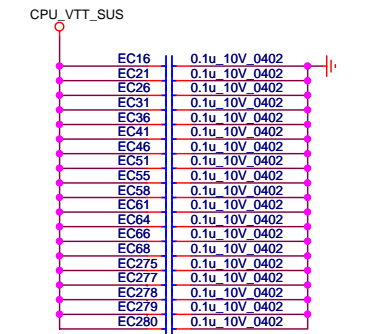
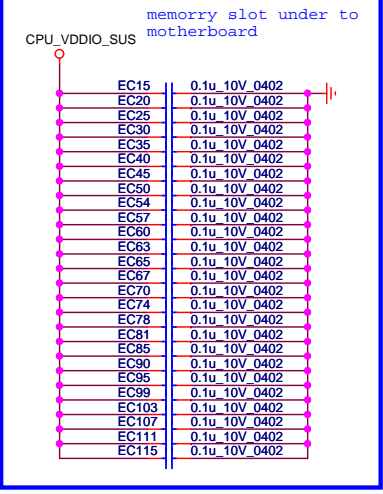
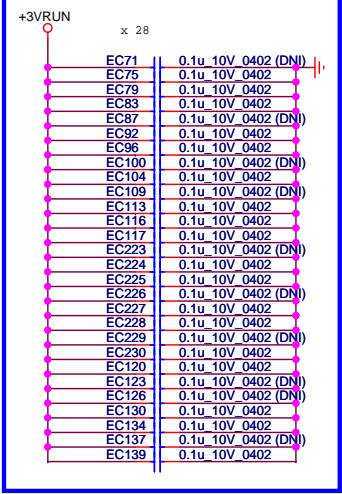
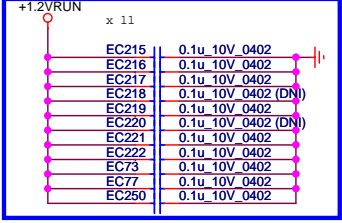
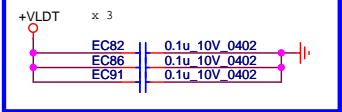
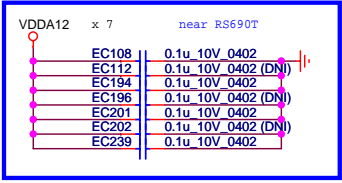
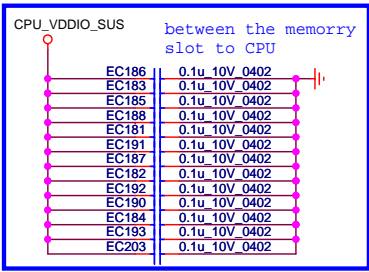
Differential Pair 90 Ohm



Differential Pair 72 Ohm



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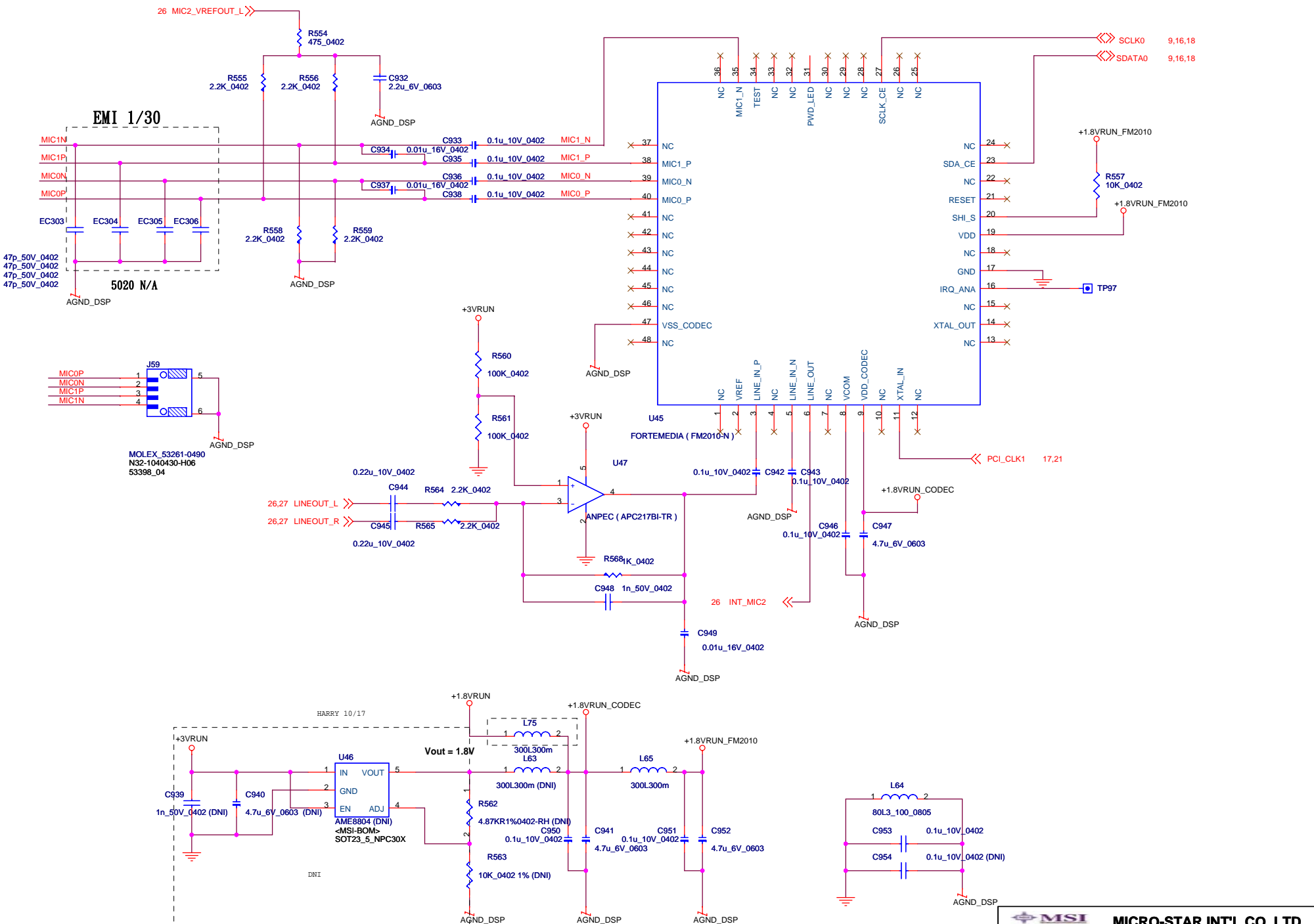
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$$V_{out} = 1.215(R_u + R_d) / R_d$$

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