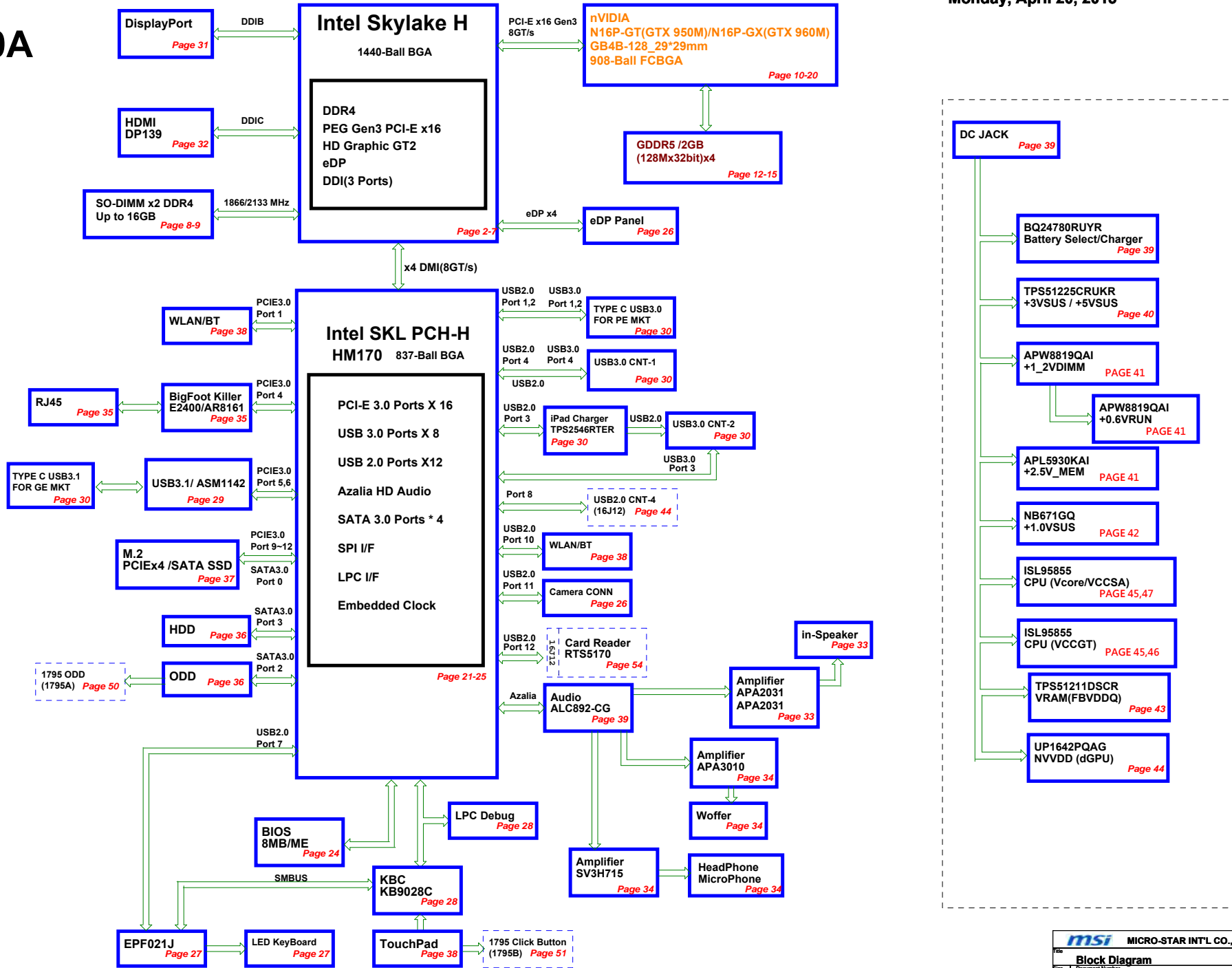


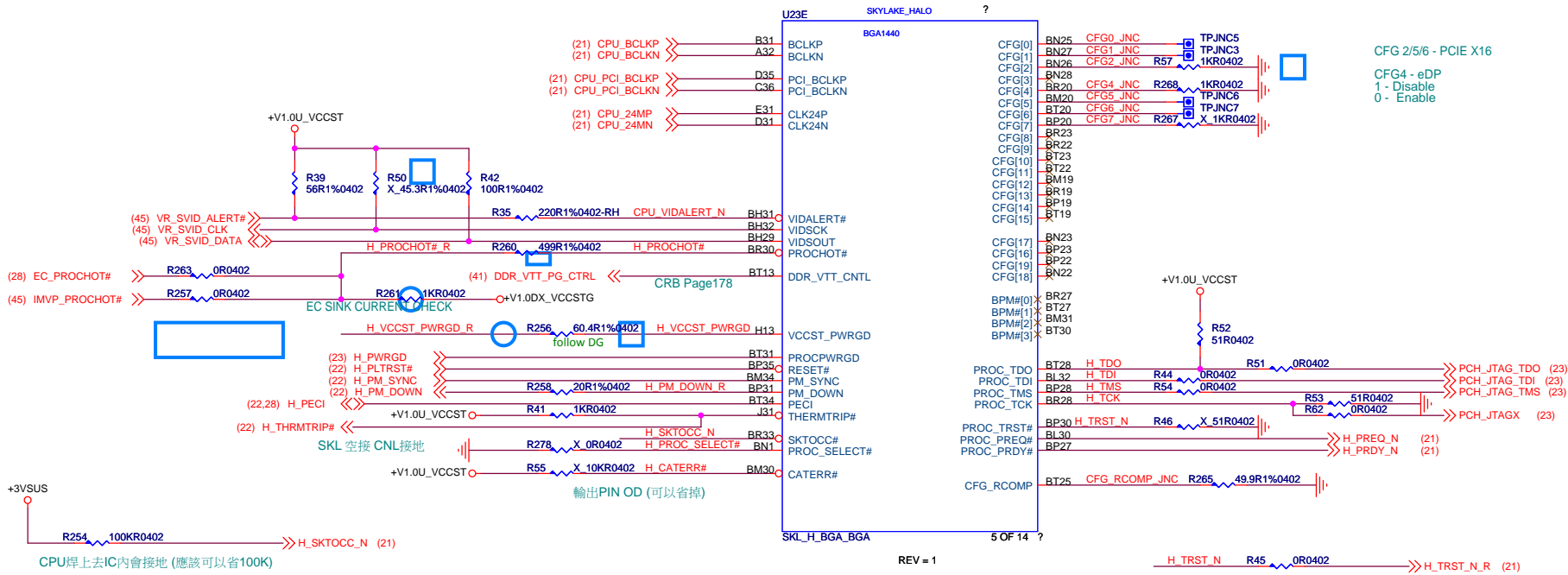
MS-16J5/MS-1795

Intel Skylake Mobile

Ver:0A

Monday, April 20, 2015





CFG 2/5/6 - PCIE X16
 CFG4 - eDP
 1 - Disable
 0 - Enable

MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

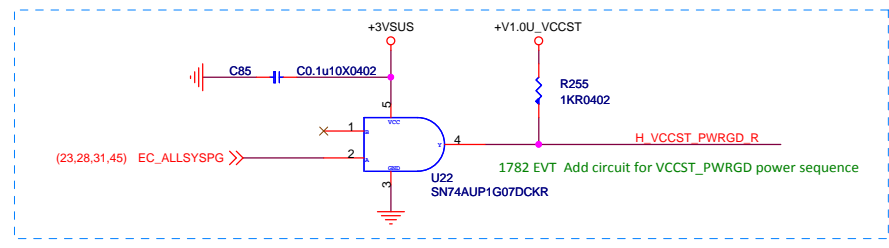
eDP Enable	
CFG4	1 = Disabled 0 = Enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESET# de assertion 0: PEG Wait for BIOS for training

PCIE Express * Static X16 Lane Numbering Reversal	
CFG2	CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. 1 = Normal operation 0 = Lane numbers reversed.

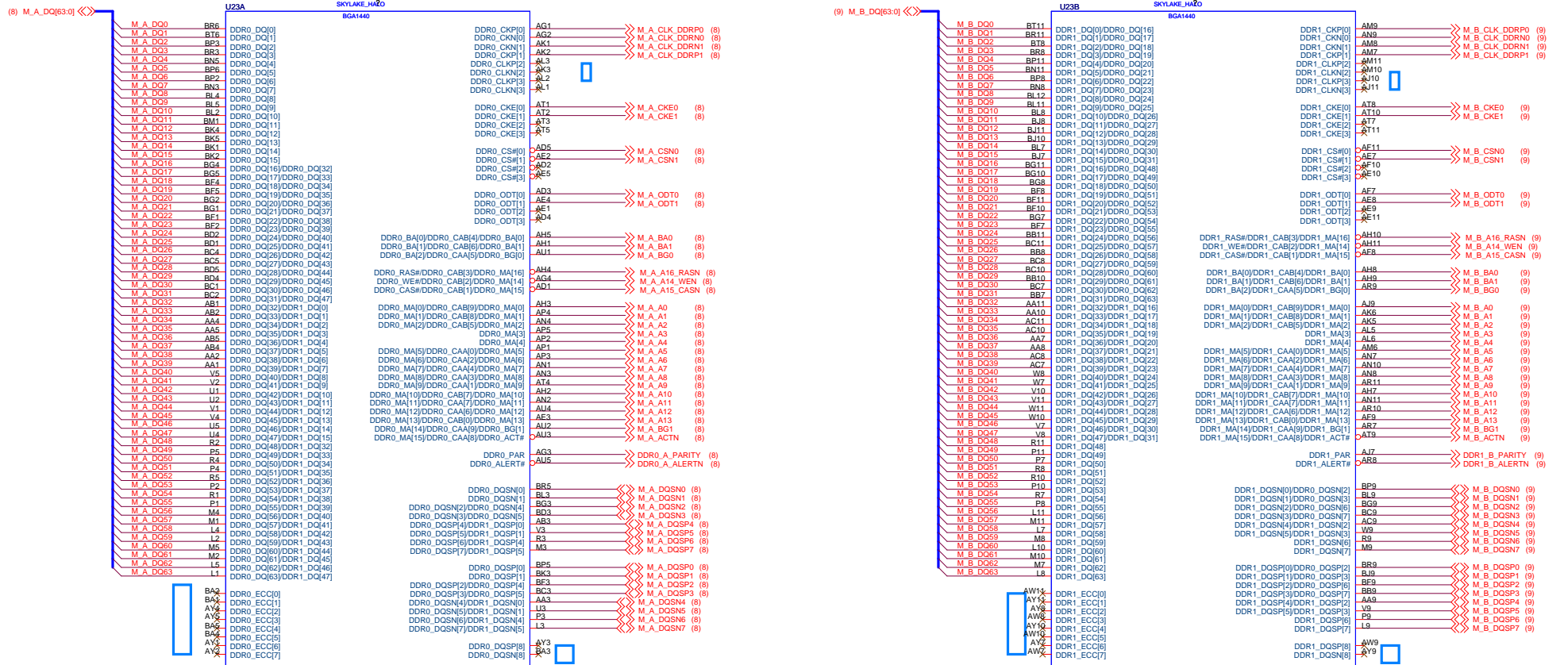
PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express*

Intel 54492 Page 37,121



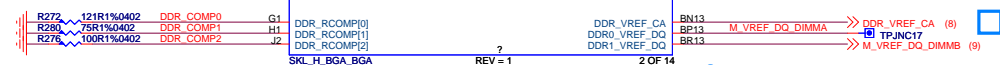
DDR Channel A

DDR Channel B



DDR CHANNEL A

DDR CHANNEL B



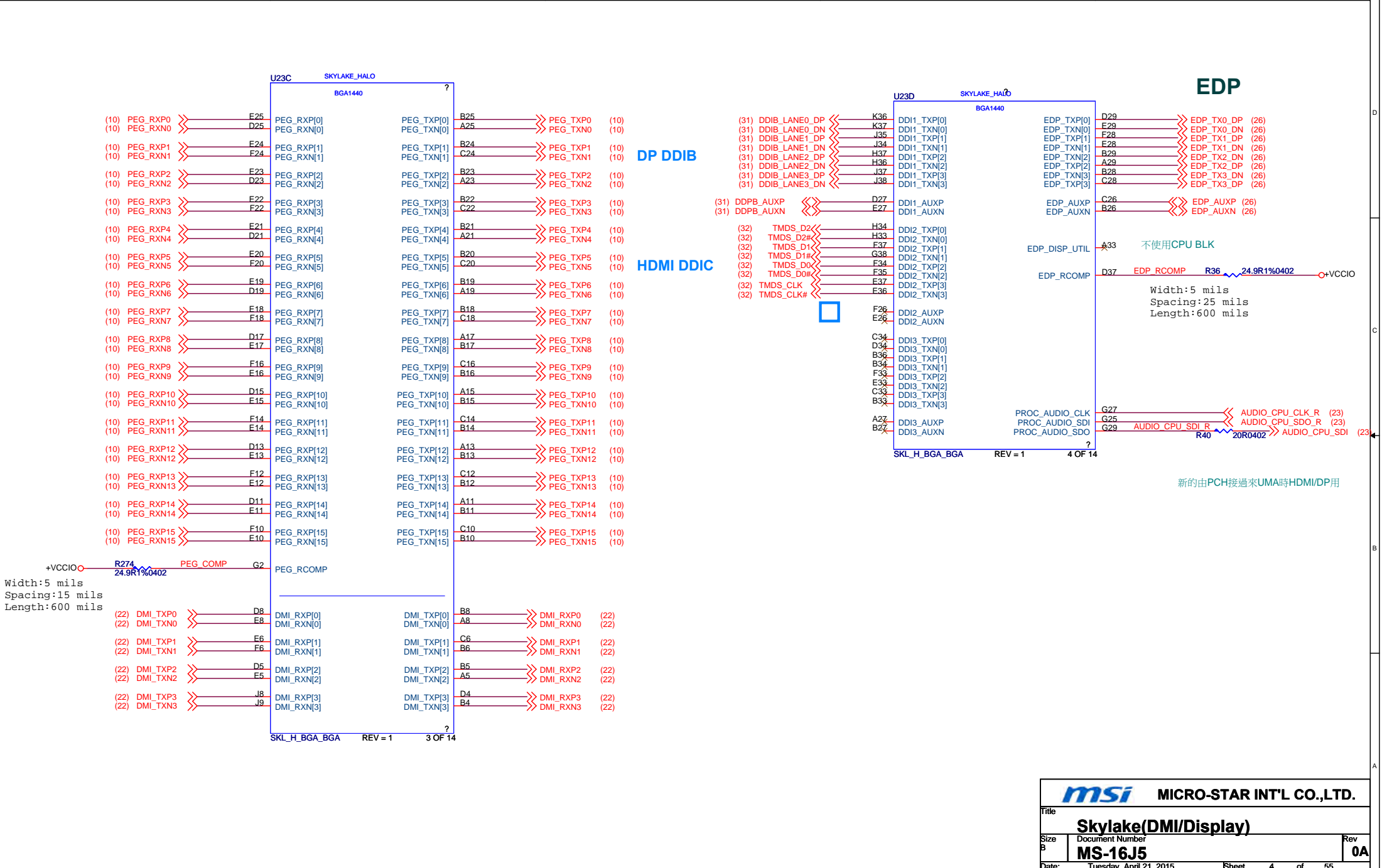
DG Page 157

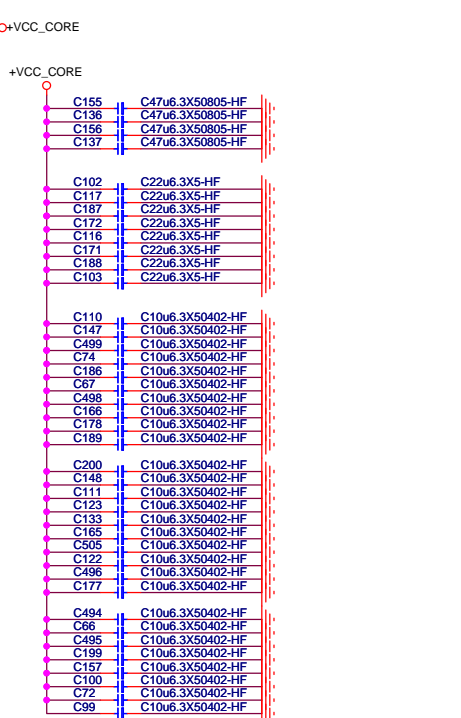
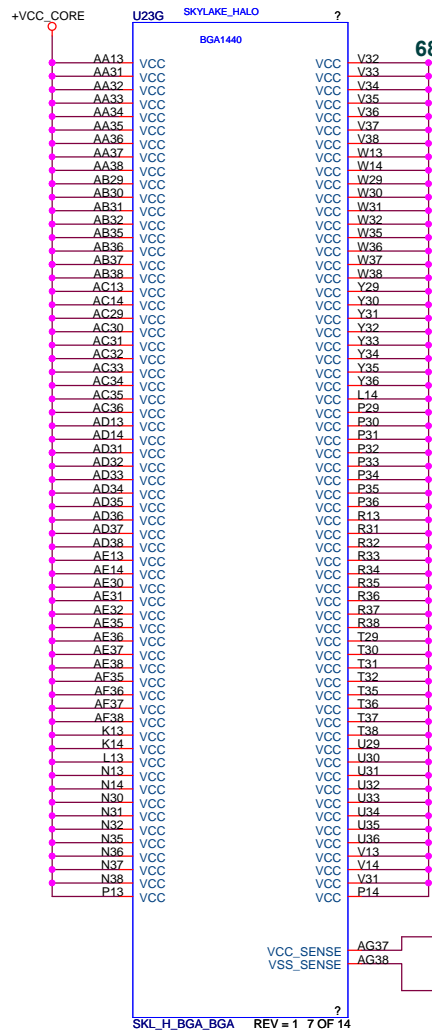
msi MICRO-STAR INT'L CO.,LTD.

Title: **Skylake(DDR4)**

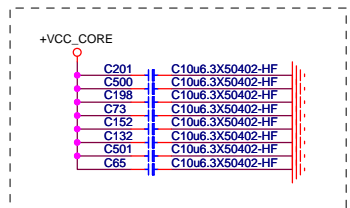
Size: **MS-16J5** Document Number: **MS-16J5** Rev: **0A**

Date: **Tuesday, April 21, 2015** Sheet **3** of **55**





少63顆0201 1uF電容
 10uF 換幾顆1uF 靠近BALL C11-105A312-M09(X6S)
 10uF 更改FOOTPRINT



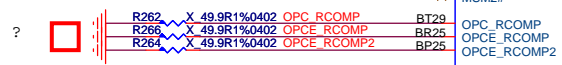
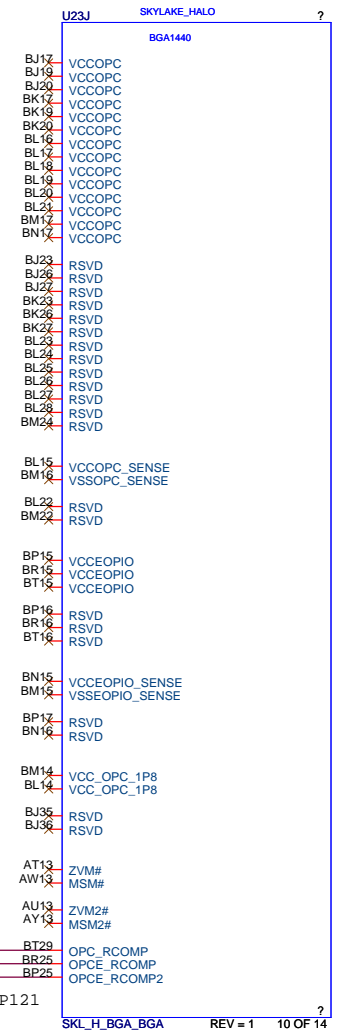
GT4 Power

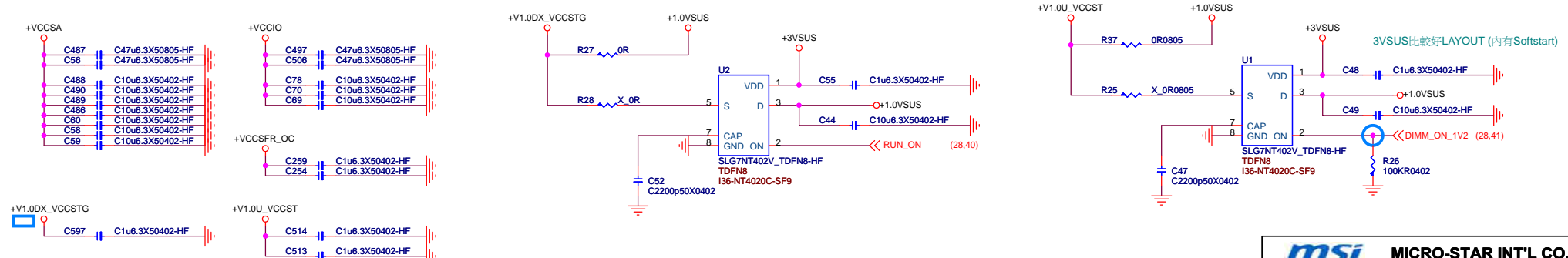
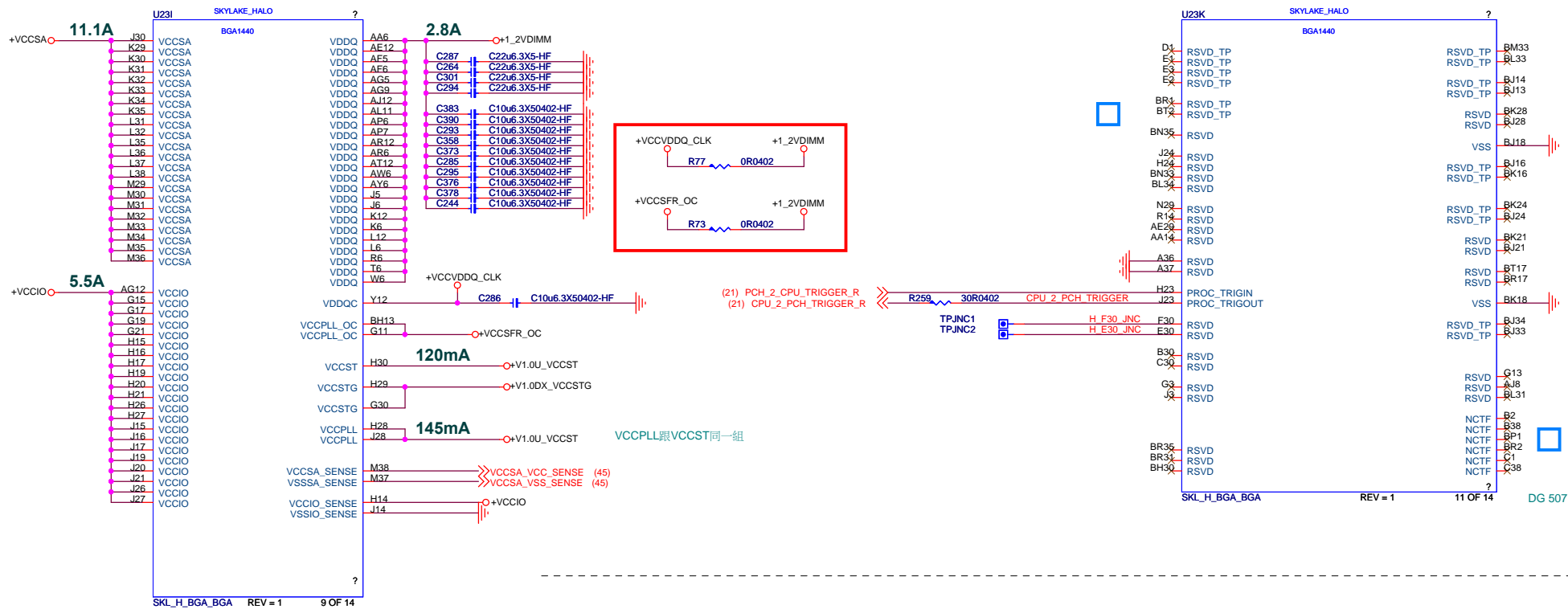
GT4 Power

GT4 Power

Unconnected for Processors without OPC. EDS.P121

VCCGTx, VCCOPC, VCCOPC_lp8, VCCEOPIO is only applicable to SKUs with OPC



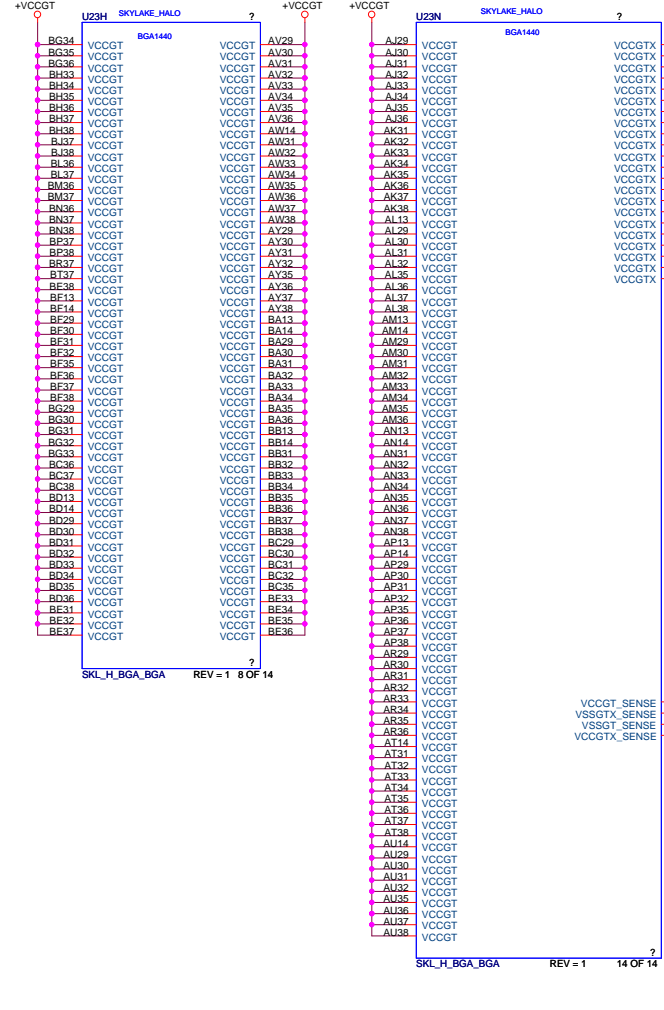
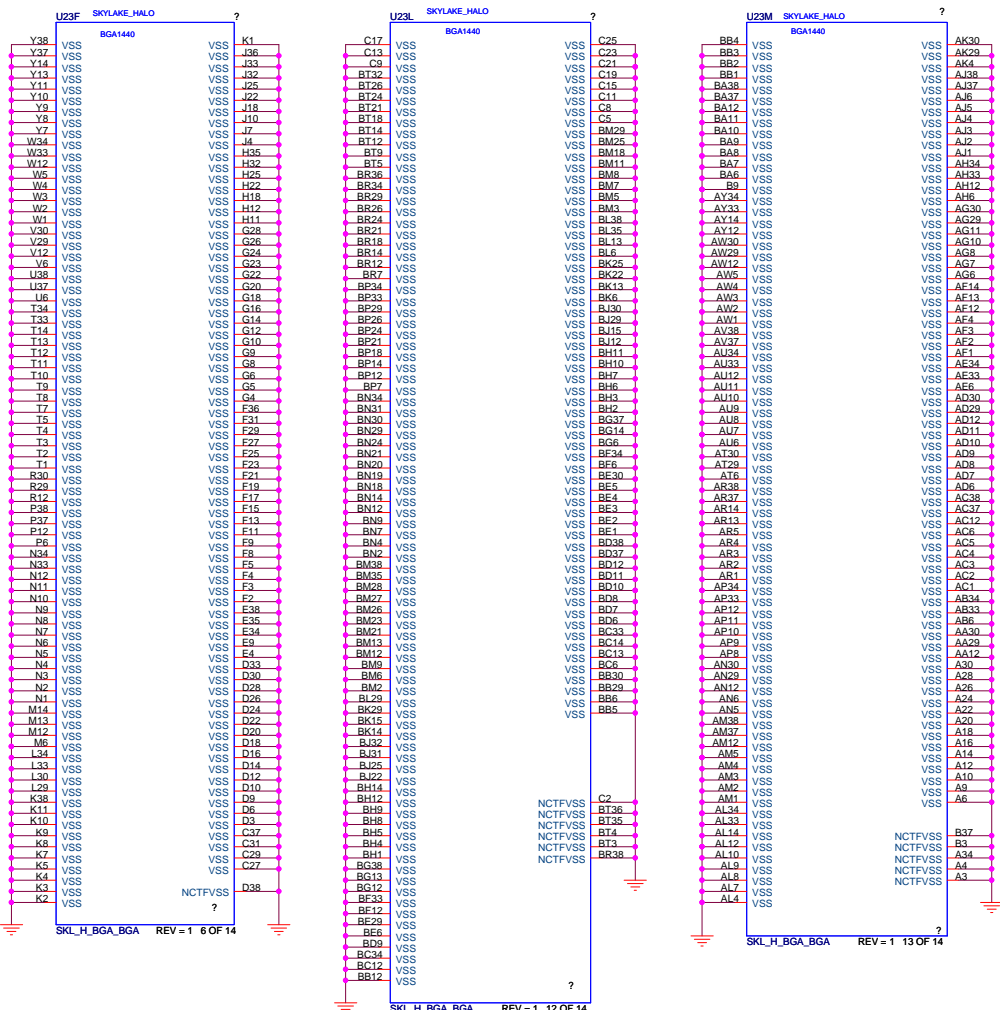


msi MICRO-STAR INT'L CO.,LTD.

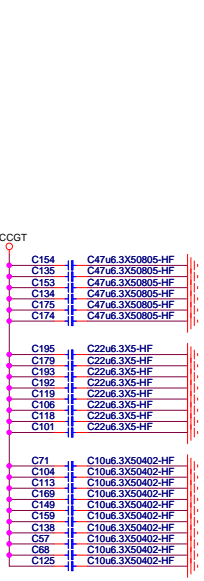
Title: **Skylake(Power2)**

Size: Custom Document Number: **MS-16J5** Rev: **0A**

Date: Tuesday, April 21, 2015 Sheet: 6 of 55

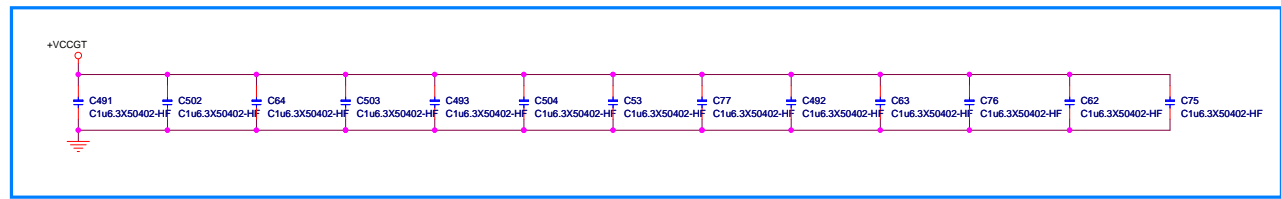


GT2 55A

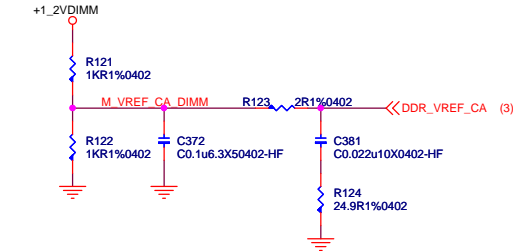
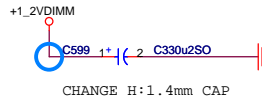
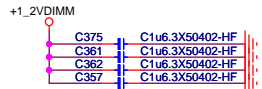
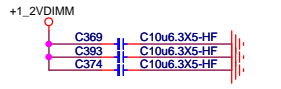
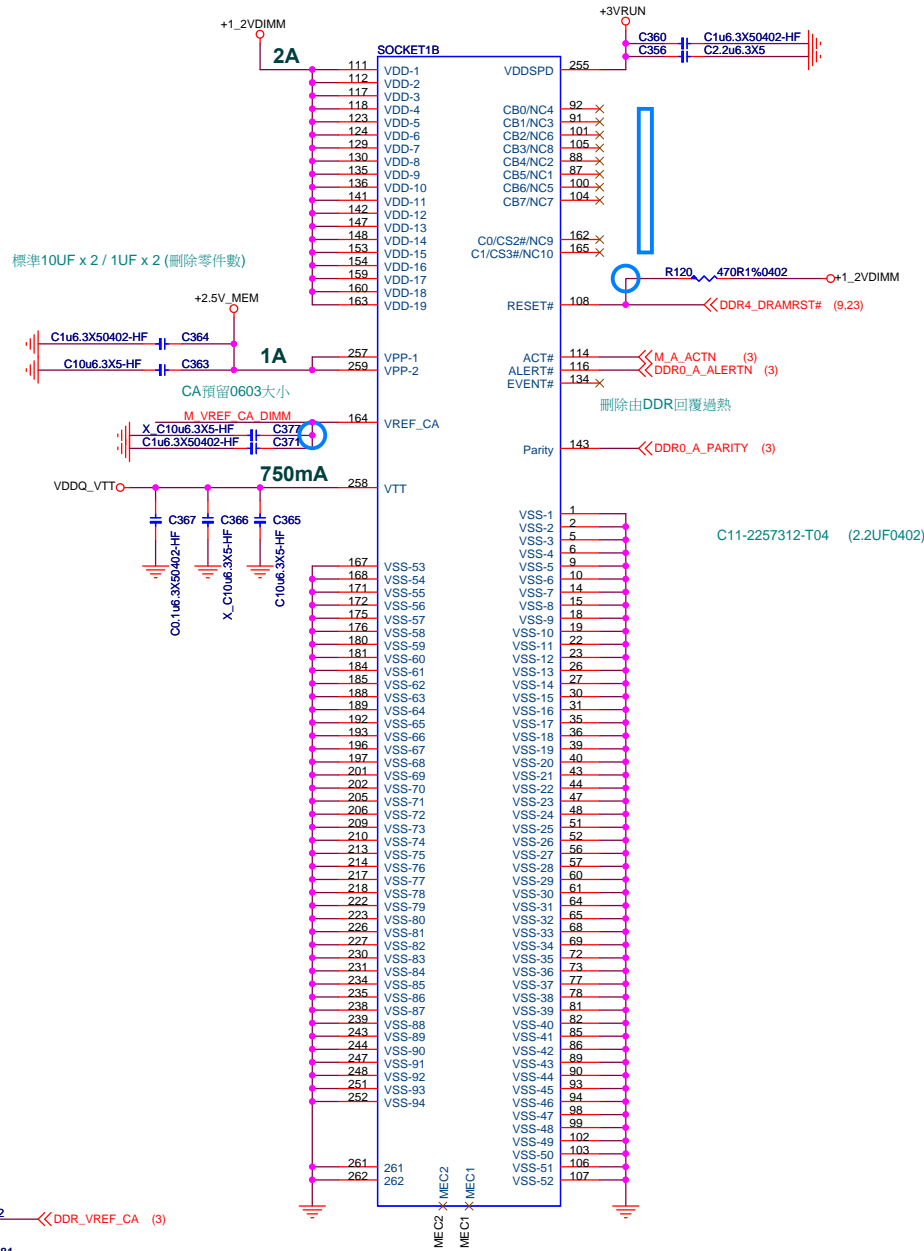
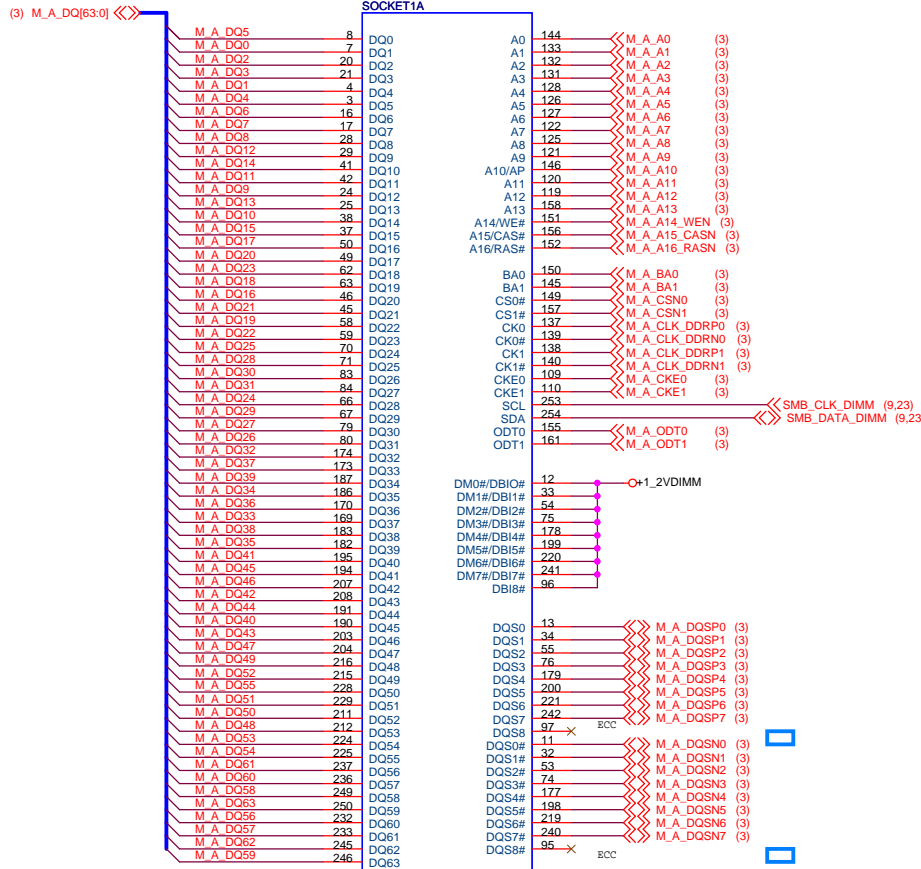


VCCGT_SENSE
 VSSGTX_SENSE
 VSSGT_SENSE
 VCCGTX_SENSE

→VCCGT_VCC_SEN (45)
 →VCCGT_VSS_SEN (45)



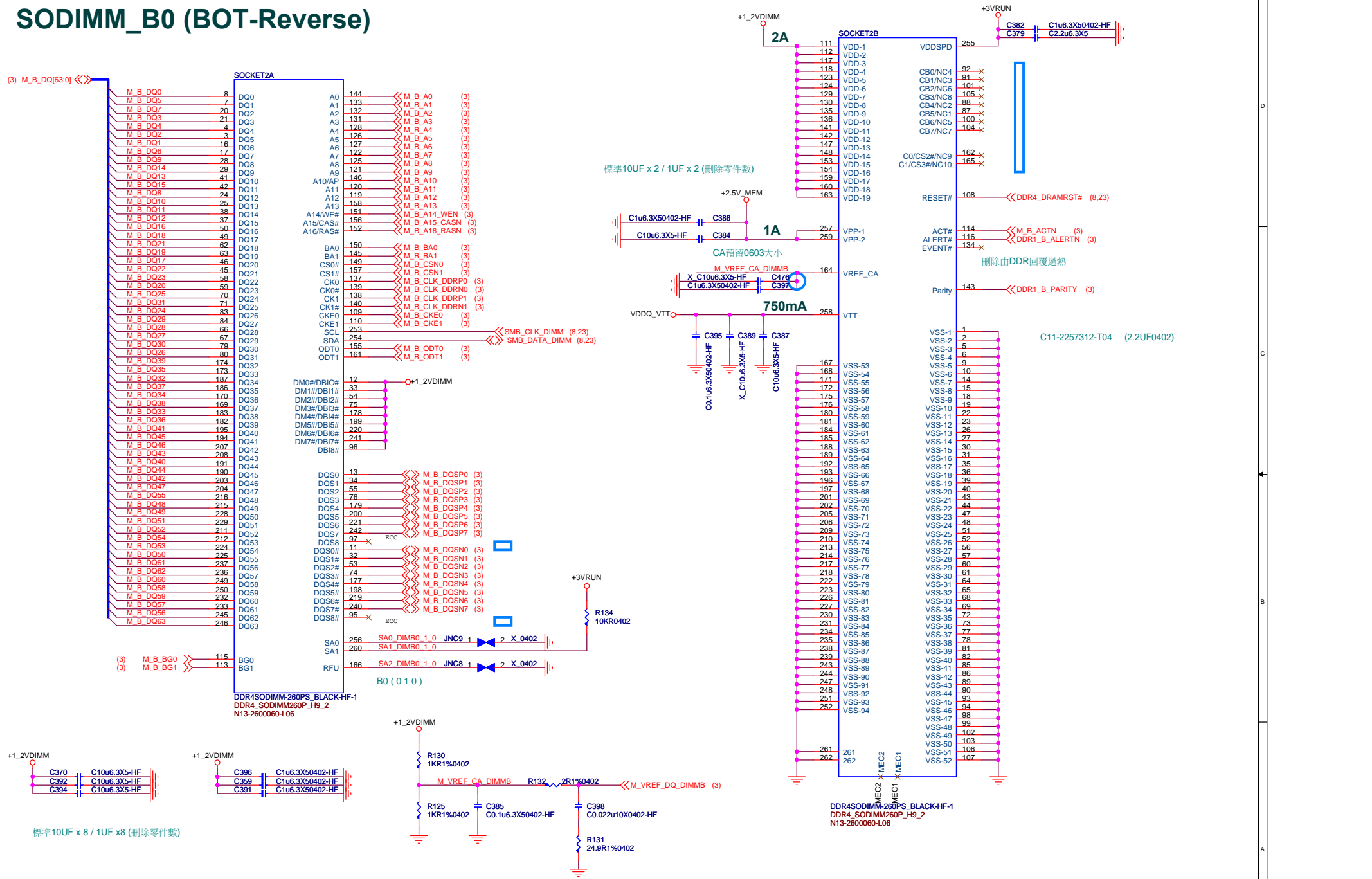
SODIMM_A0 (BOT-Reverse)



DDR4SODIMM-260PS_BLACK-HF-1
DDR4_SODIMM260P_H5_2_1
N13-2600050-L06

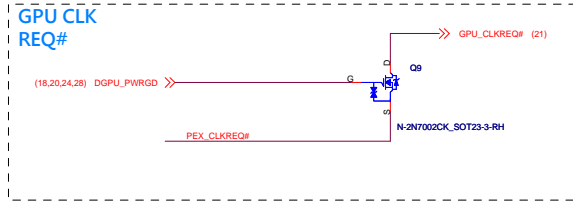
msi MICRO-STAR INT'L CO.,LTD.		
Title DDR4 SODIMM A0		
Size	Document Number	Rev
Custom	MS-16J5	0A
Date:	Tuesday, April 21, 2015	Sheet 8 of 55

SODIMM_B0 (BOT-Reverse)



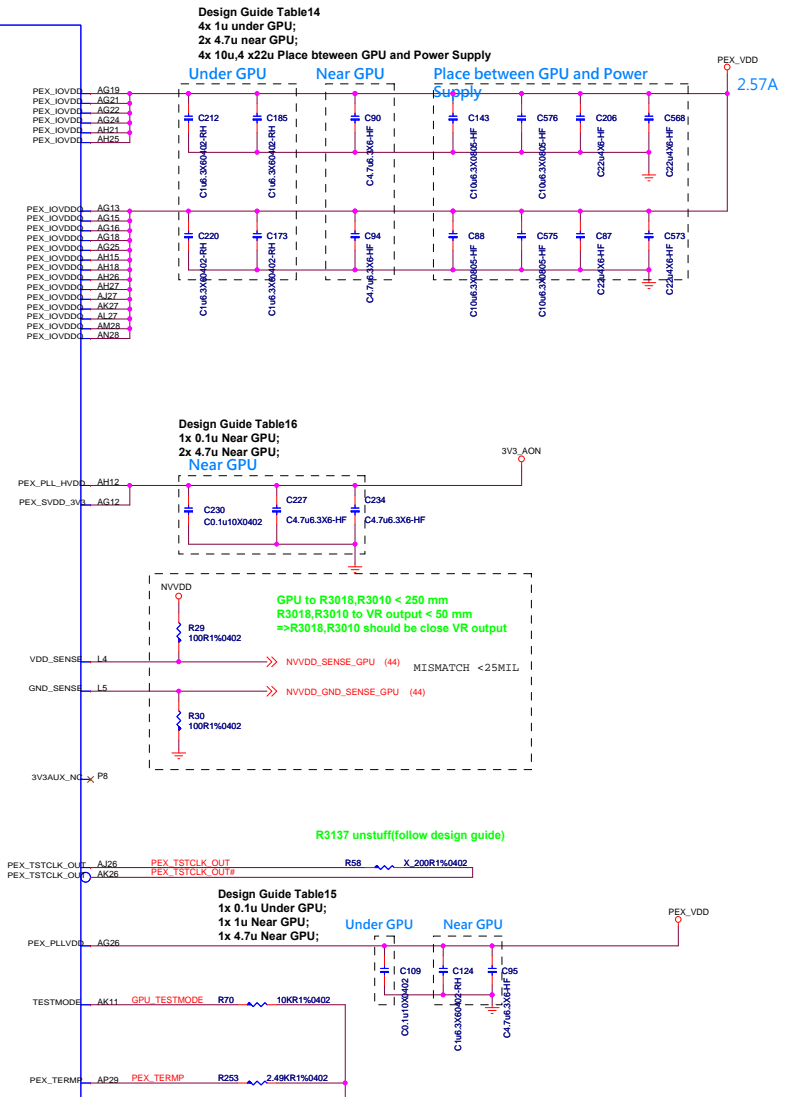
msi MICRO-STAR INT'L CO.,LTD.		
Title DDR4 SODIMM B0		
Size	Document Number	Rev
Custom	MS-16J5	0A
Date:	Tuesday, April 21, 2015	Sheet 9 of 55

N16P-GX(PCI-Express Gen3 x16 Interface)



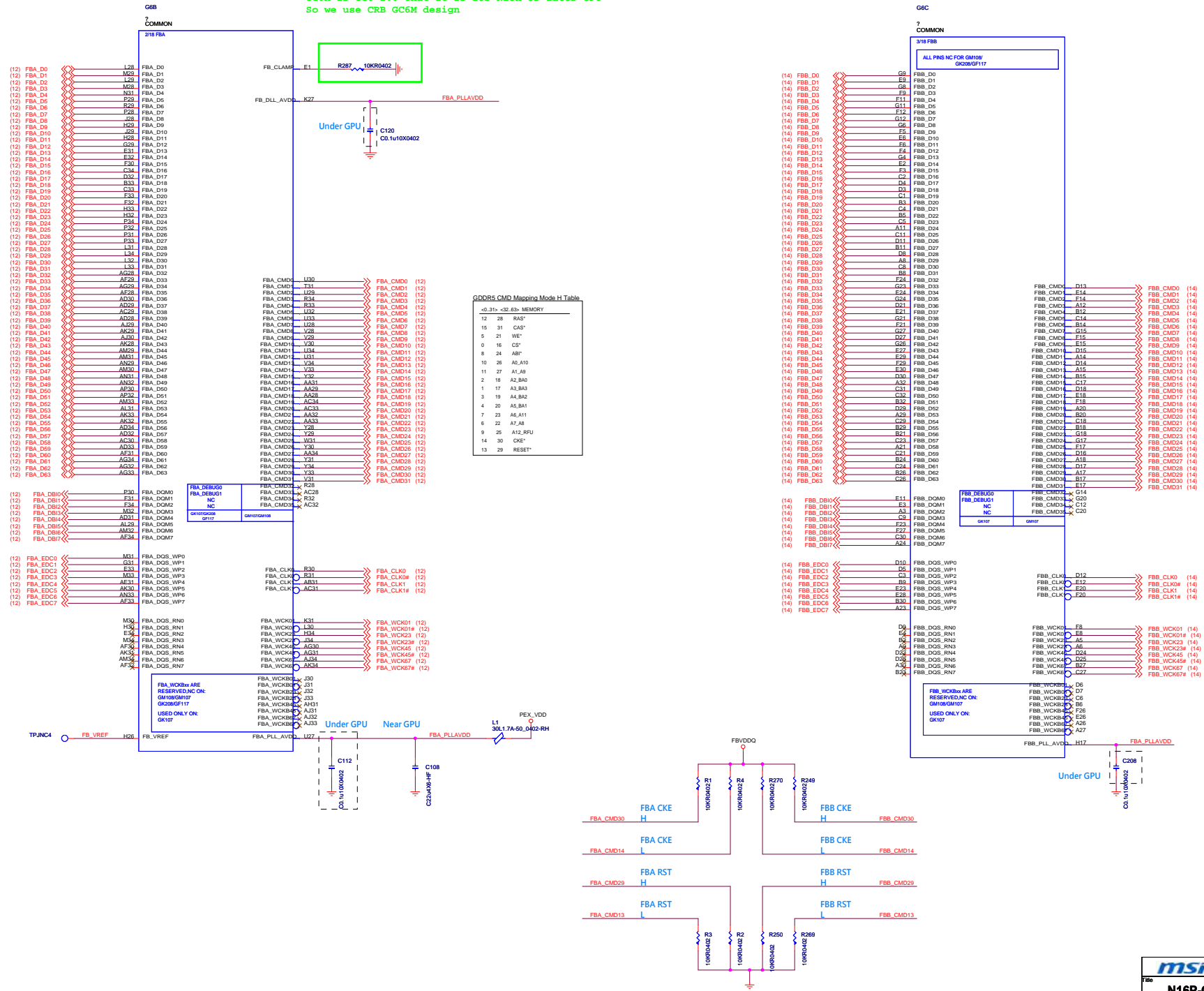
GTX950
 B03-0N16P05-N08
 X_N16P-GT-A2

Signal	Component	Value	Location
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(4) PEG_TXN15	C563	C0.22u16X0402-HF	PEG C RXN15_JNC
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(4) PEG_RXN14	C249	C0.22u16X0402-HF	PEG C TXN14_JNC
(4) PEG_TXP14	C561	C0.22u16X0402-HF	PEG C RXP14_JNC
(4) PEG_RXN14	C562	C0.22u16X0402-HF	PEG C RXN14_JNC
(4) PEG_RXP13	C229	C0.22u16X0402-HF	PEG C TXP13_JNC
(4) PEG_RXN13	C243	C0.22u16X0402-HF	PEG C TXN13_JNC
(4) PEG_TXP13	C560	C0.22u16X0402-HF	PEG C RXP13_JNC
(4) PEG_TXN13	C561	C0.22u16X0402-HF	PEG C RXN13_JNC
(4) PEG_RXP12	C228	C0.22u16X0402-HF	PEG C TXP12_JNC
(4) PEG_RXN12	C222	C0.22u16X0402-HF	PEG C TXN12_JNC
(4) PEG_TXP12	C549	C0.22u16X0402-HF	PEG C RXP12_JNC
(4) PEG_TXN12	C550	C0.22u16X0402-HF	PEG C RXN12_JNC
(4) PEG_RXP11	C221	C0.22u16X0402-HF	PEG C TXP11_JNC
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(4) PEG_TXN11	C548	C0.22u16X0402-HF	PEG C RXN11_JNC
(4) PEG_RXP10	C211	C0.22u16X0402-HF	PEG C TXP10_JNC
(4) PEG_RXN10	C219	C0.22u16X0402-HF	PEG C TXN10_JNC
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(4) PEG_TXN10	C542	C0.22u16X0402-HF	PEG C RXN10_JNC
(4) PEG_RXP9	C210	C0.22u16X0402-HF	PEG C TXP9_JNC
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(4) PEG_TXP7	C534	C0.22u16X0402-HF	PEG C RXP7_JNC
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(4) PEG_RXN2	C114	C0.22u16X0402-HF	PEG C TXN2_JNC
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(4) PEG_TXP0	C515	C0.22u16X0402-HF	PEG C RXP0_JNC
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N16P-GX (Frame Buffer Interface)

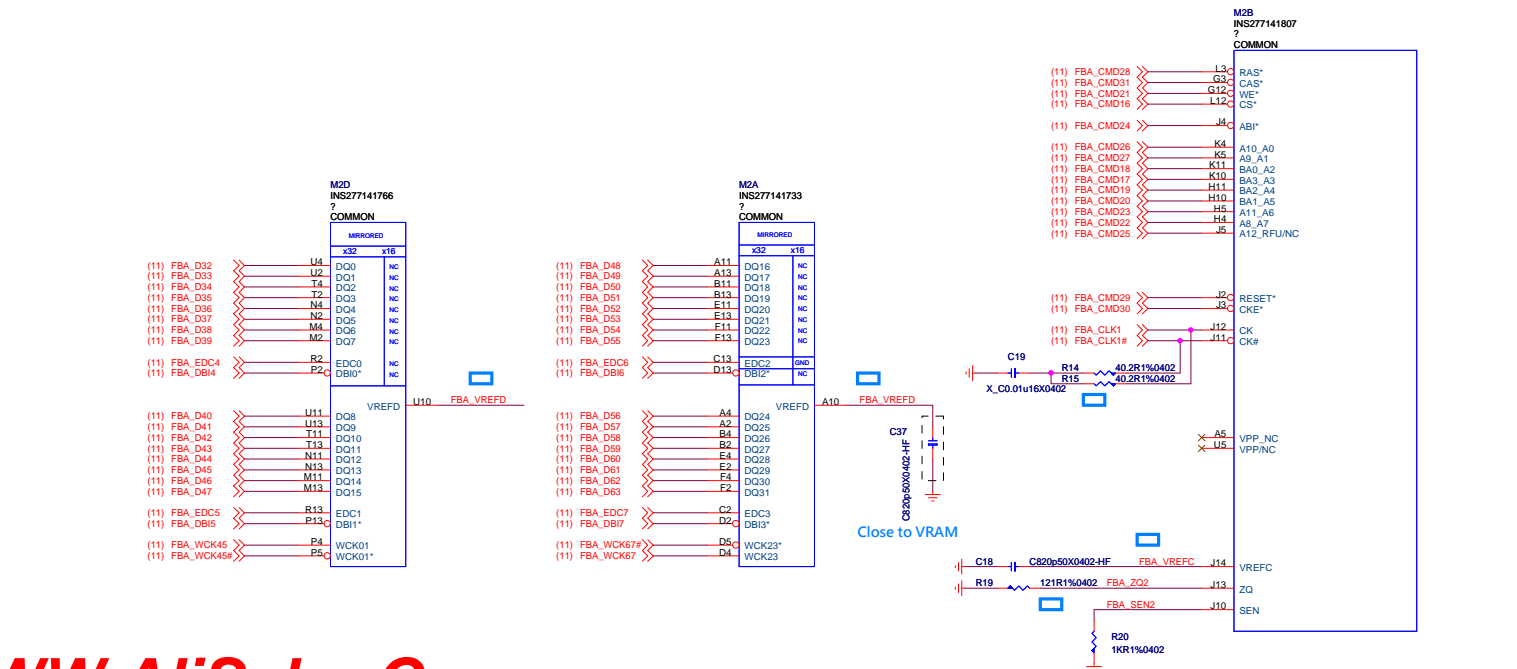
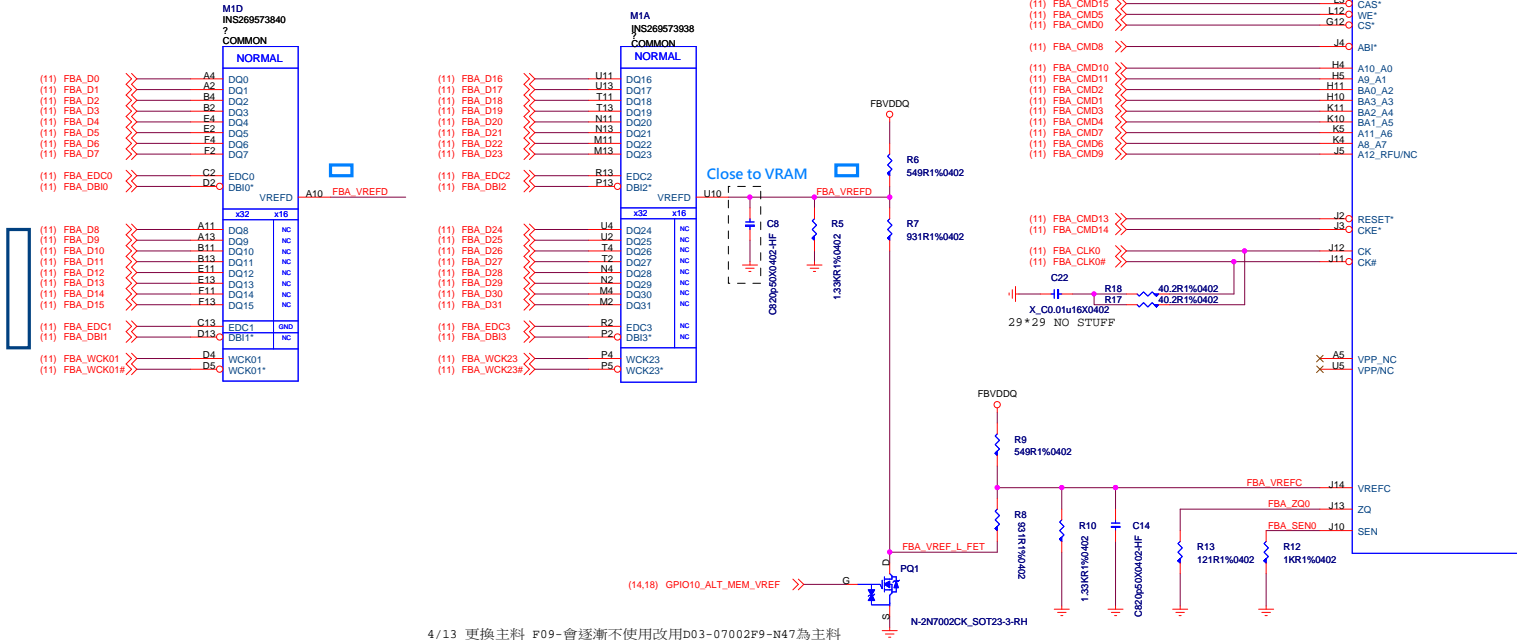
GC6M is GC6 2.0 that it is for N15x or later GPU
So we use CRB GC6M design



GDDR5 CMD Mapping Mode H Table

12	28	BASE
5	21	WE'
0	16	CS'
8	24	AB'
10	26	AO_A10
11	27	AI_A9
18	34	BA0
3	19	AA0A2
4	20	AA_BA1
7	23	AA_A11
6	22	AT_A8
14	30	CKP'
13	29	RESET'

N16P-GX (GDDR5 Frame A-1)



msi MICRO-STAR INT'L CO.,LTD.

Part Number: **N16P-GX GDDR5 Frame A-1**

Size: Custom

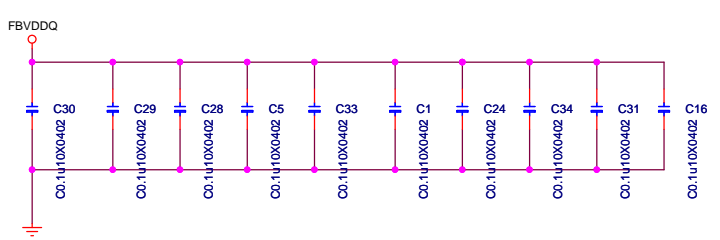
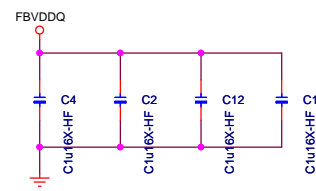
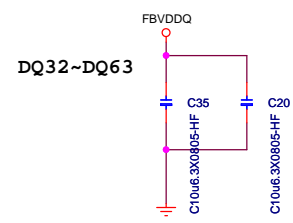
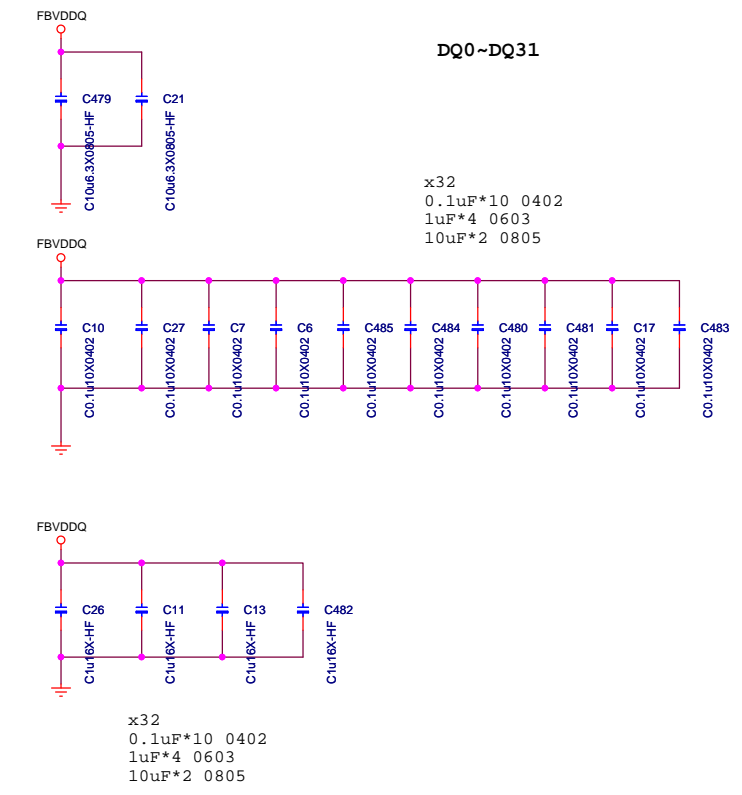
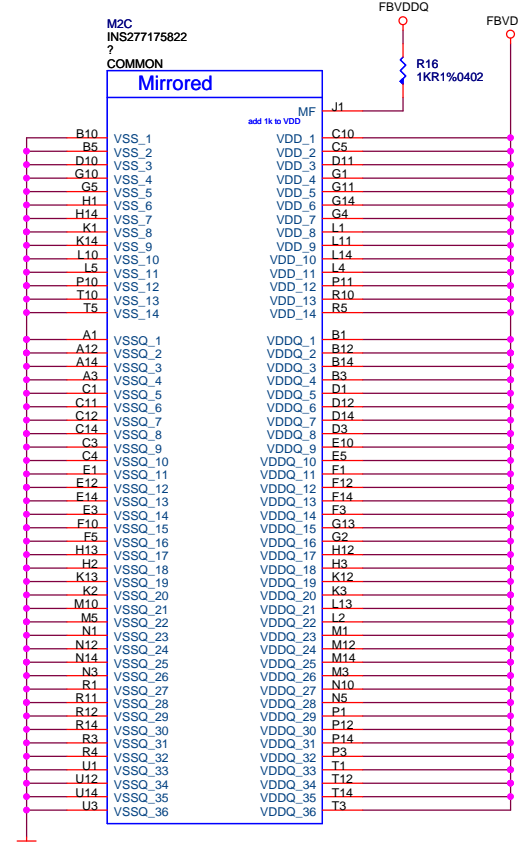
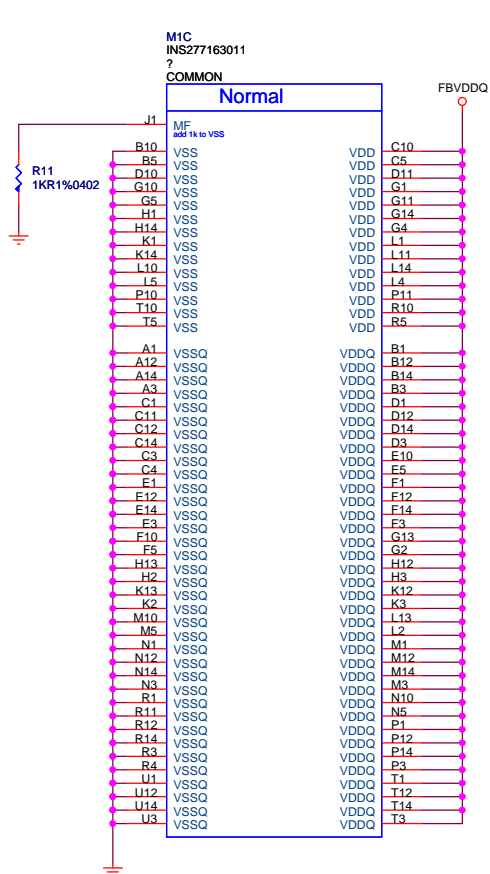
Document Number: **MS-16J5**

Date: Tuesday, April 21, 2015

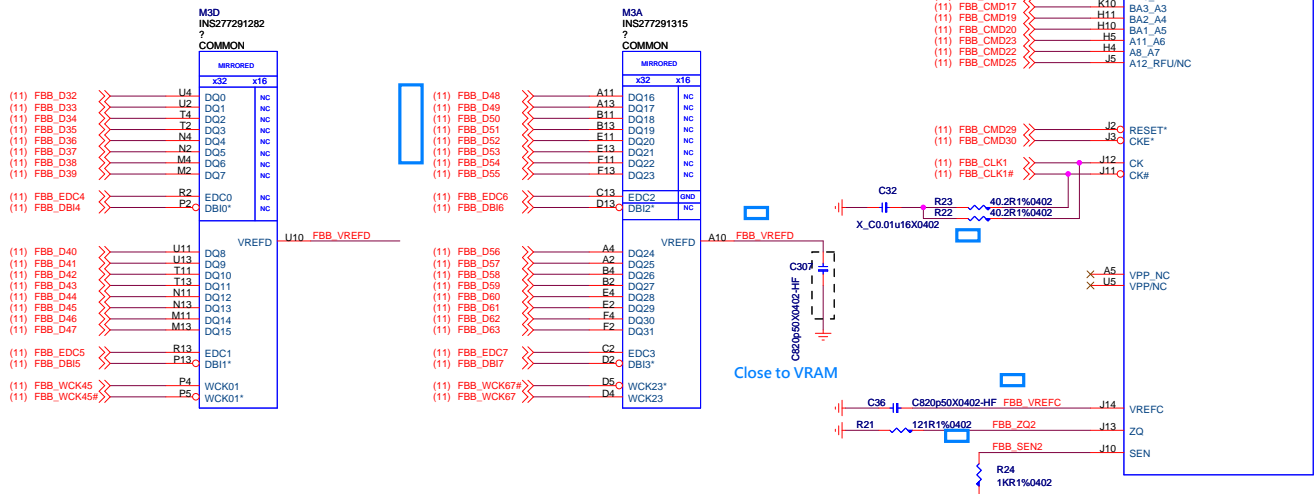
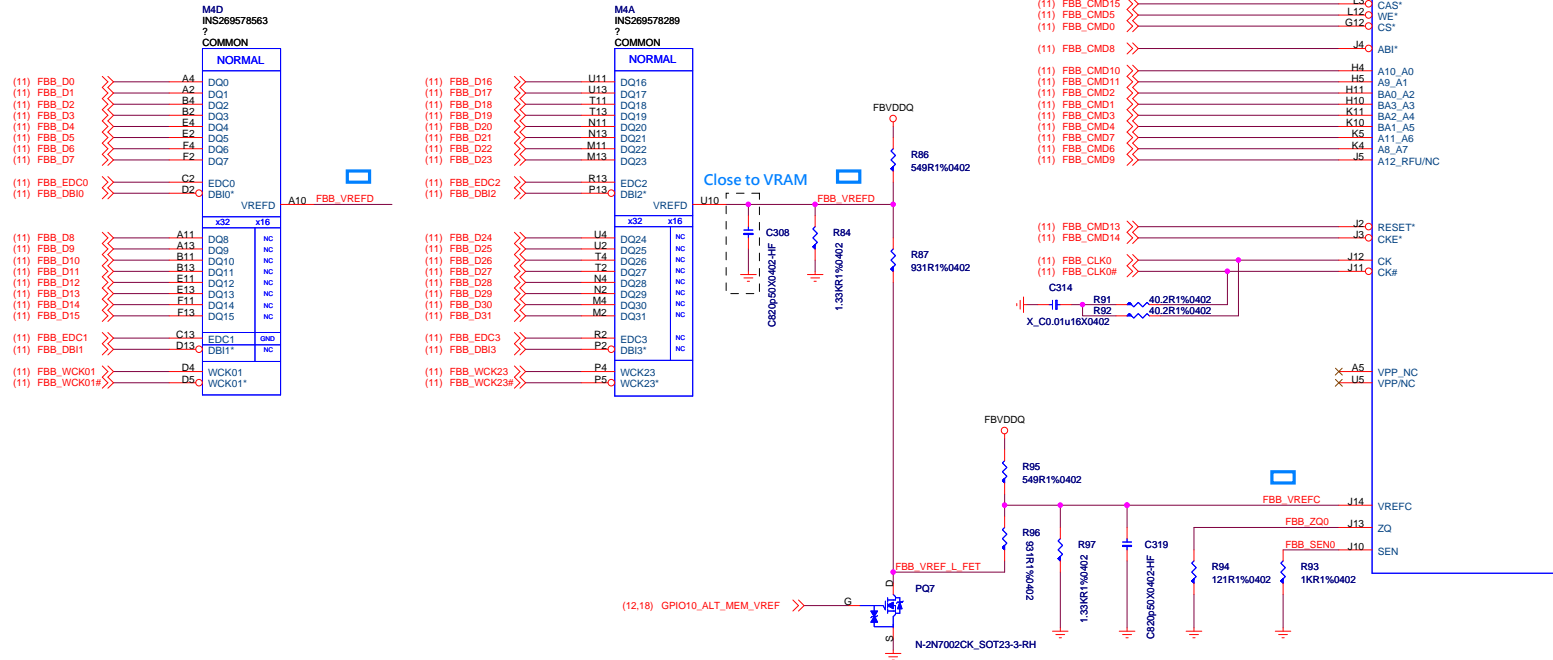
Sheet 12 of 55

Rev: **0A**

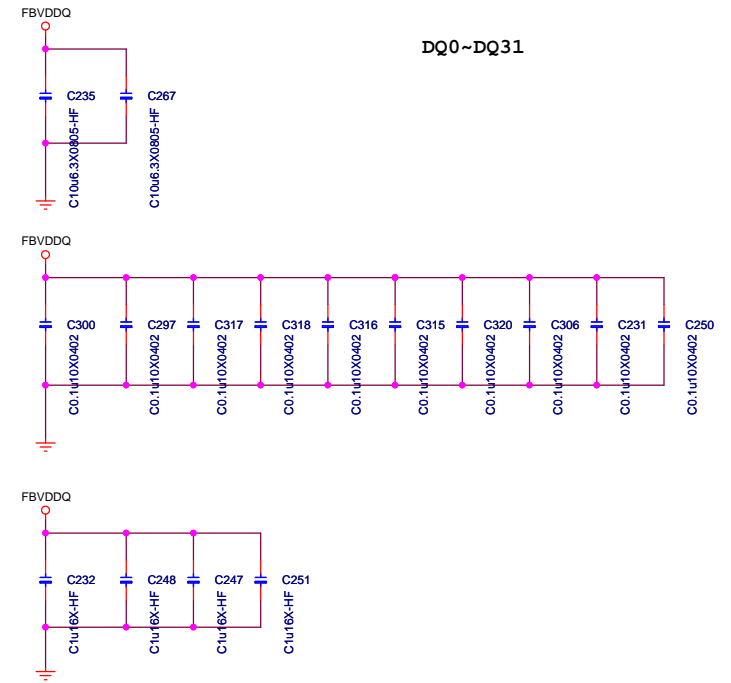
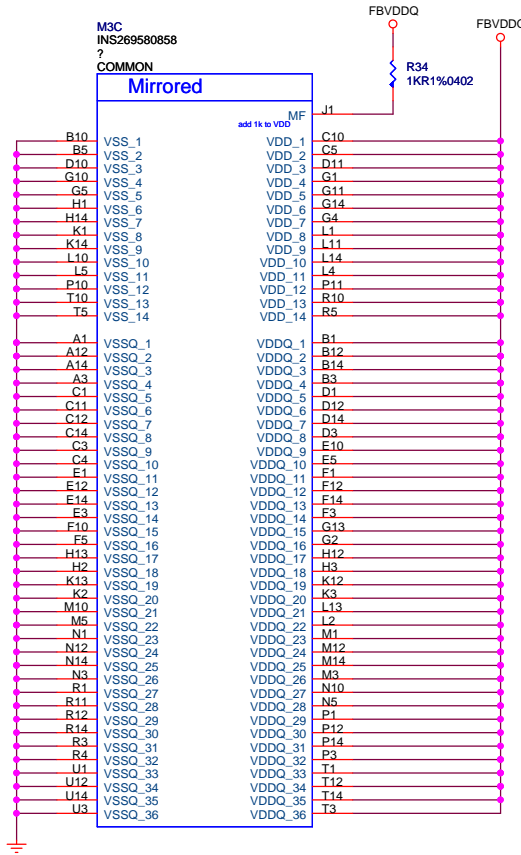
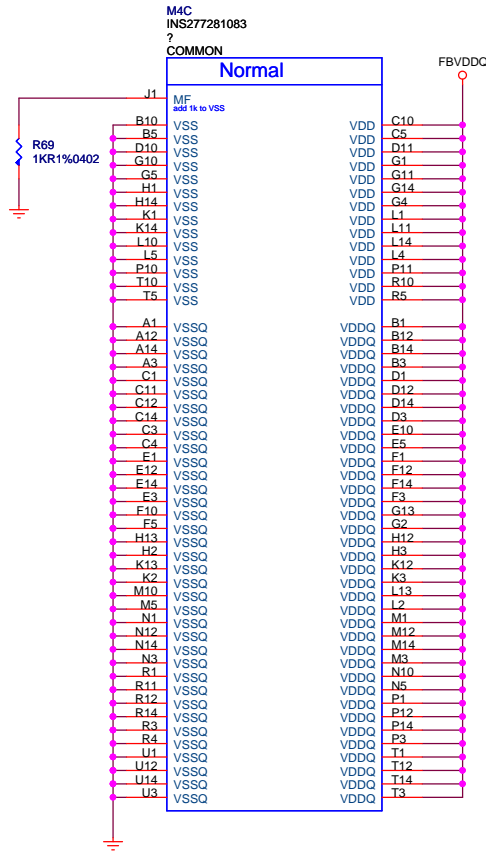
N16P-GX(GDDR5 Frame A-2)



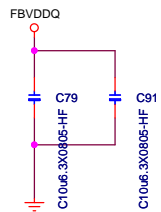
N16P-GX (GDDR5 Frame B-1)



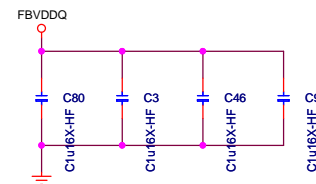
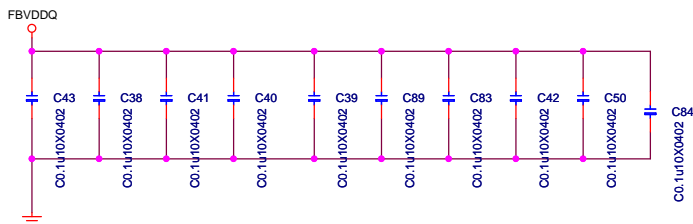
N16P-GX(GDDR5 Frame B-2)



DQ0~DQ31

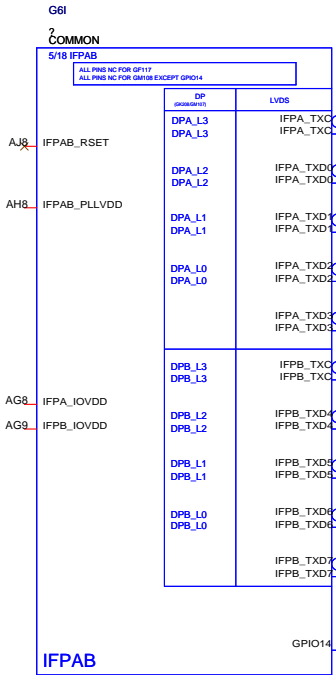


DQ32~DQ63

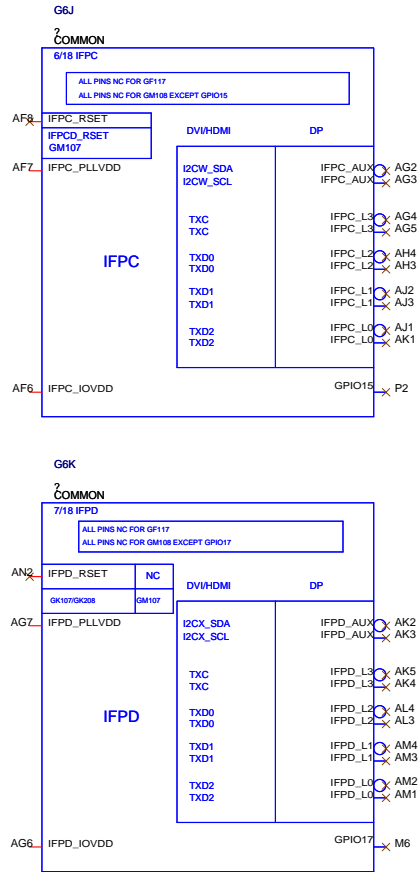


N16P-GX(Display IF)

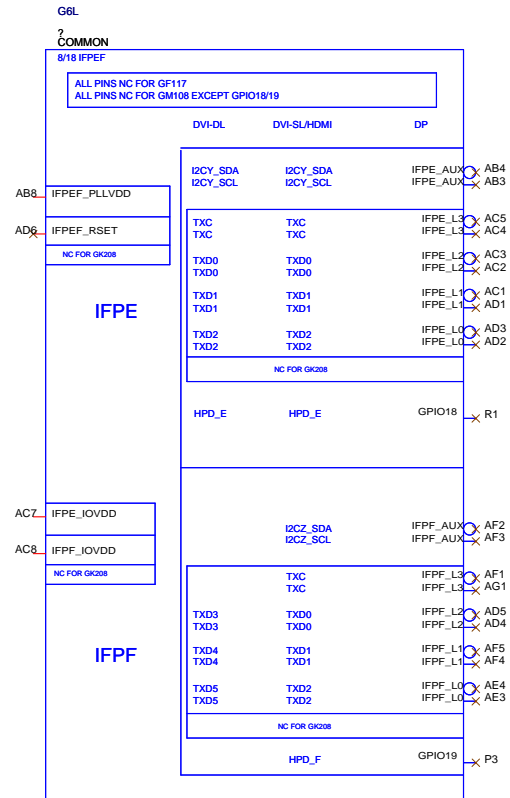
IFP A/B LVDSDual Link



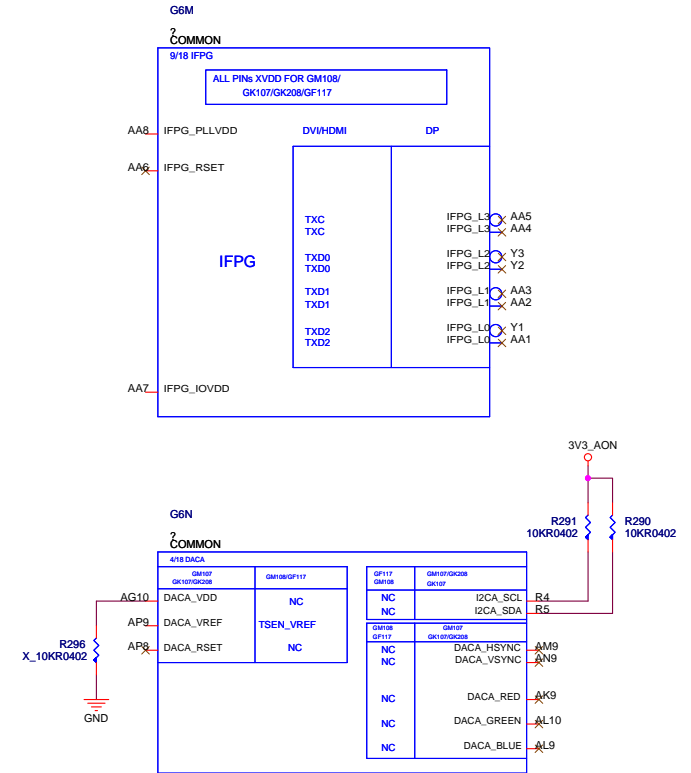
IFP C Native HDMI OR DP



IFP E/F Dual Link TMDS DVI-I

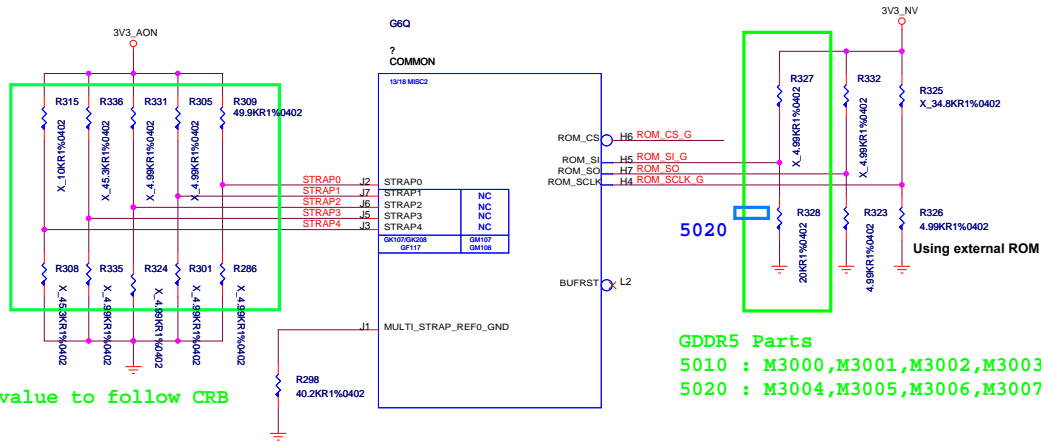


DAC A VGA

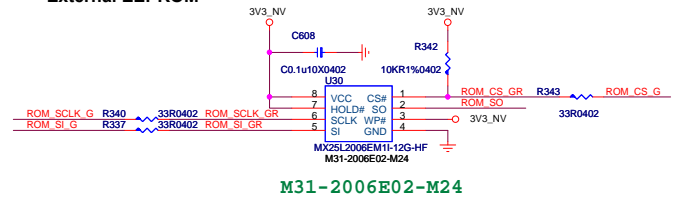


msi MICRO-STAR INT'L CO.,LTD.	
Title: N16P-GX Display IF	
Size: Custom	Document Number: MS-16J5
Date: Tuesday, April 21, 2015	Rev: 0A
Sheet: 16	of 55

ROM, MULTI-LEVEL STRAPS



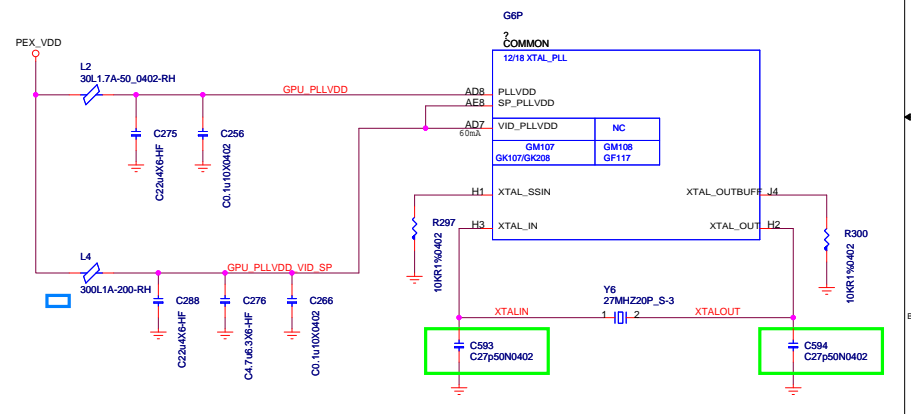
External EEPROM



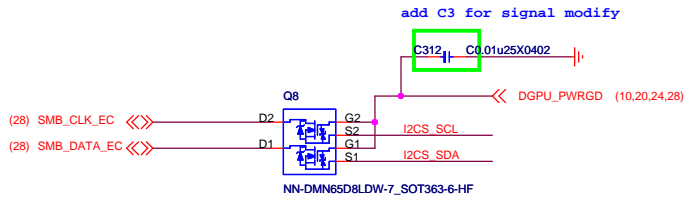
DEFAULT SETTING

ROM_S2	Samsung	V_BOT5	5020
128Mx32bit		M12-4132525-S02	
R11-0203T12-W08		X_K4G41325FC-HC03	
X_20KR1%0402			
ROM_H2	Hynix	V_BOT4	5020
128Mx32bit		M12-5GC4H05-H23	
R11-0153T12-W08		X_H5GC4H24MFR-T2C	
X_15KR1%0402			
ROM_M2	Micron	V_BOT6	5020
128Mx32bit		M12-4032B05-E59	
R11-2492T12-W08		X_EDW4032BABG-60-F-HF	
X_24.9KR1%0402			
ROM_H3	Hynix	V_BOT7	5020
128Mx32bit		M12-5GC4H65-H23	
R11-3482T12-W08		X_H5GC4H24AJR-T2C	
X_34.8KR1%0402			

ROM_SI	RAM_CFG[3:0]	
ROM_SO	DEVID_SEL PCIE_CFG SMB_ALT_ADDR VGADEVICE	5K PD
ROM_SCLK	SOR_EXposed[3:0]	5K PD
STRAP0		50K PU 3V3_AON
STRAP1		Reserved
STRAP2		Reserved
STRAP3		Reserved
STRAP4		Reserved

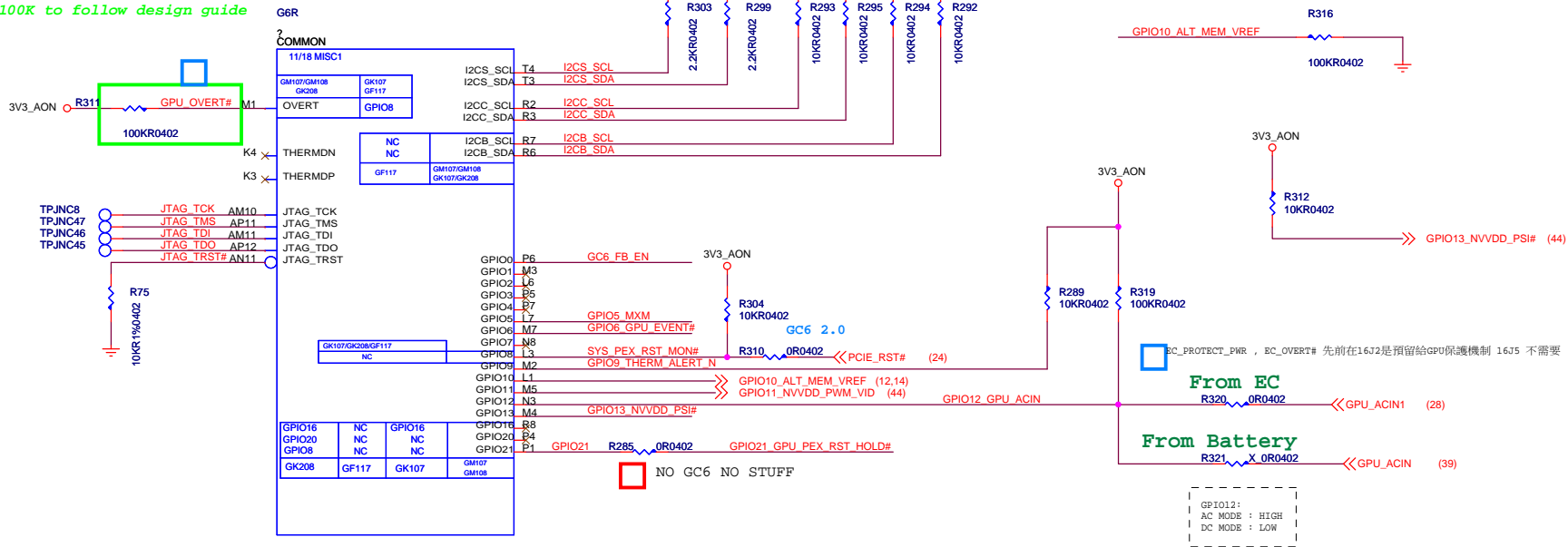


GND		3V3
5K	0000	1000
10K	0001	1010
15K	0010	1011
20K	0011	1101
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111
	PD	PU



CRB有兩種接法
 一種接3V3_NV
 一種接3V3_AON

change 100K to follow design guide

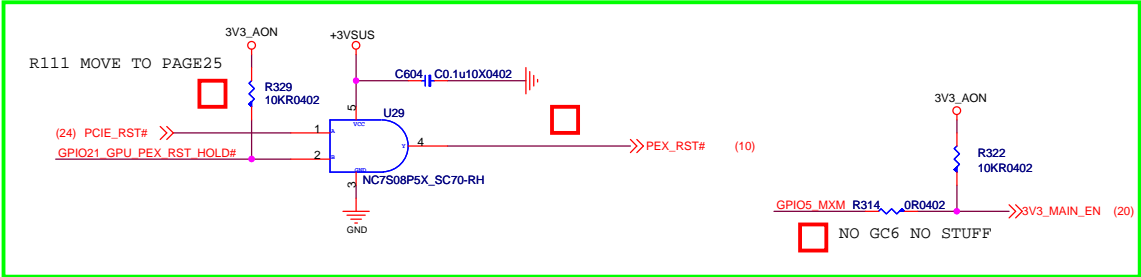
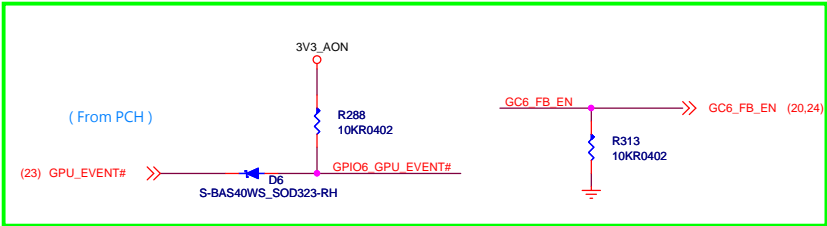


EC_PROTECT_PWR, EC_OVERT# 先前在16J2是預留給GPU保護機制 16J5 不需要

From EC
 R320 0R0402 << GPU_ACIN1 (28)

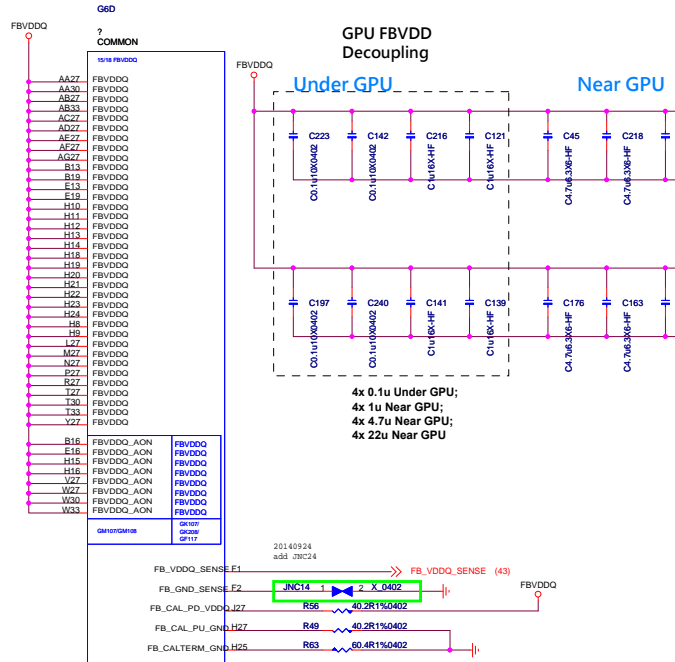
From Battery
 R321 X 0R0402 << GPU_ACIN (39)

GPIO12:
 AC MODE : HIGH
 DC MODE : LOW

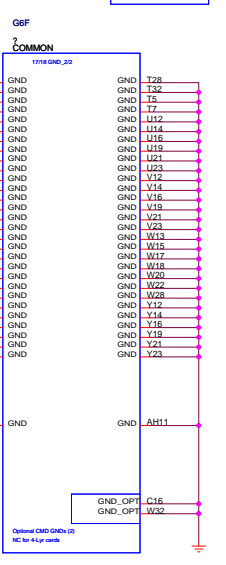
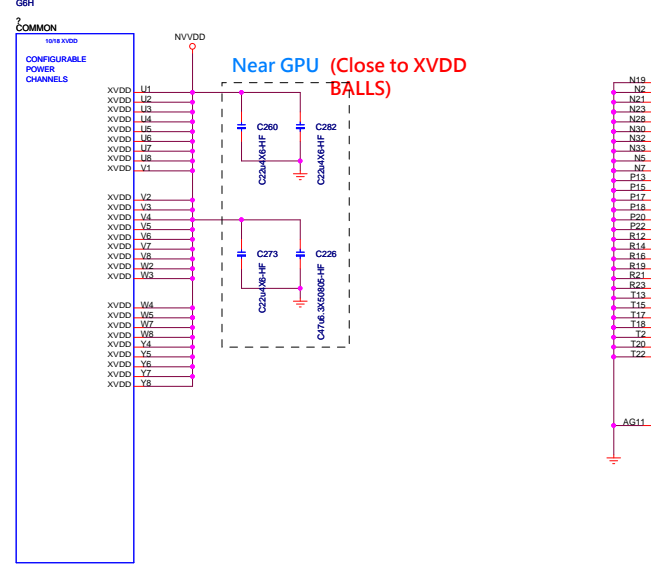
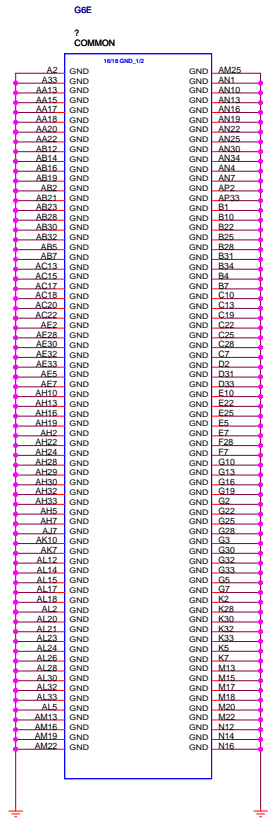
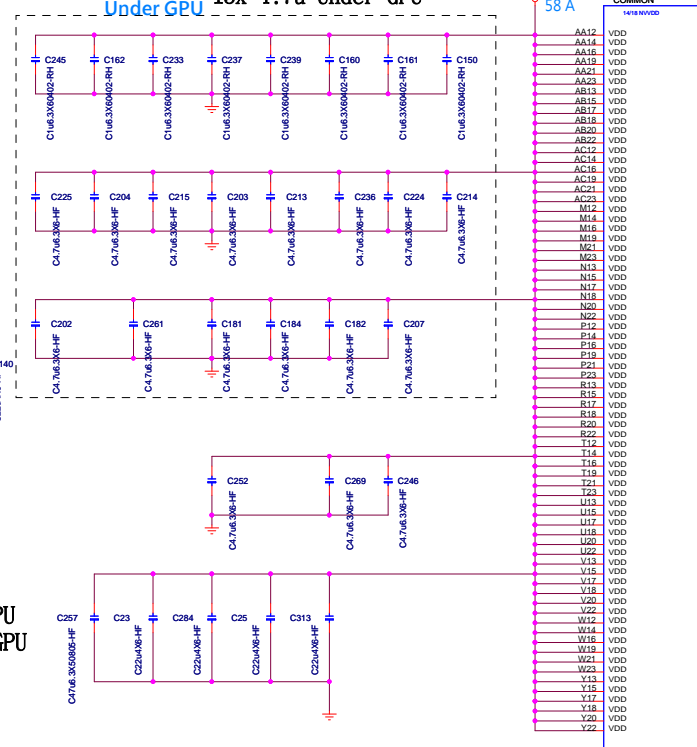


N16P-GX (Power & GND)

8x 1u Under GPU;
15x 4.7u Under GPU



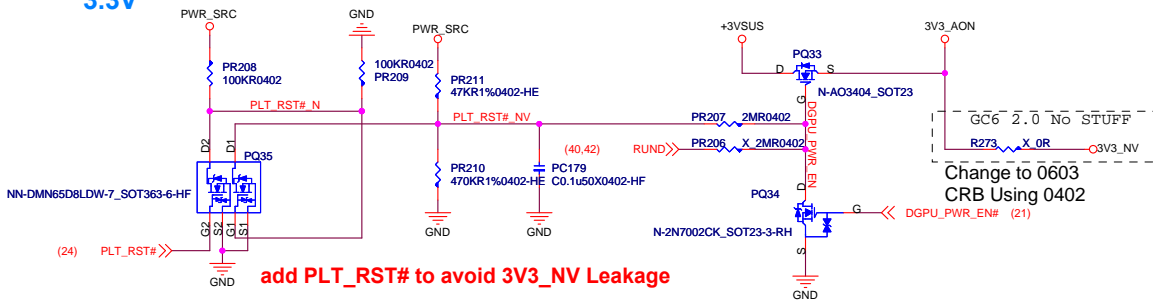
7x 22u near GPU
5x 4.7u near GPU



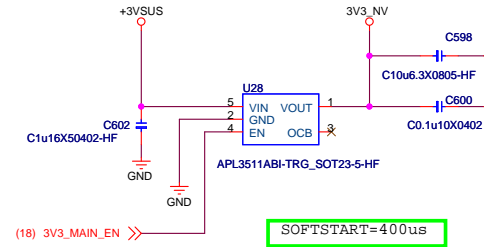
N16P-GX(Power Control)

nVIDIA Power Sequence Control 3V3_AON -> 3V3_NV -> NVVDD -> PEX_VDD -> FBVDDQ -> DGPUPWRGD

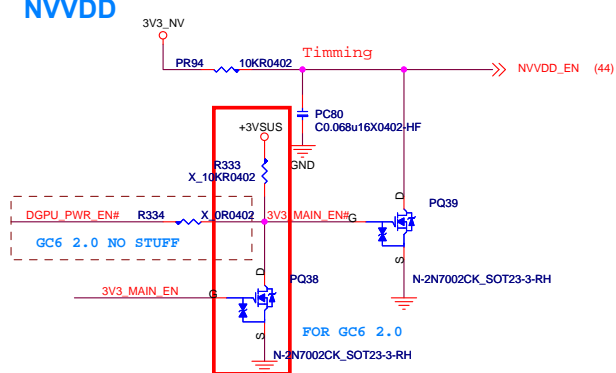
3.3V



GC6 2.0 STUFF



NVVDD



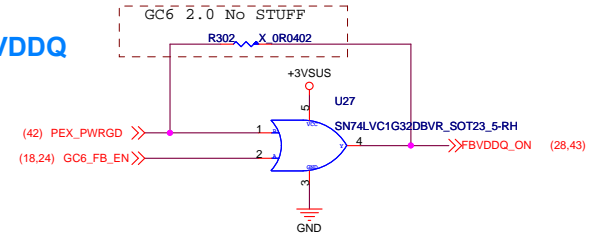
PEX_VDD



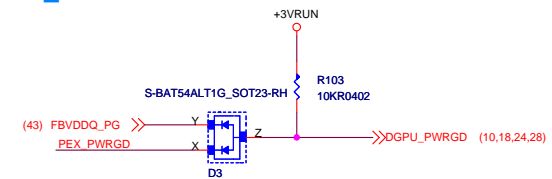
EDP Design Guide:
N16P-GX
NVVDD : 51.1A ; Peak 87A
3.3VRUN : 0.34A
PEX_VDD : 2.57A
FBVDDQ : 8.75A

EDP Design Guide:
N16P-GT
NVVDD : 30.2A ; Peak 53A
3.3VRUN : 0.34A
PEX_VDD : 2.57A
FBVDDQ : 8.75A

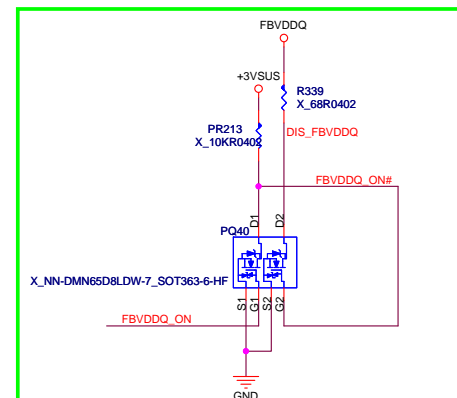
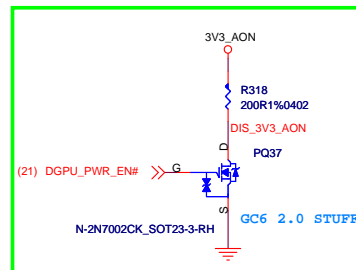
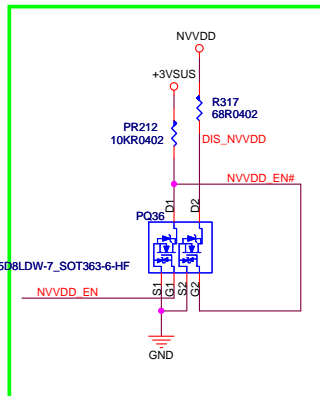
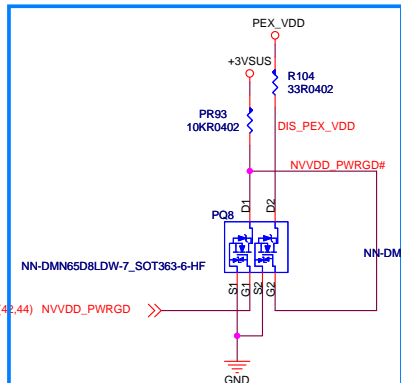
FBVDDQ



DGPU_PWRGD



Discharge Circuit



Width: 4 mils
Spacing: 15/20 mils
Length: 1000 mils

+1.0VSUS

R156 2.7KR1%0402-HE XCLK_RBIAIS

RTCX1_JNC BC3
RTCX2_JNC BD10

(10) GPU_CLKREQ#>> CLKREQ1# AW24
CLKREQ2# AT24

(35) GLAN_CLKREQ#>> BD25
(38) WLAN_CLKREQ#>> BB24
(29) PCIECLK_USB_REQ#>> BE28

(37) SSD_CLKREQ#>> CLKREQ6# AT33
CLKREQ8# AR31
CLKREQ9# BD32
CLKREQ10# BC32
CLKREQ11# BB31
CLKREQ12# BA33
CLKREQ13# AW33
CLKREQ14# BB33
CLKREQ15# BD33

R13 CLKOUT_PCIE_N15
R14 CLKOUT_PCIE_P15

P4 CLKOUT_PCIE_N14
P2 CLKOUT_PCIE_P14

W2 CLKOUT_PCIE_N13
Y9 CLKOUT_PCIE_P13

U2 CLKOUT_PCIE_N12
U3 CLKOUT_PCIE_P12

R13 CLKOUT_PCIE_N15
R14 CLKOUT_PCIE_P15

P4 CLKOUT_PCIE_N14
P2 CLKOUT_PCIE_P14

W2 CLKOUT_PCIE_N13
Y9 CLKOUT_PCIE_P13

U2 CLKOUT_PCIE_N12
U3 CLKOUT_PCIE_P12

R13 CLKOUT_PCIE_N15
R14 CLKOUT_PCIE_P15

P4 CLKOUT_PCIE_N14
P2 CLKOUT_PCIE_P14

W2 CLKOUT_PCIE_N13
Y9 CLKOUT_PCIE_P13

U2 CLKOUT_PCIE_N12
U3 CLKOUT_PCIE_P12

R13 CLKOUT_PCIE_N15
R14 CLKOUT_PCIE_P15

P4 CLKOUT_PCIE_N14
P2 CLKOUT_PCIE_P14

W2 CLKOUT_PCIE_N13
Y9 CLKOUT_PCIE_P13

U2 CLKOUT_PCIE_N12
U3 CLKOUT_PCIE_P12

R13 CLKOUT_PCIE_N15
R14 CLKOUT_PCIE_P15

P4 CLKOUT_PCIE_N14
P2 CLKOUT_PCIE_P14

W2 CLKOUT_PCIE_N13
Y9 CLKOUT_PCIE_P13

U2 CLKOUT_PCIE_N12
U3 CLKOUT_PCIE_P12

R13 CLKOUT_PCIE_N15
R14 CLKOUT_PCIE_P15

P4 CLKOUT_PCIE_N14
P2 CLKOUT_PCIE_P14

W2 CLKOUT_PCIE_N13
Y9 CLKOUT_PCIE_P13

U2 CLKOUT_PCIE_N12
U3 CLKOUT_PCIE_P12

R13 CLKOUT_PCIE_N15
R14 CLKOUT_PCIE_P15

P4 CLKOUT_PCIE_N14
P2 CLKOUT_PCIE_P14

W2 CLKOUT_PCIE_N13
Y9 CLKOUT_PCIE_P13

U2 CLKOUT_PCIE_N12
U3 CLKOUT_PCIE_P12

R13 CLKOUT_PCIE_N15
R14 CLKOUT_PCIE_P15

P4 CLKOUT_PCIE_N14
P2 CLKOUT_PCIE_P14

W2 CLKOUT_PCIE_N13
Y9 CLKOUT_PCIE_P13

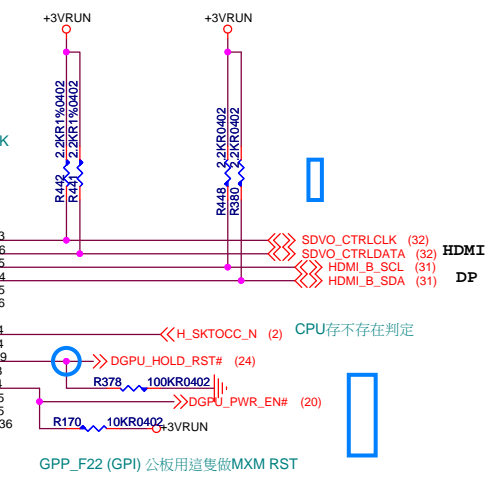
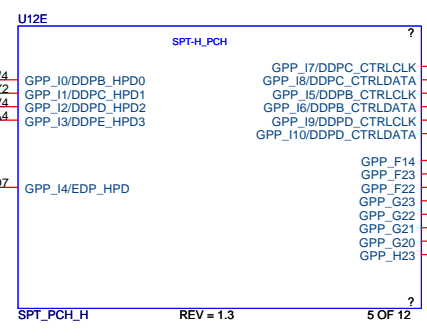
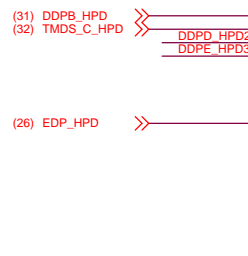
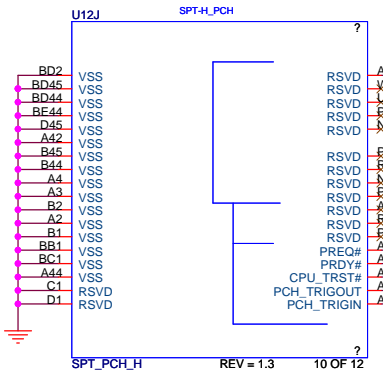
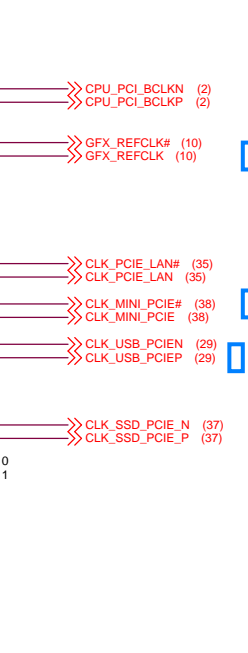
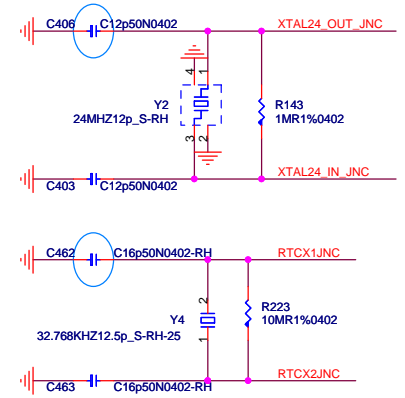
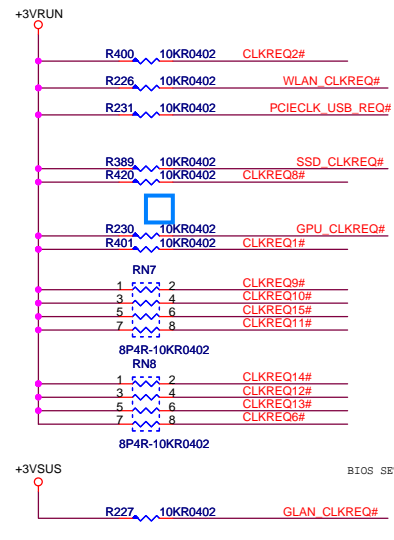
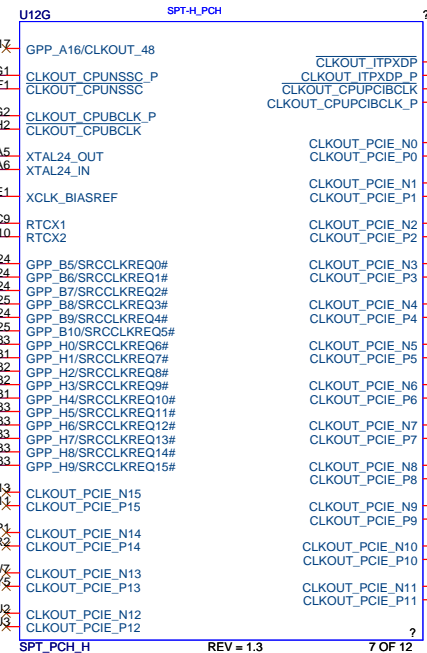
U2 CLKOUT_PCIE_N12
U3 CLKOUT_PCIE_P12

R13 CLKOUT_PCIE_N15
R14 CLKOUT_PCIE_P15

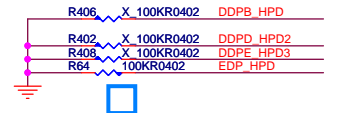
P4 CLKOUT_PCIE_N14
P2 CLKOUT_PCIE_P14

W2 CLKOUT_PCIE_N13
Y9 CLKOUT_PCIE_P13

U2 CLKOUT_PCIE_N12
U3 CLKOUT_PCIE_P12



内部都沒PD所以要外面做

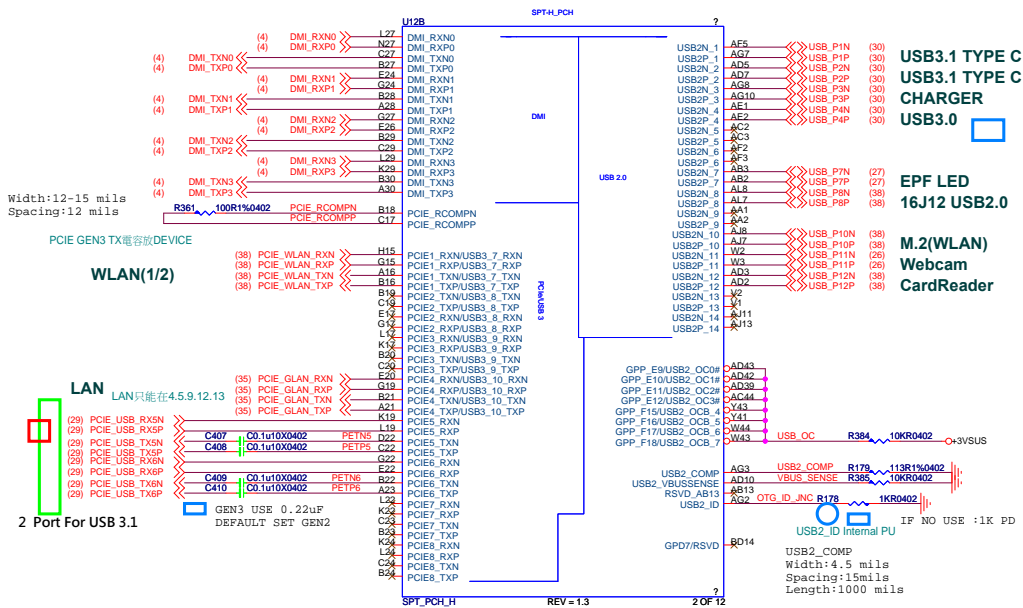


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Title: **PCH 1(CLK/DDI)**

Size A3 Document Number **MS-16J5** Rev **0A**

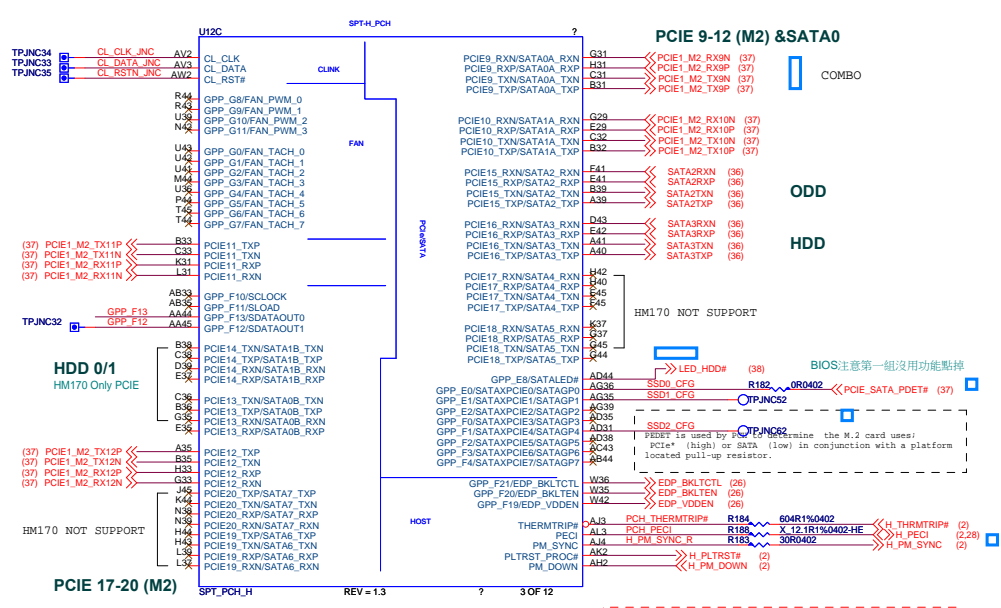
Date: Tuesday, April 21, 2015 Sheet 21 of 55



Width:12-15 mils
Spacing:12 mils

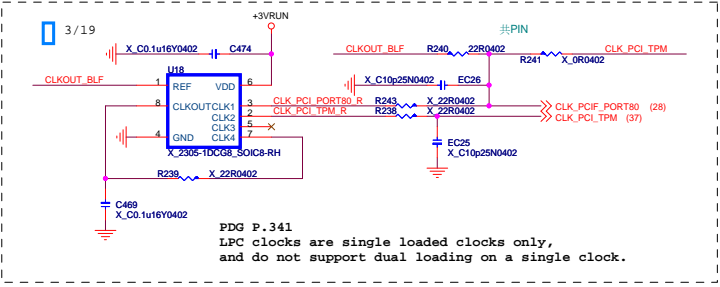
LAN 只能在4.5.9.12.13

2 Port For USB 3.1



BIOS注意第一組沒有功能點
H1M170 NOT SUPPORT
H1M170 NOT SUPPORT
CRB GFX Select (GPP_F13)
0 - Internal GFX
1 - MXM GFX

SKU	High Speed SATA I/O Ports							
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5	SATA-6	SATA-7
HM170	GEN3	GEN3	GEN3	GEN3	x	x	x	x
C236	GEN3	GEN3	GEN3	GEN3	GEN3	GEN3	GEN3	GEN3

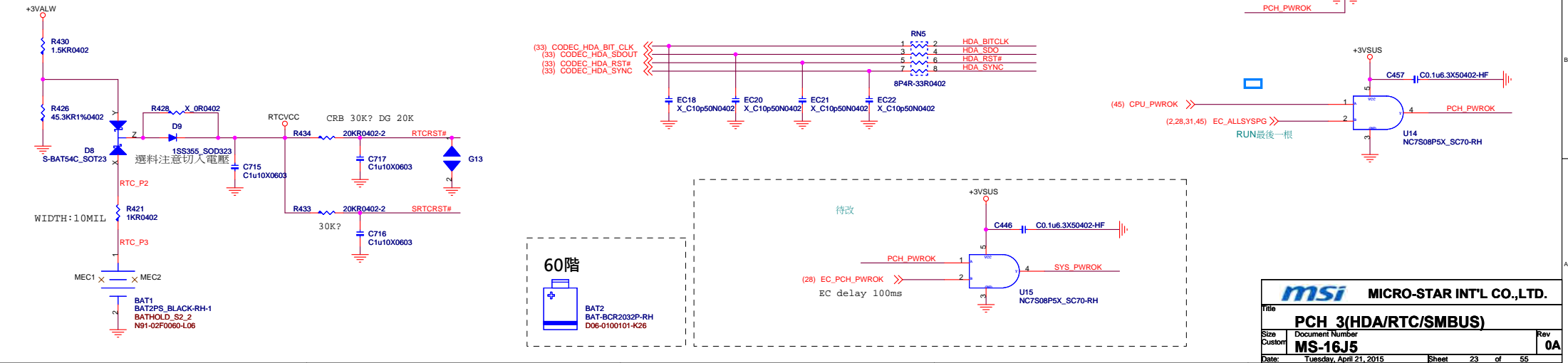
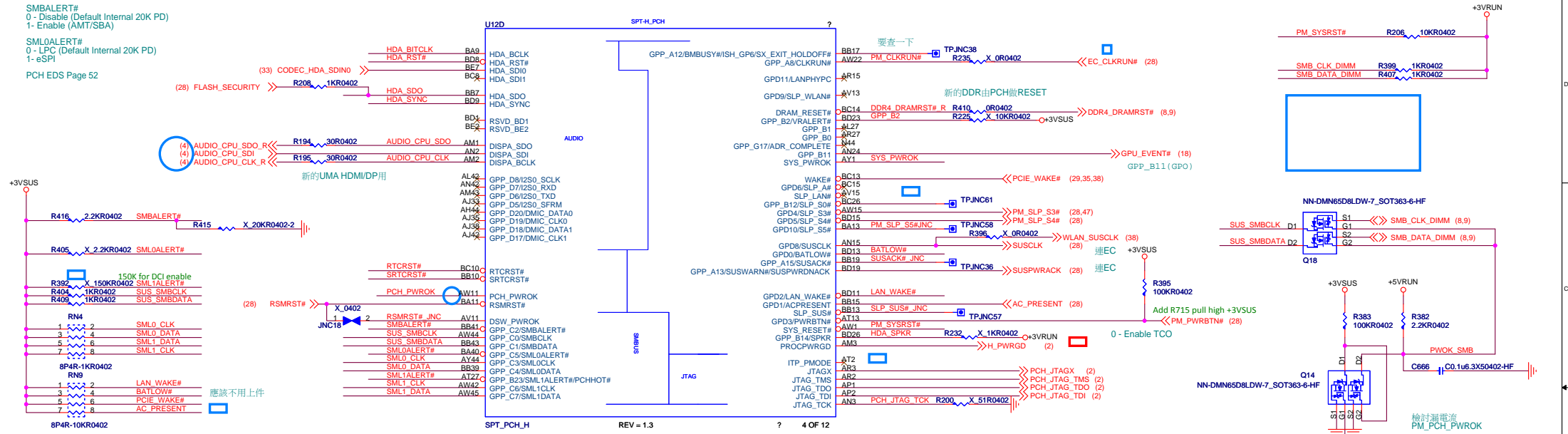


PDG P.341
LPC clocks are single loaded clocks only,
and do not support dual loading on a single clock.

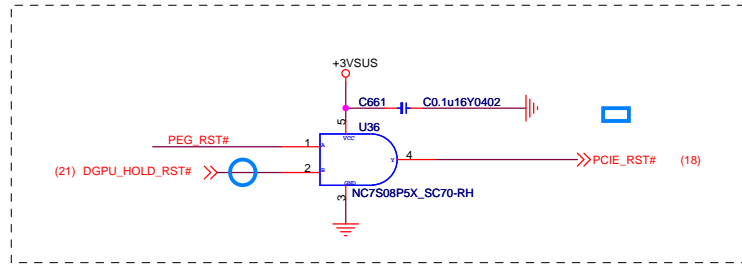
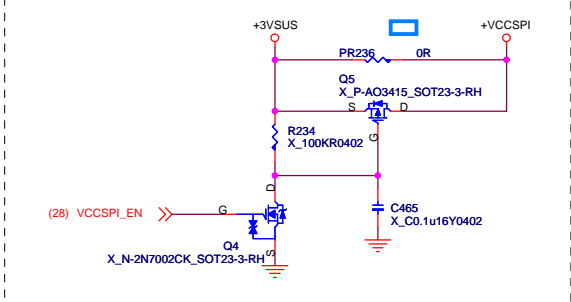
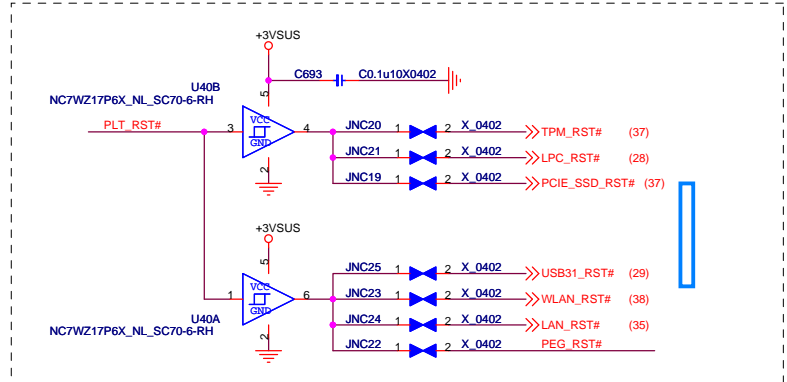
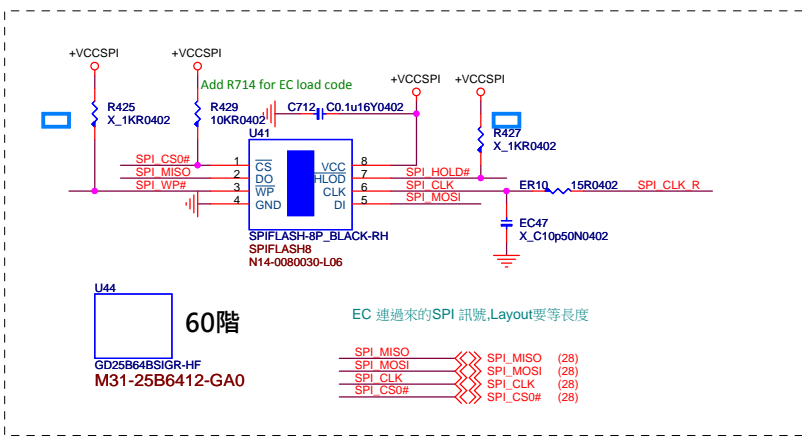
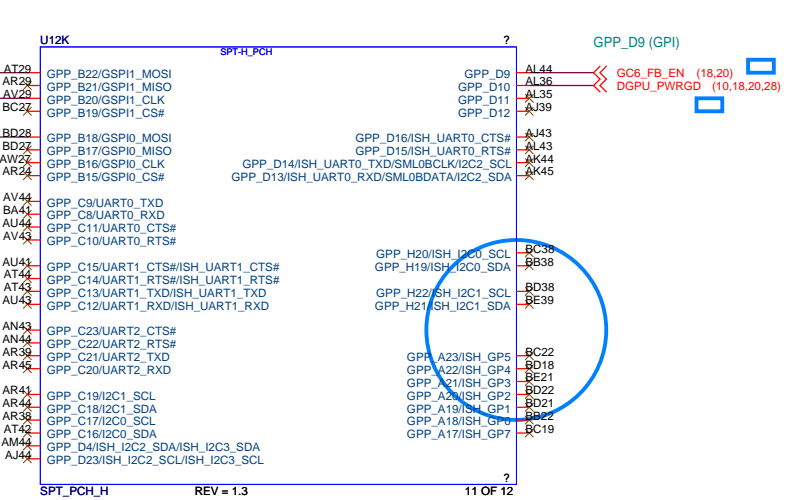
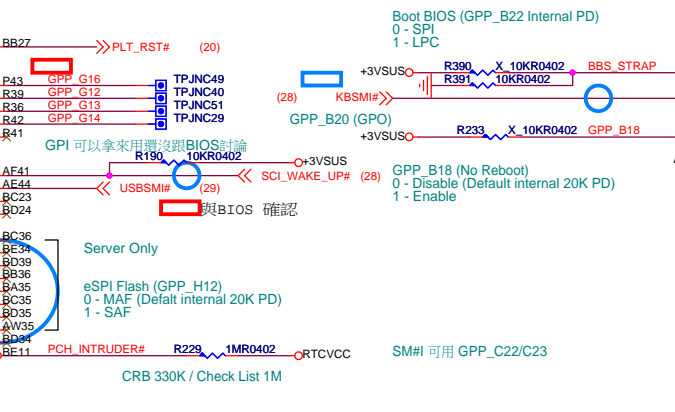
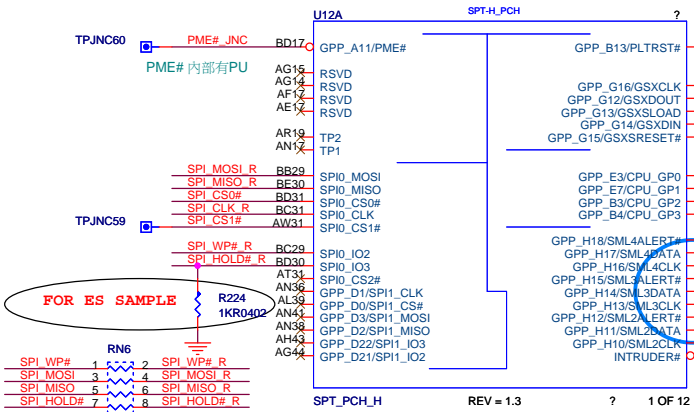
SMBALERT#
 0 - Disable (Default Internal 20K PD)
 1 - Enable (AMT/SBA)

SML0ALERT#
 0 - LPC (Default Internal 20K PD)
 1 - eSPI

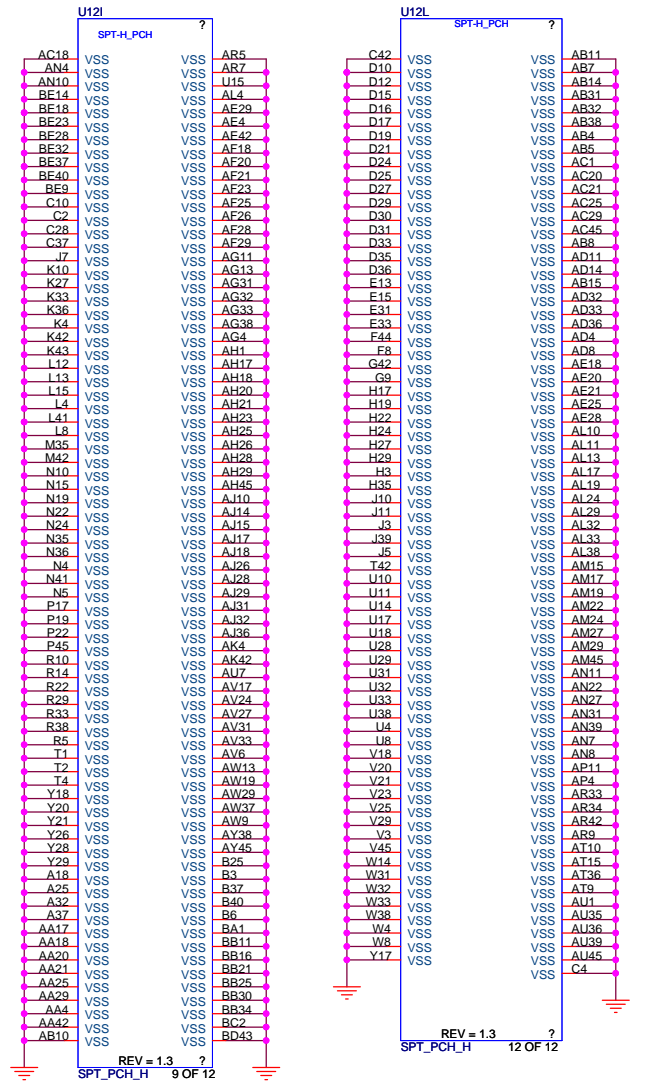
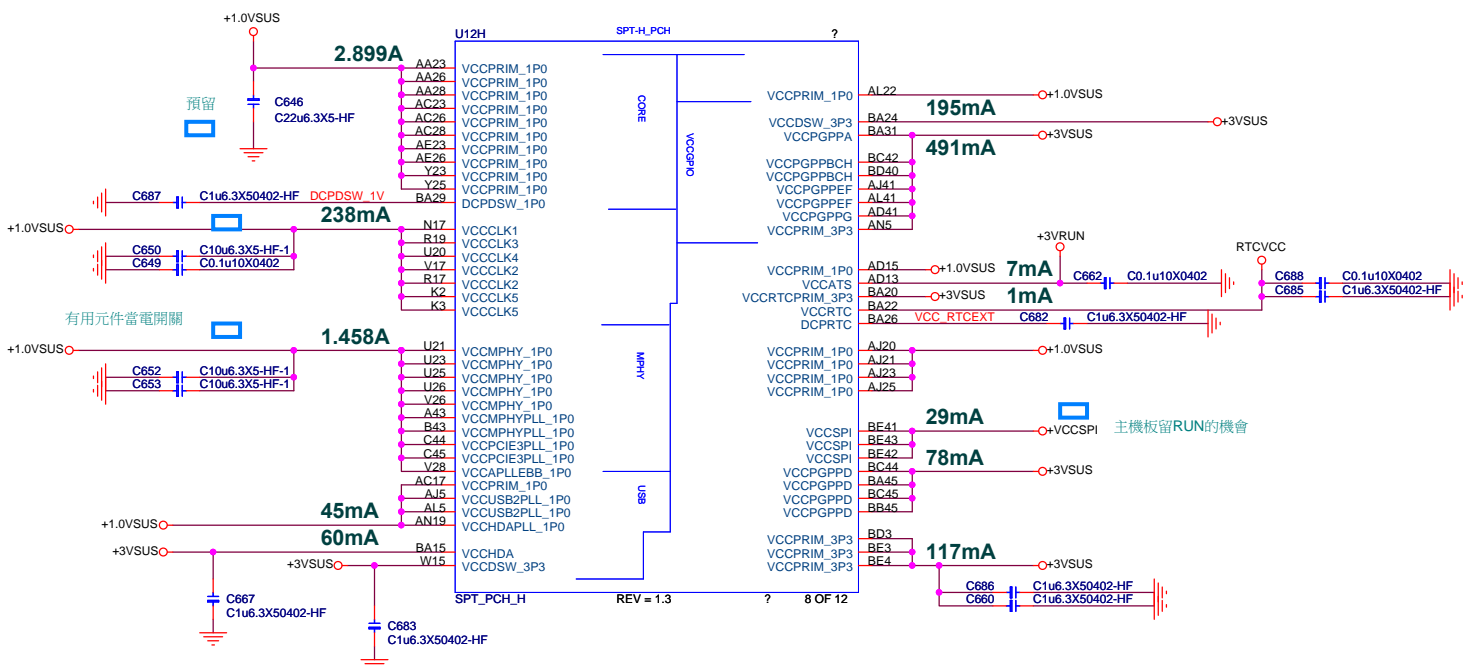
PCH EDS Page 52



msi MICRO-STAR INT'L CO.,LTD.		
Title PCH 3(HDA/RTC/SMBUS)		
Size	Document Number	Rev
Customer	MS-16J5	0A
Date:	Tuesday, April 21, 2015	Sheet 23 of 55



msi MICRO-STAR INT'L CO.,LTD.		
Title: PCH 4(SPI/GPIO)		
Size: Custom	Document Number: MS-16J5	Rev: 0A
Date: Tuesday, April 21, 2015	Sheet: 24	of 55



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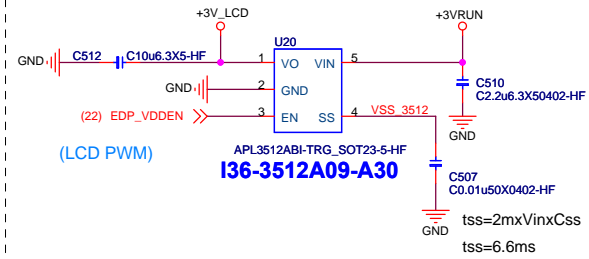
File: **PCH 5(Power1)**

Size: Custom Document Number: **MS-16J5** Rev: **0A**

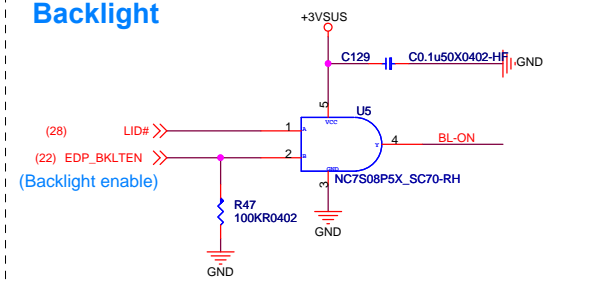
Date: Tuesday, April 21, 2015 Sheet 25 of 55

eDP

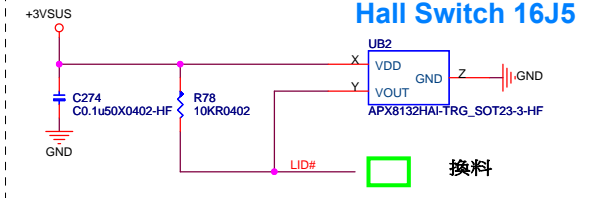
Panel Device Logic Power



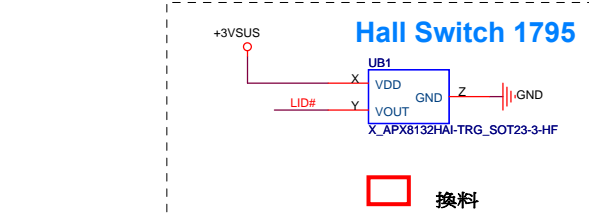
Backlight



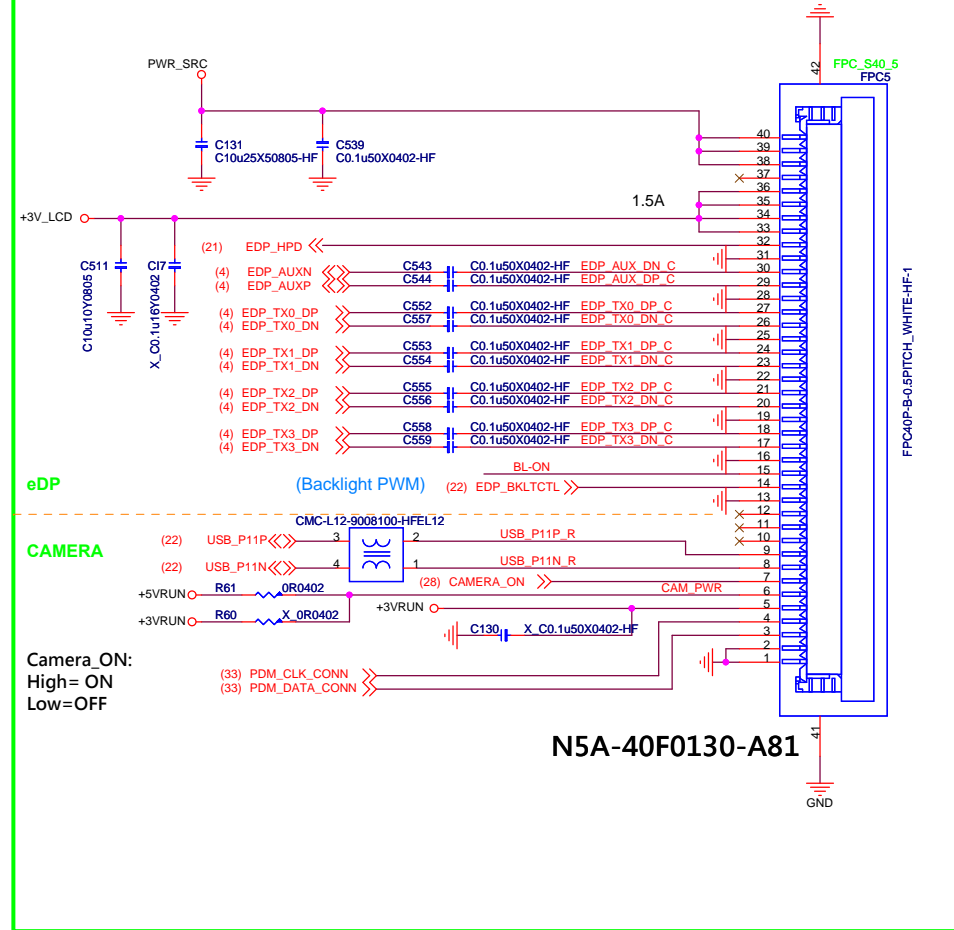
Hall Switch 16J5



Hall Switch 1795

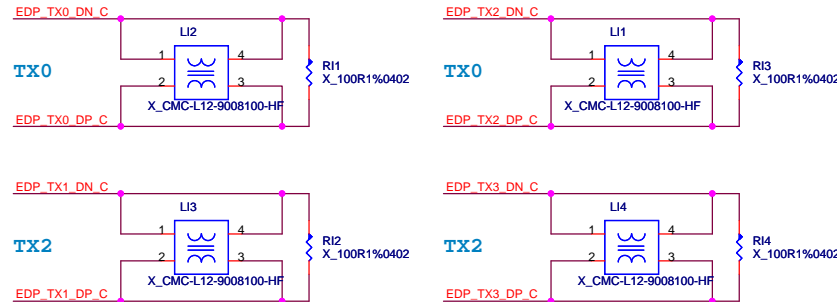


eDP CONN CAMERA



LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon



Place Close eDP Connector

Reserve for EMI

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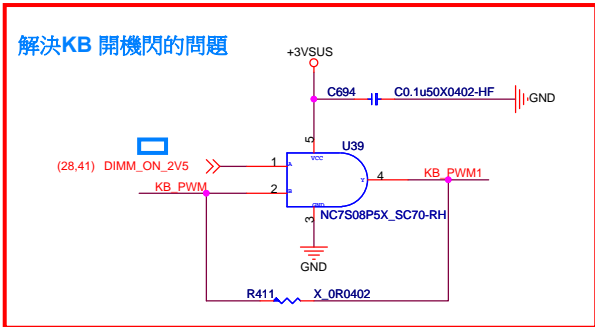
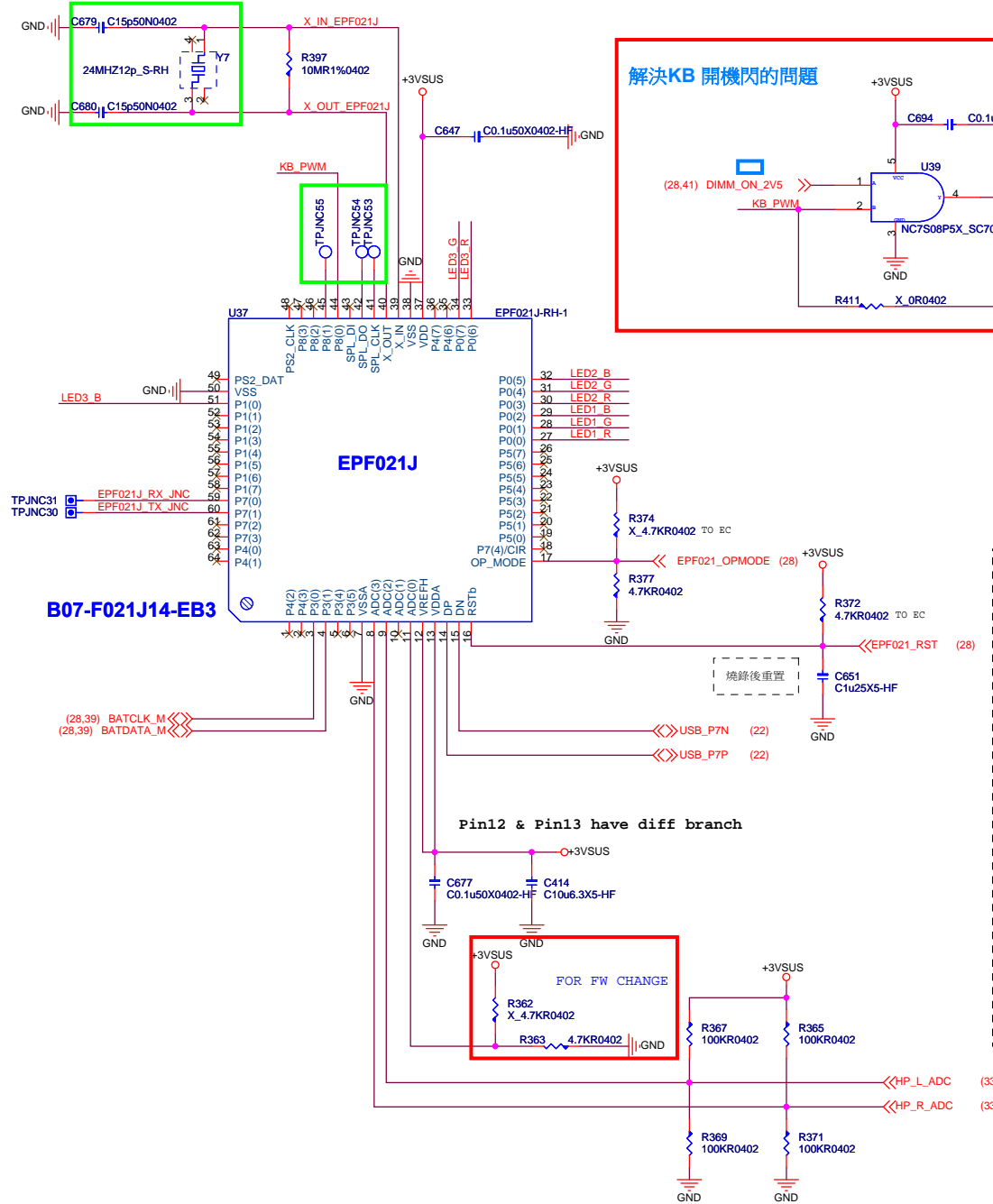
Title: **eDP /Camera**

Size: Document Number **MS-16J5** Rev **0A**

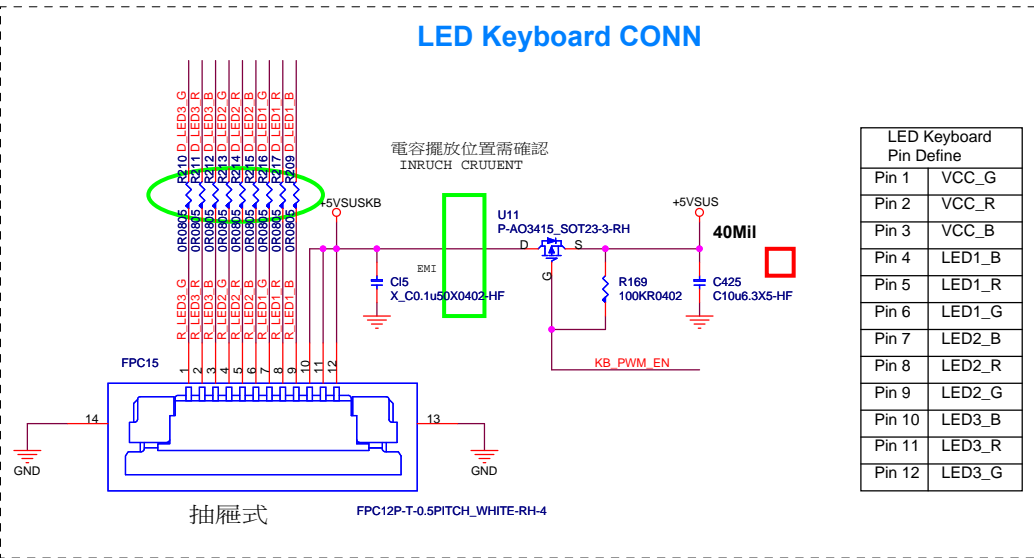
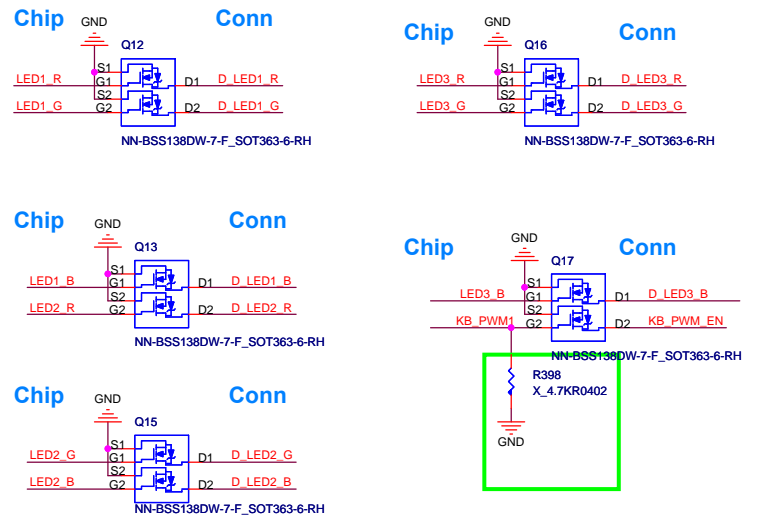
Date: Tuesday, April 21, 2015 Sheet 26 of 55

LED 8051 Controller

C749 and C750 change to 15pF for SA

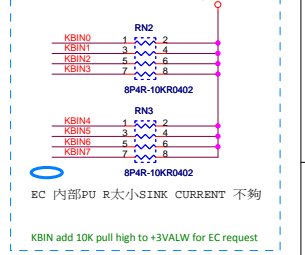
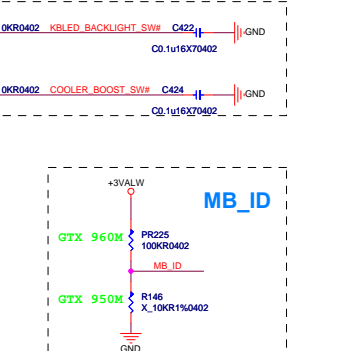
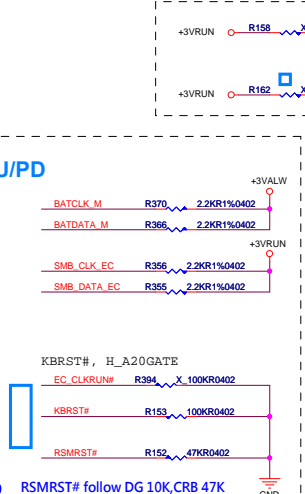
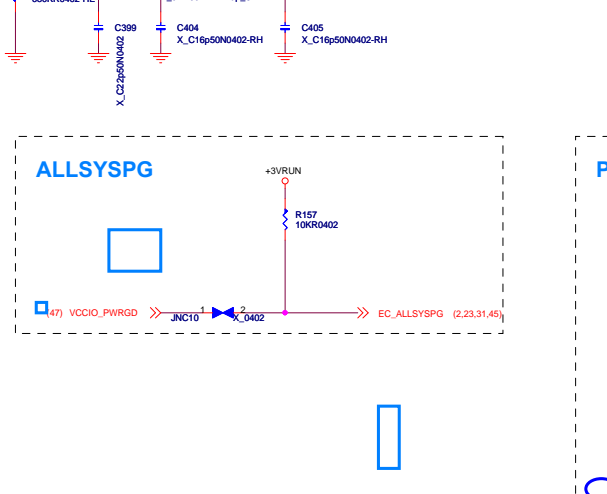
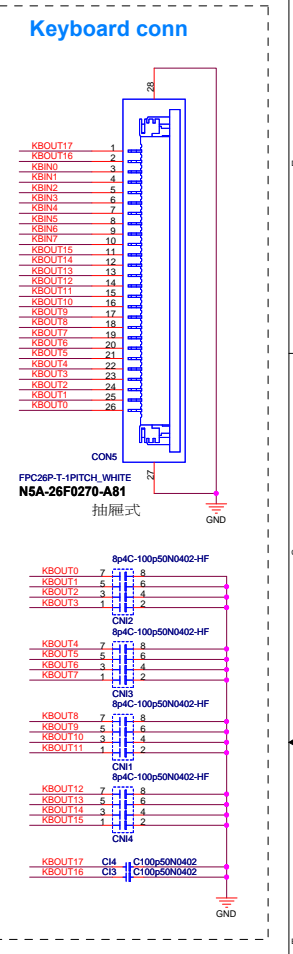
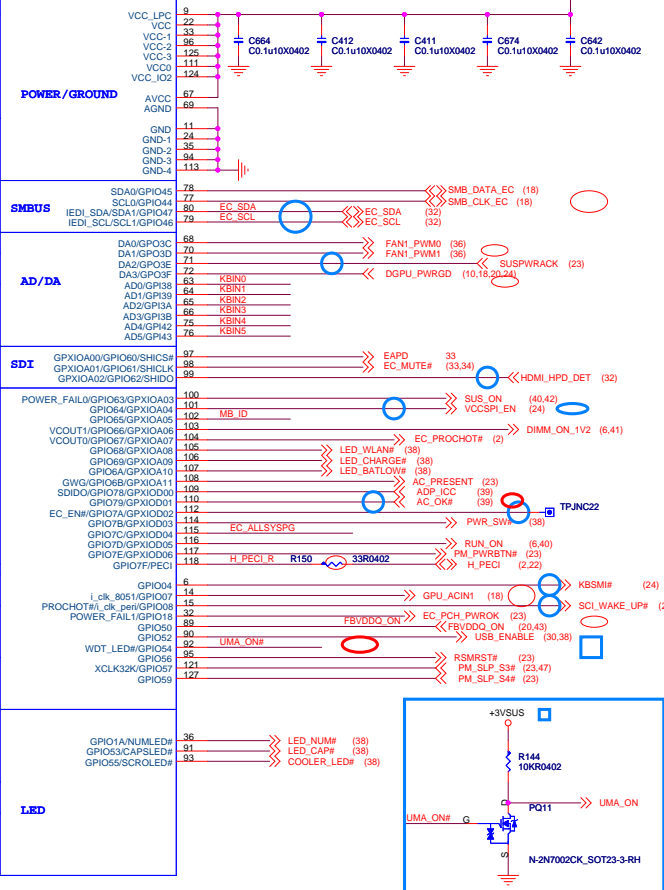
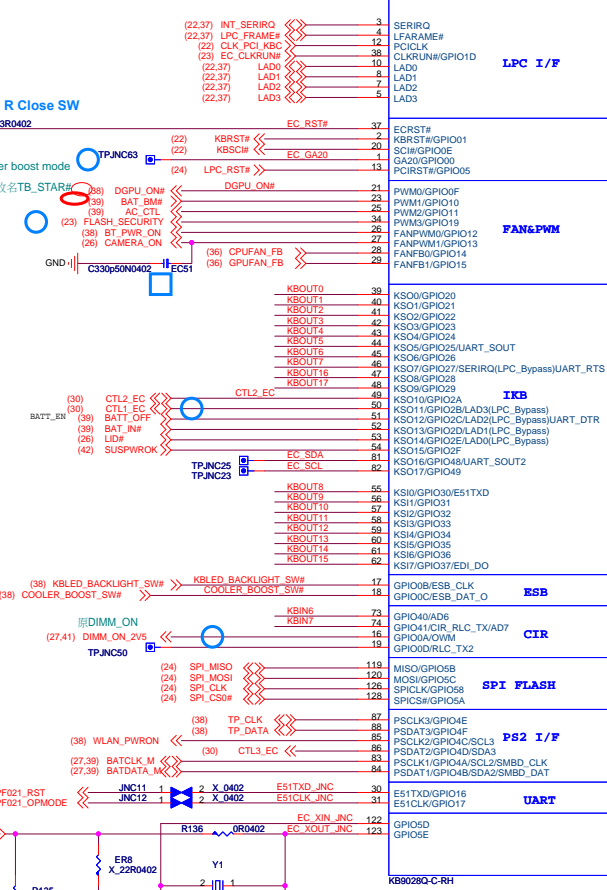
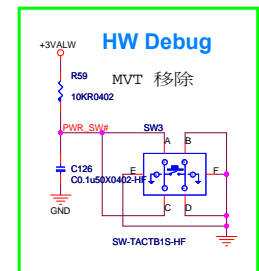
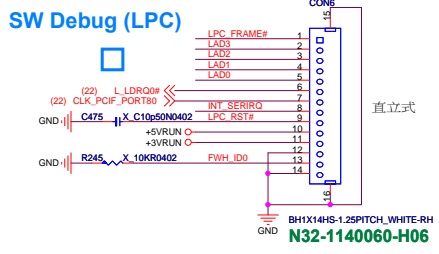
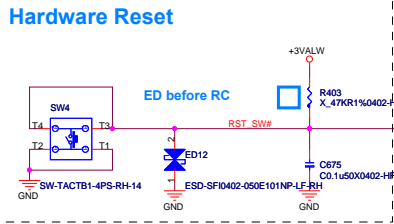


EPF021J Sink current not enough, only using BSS138 (0.22A)



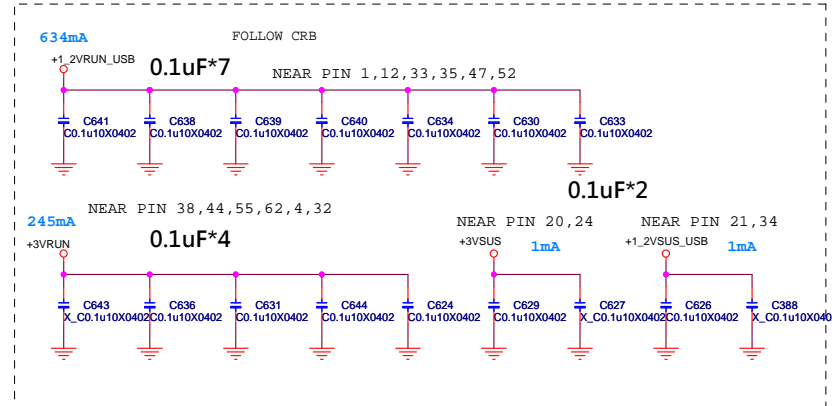
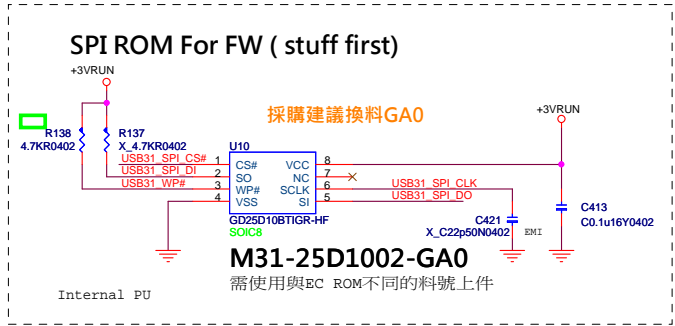
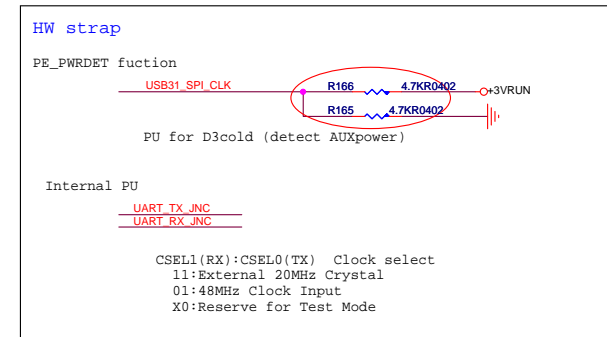
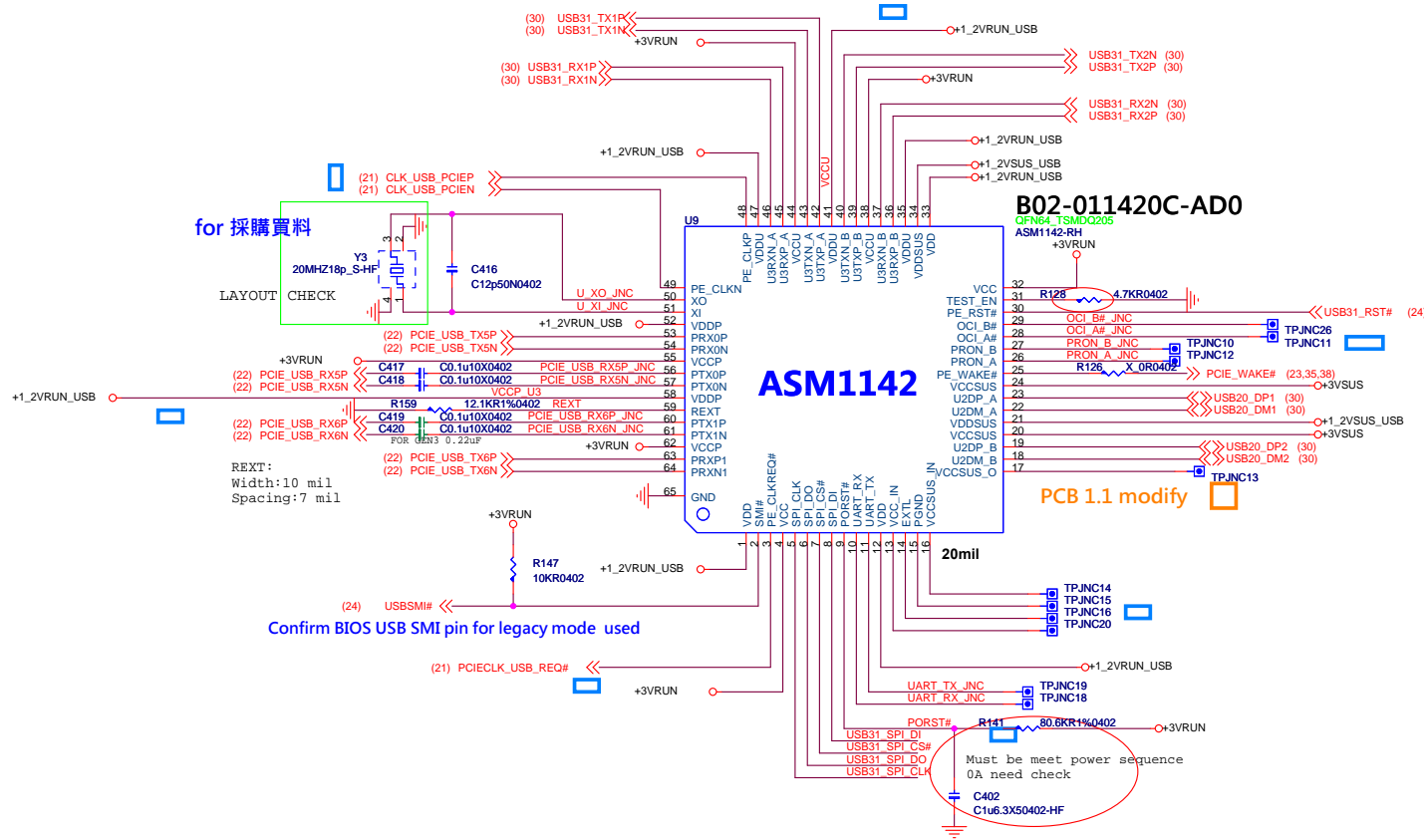
LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

KBC/EC/uP (ENE9028)

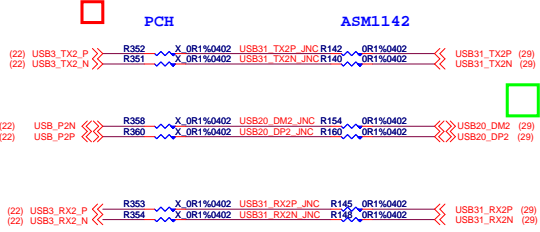


USB 3.0/ USB.3.1

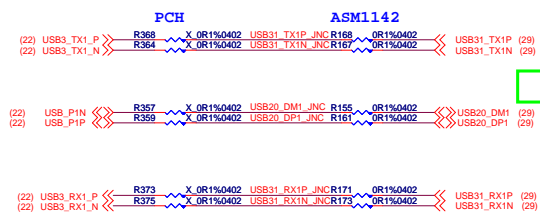
PCIE to USB 3.1



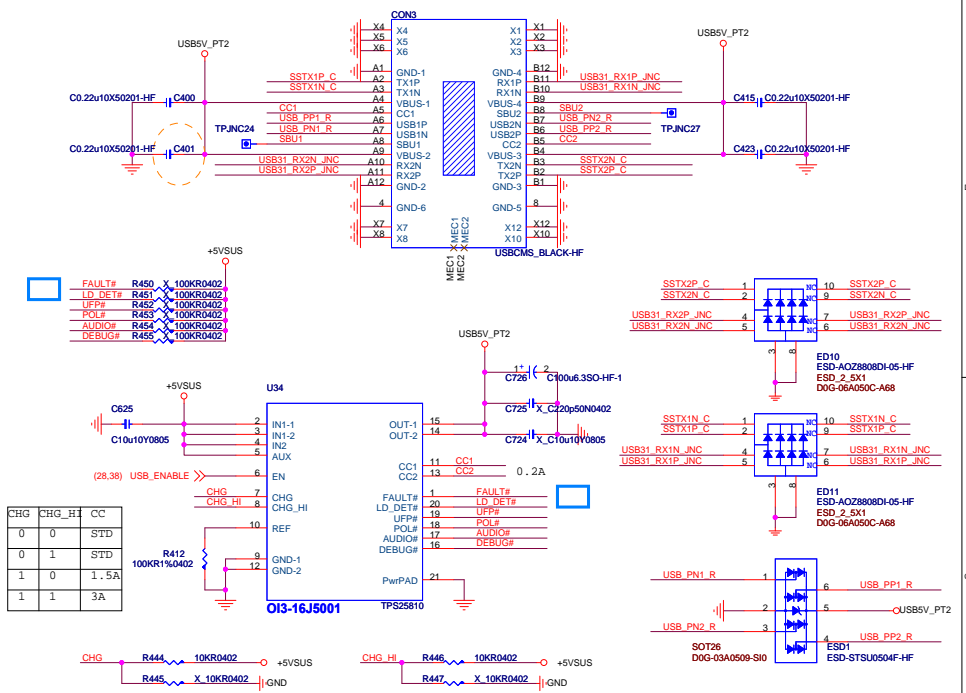
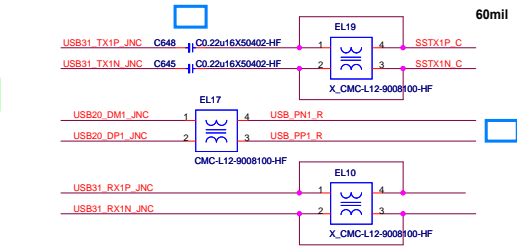
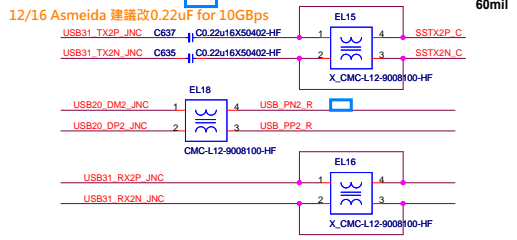
USB 3.0 Port 1



USB 3.0 Port 2

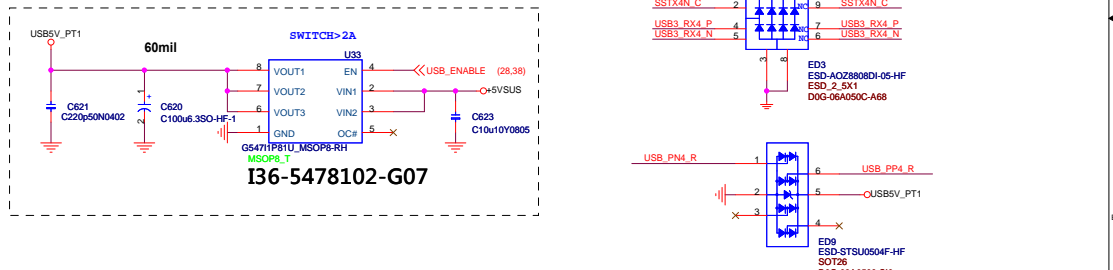
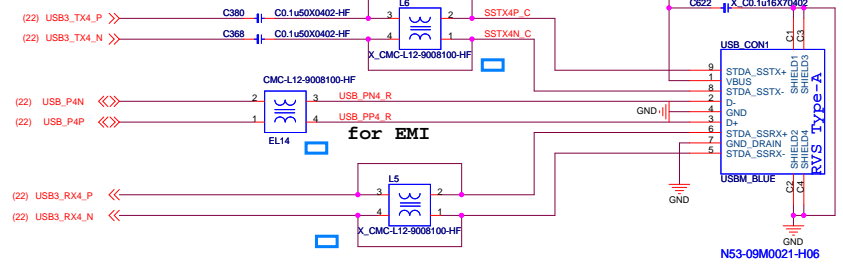


USB3.1 TYPE C



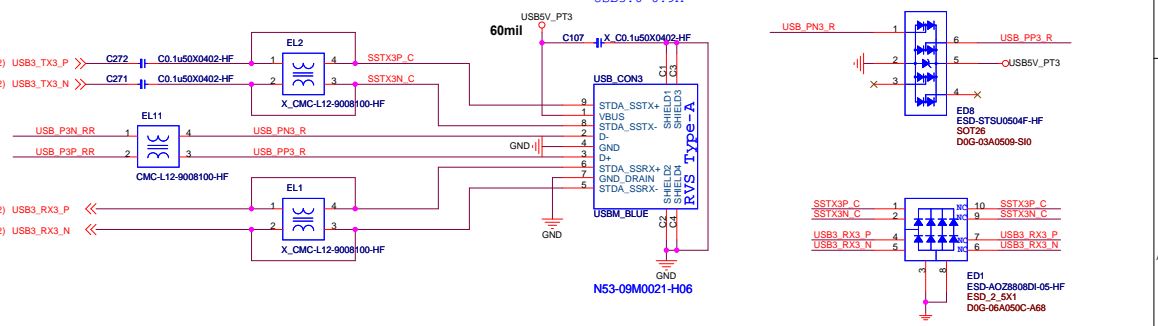
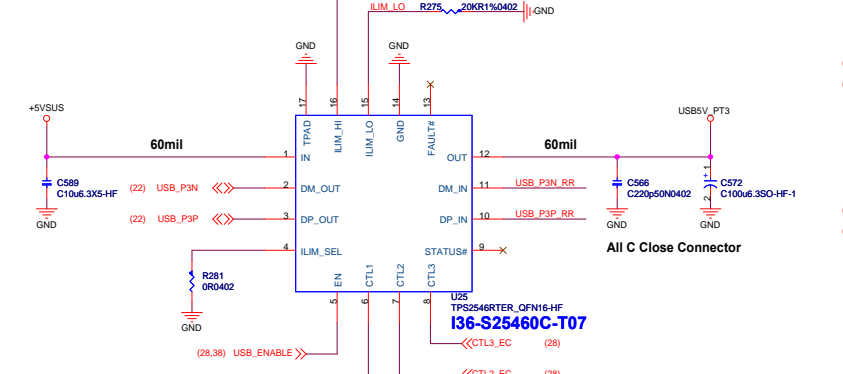
for EMI

USB3.0 CNT-1



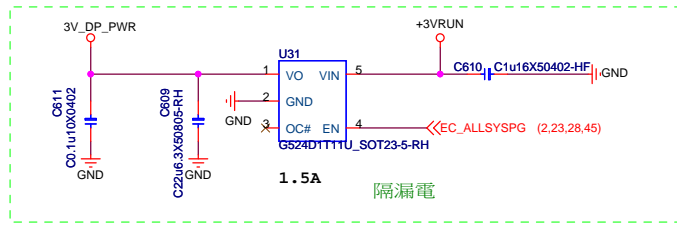
USB3.0 CNT-3

i-Charger



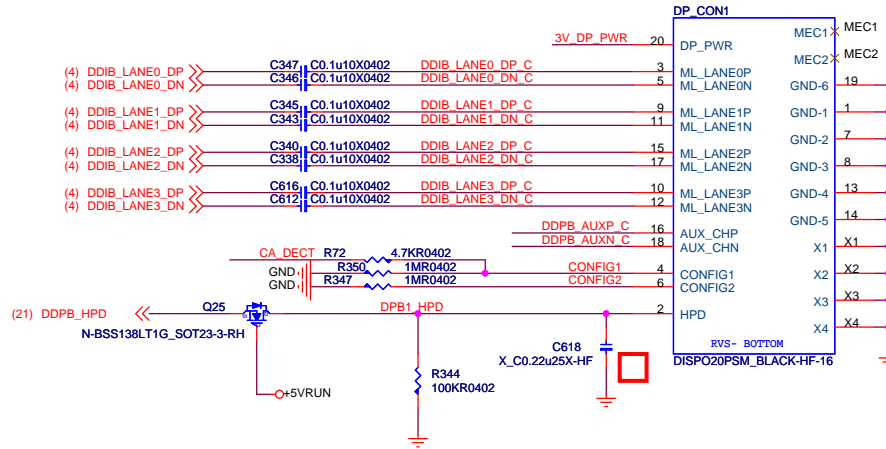
Display Port

The preset trip limit must not exceed 3A at the Upstream device connector DP_PWR pin and 1.5A at the Downstream device connector DP_PWR pin.

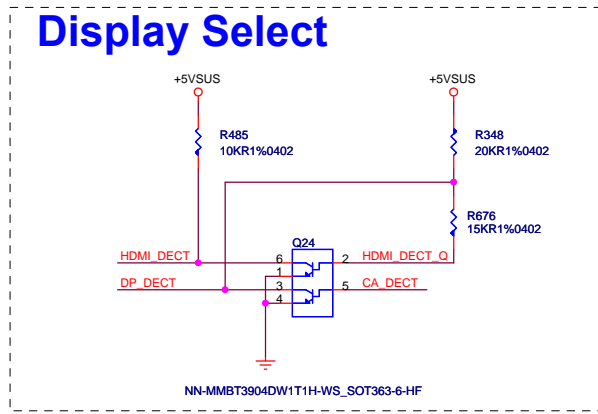


ESD Contact ± 5 KV & Air ± 15 KV

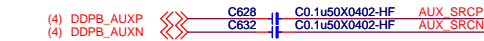
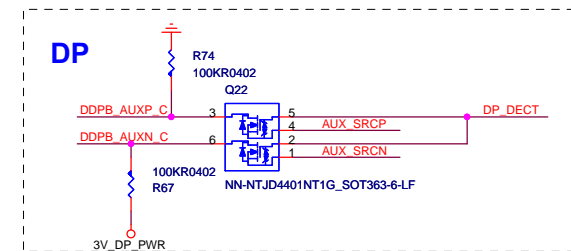
Display Port



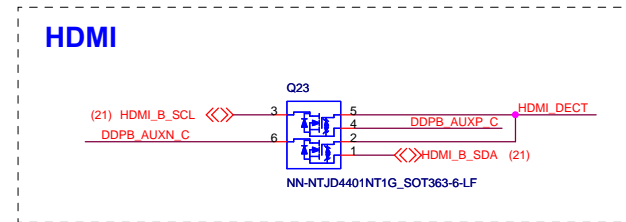
Display Select



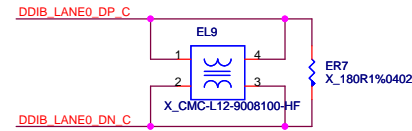
Dual Mode Switch



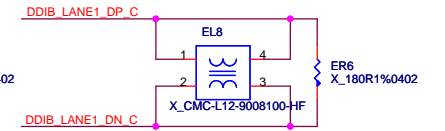
HDMI



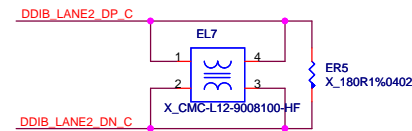
EMI Close Connector LANE0



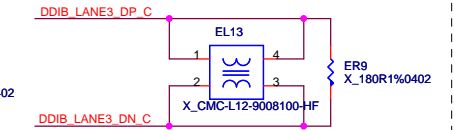
LANE1



LANE2

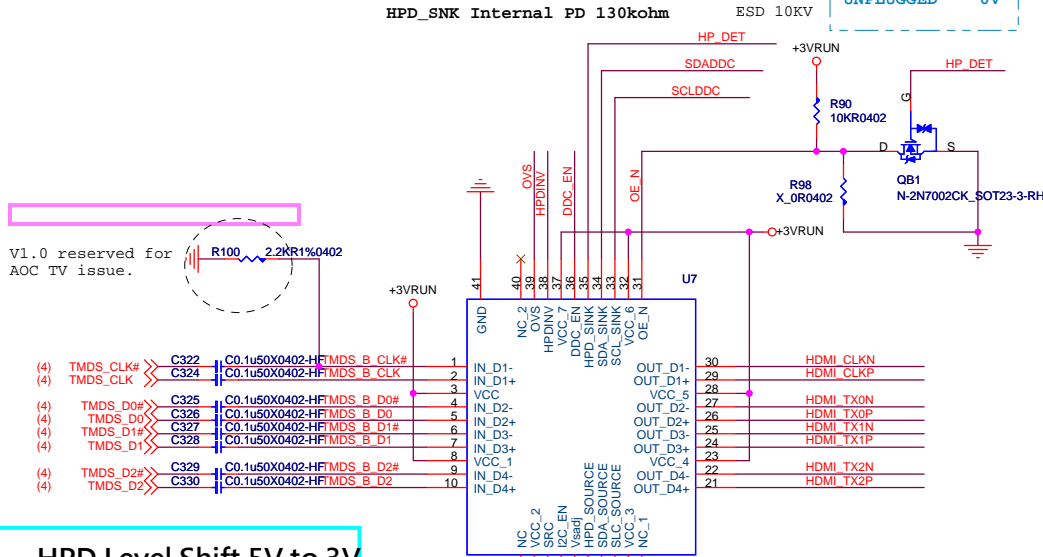


LANE3

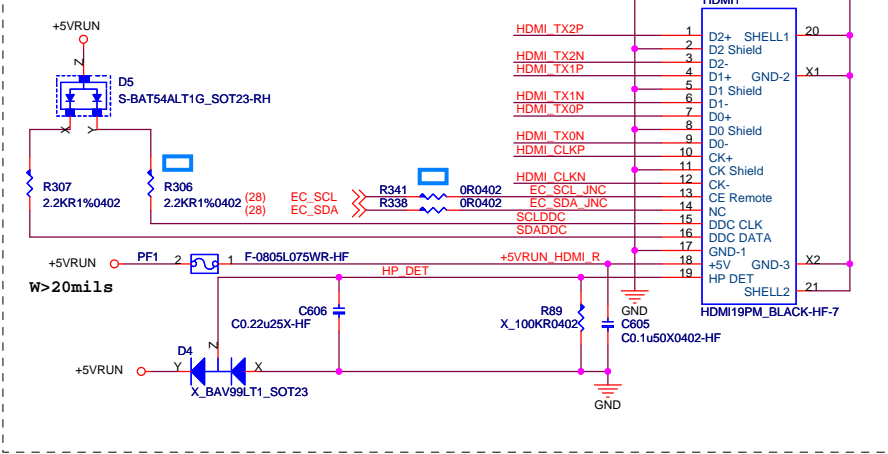


msi MICRO-STAR INT'L CO.,LTD.	
Title DP	
Size	Document Number MS-16J5
Date:	Tuesday, April 21, 2015
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Rev	0A

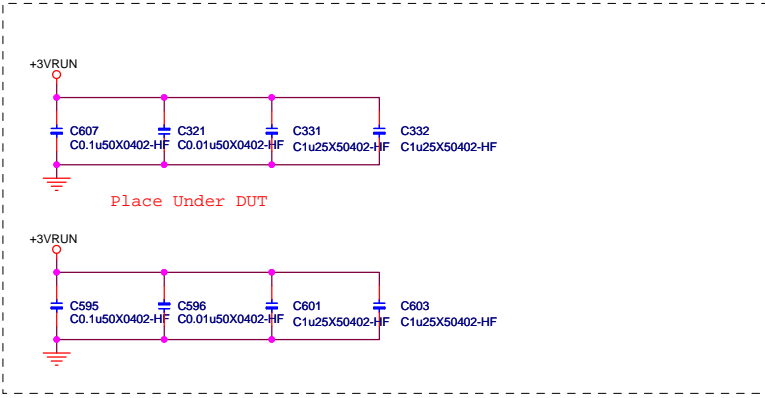
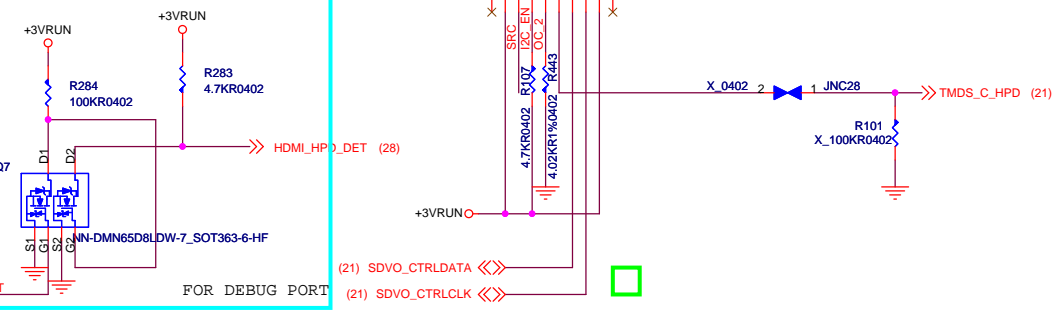
HDMI Level Shifter



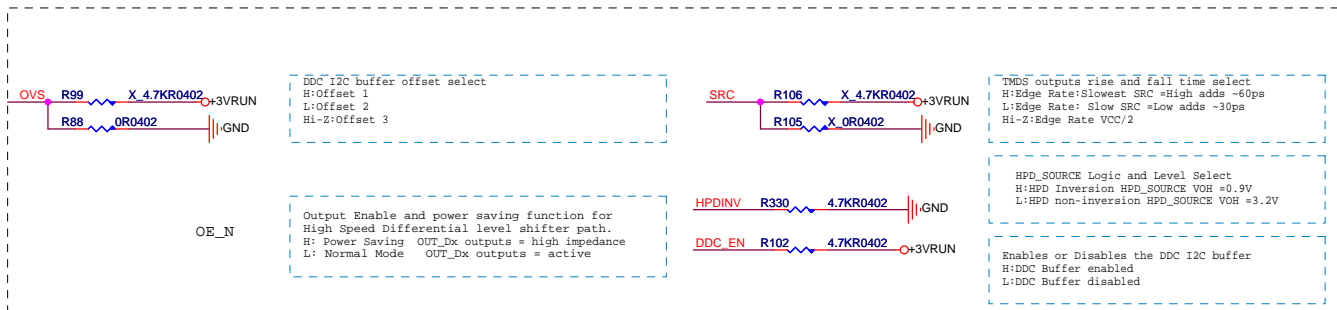
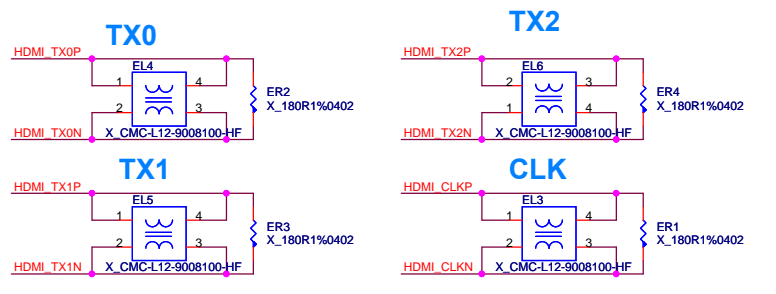
HDMI Connector



HPD Level Shift 5V to 3V



EMI Close Connector



msi MICRO-STAR INT'L CO.,LTD.

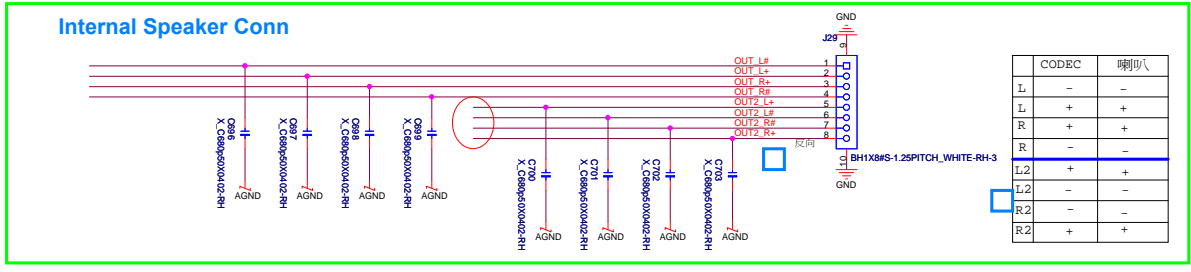
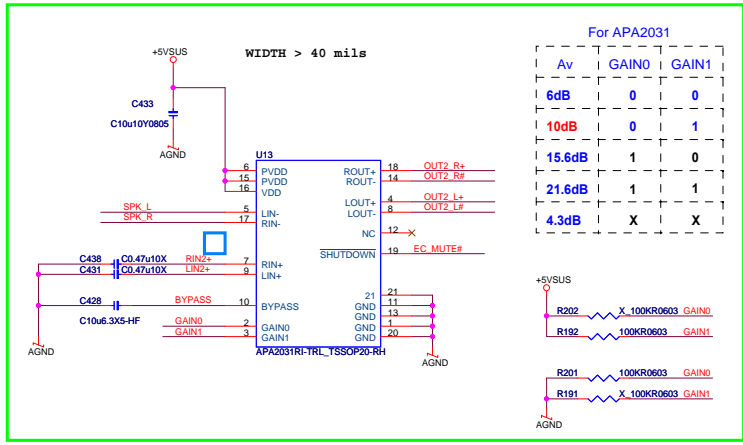
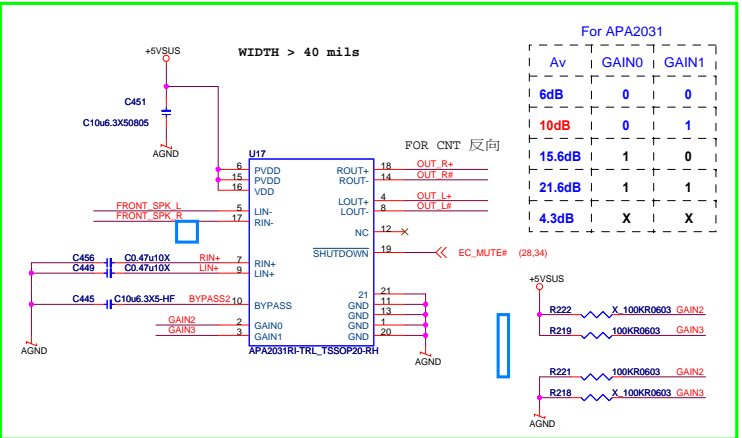
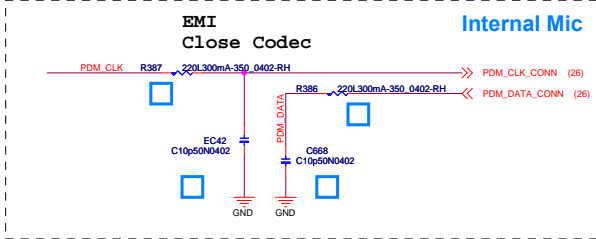
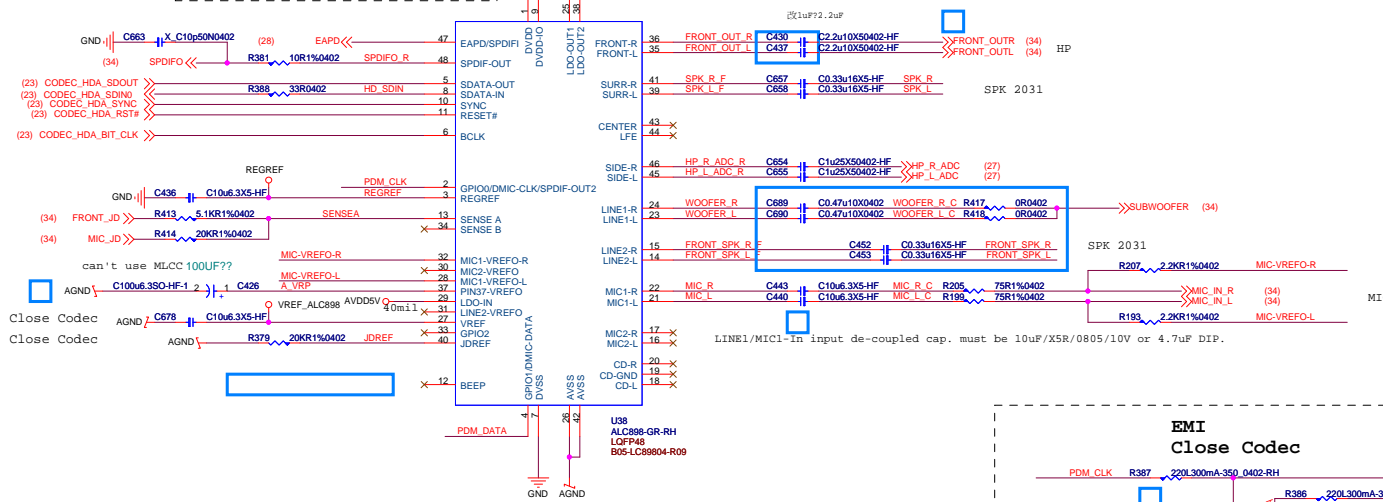
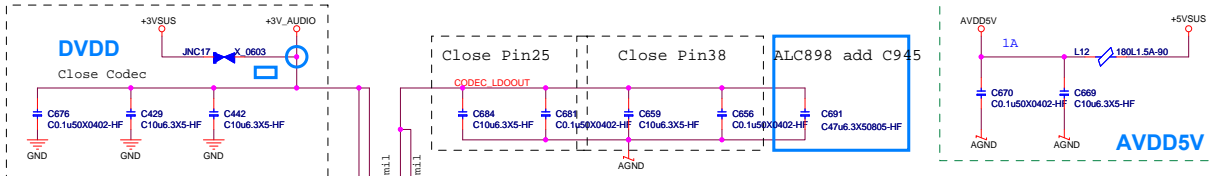
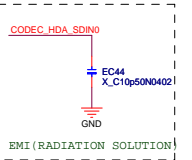
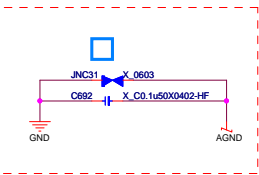
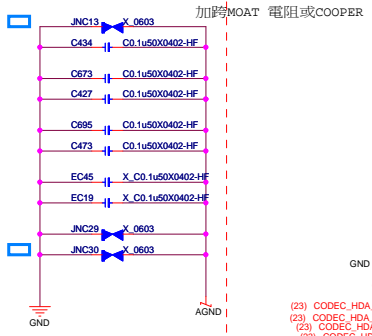
Title **HDMI DP139**

Size Document Number **MS-16J5**

Date: Tuesday, April 21, 2015 Sheet 32 of 59

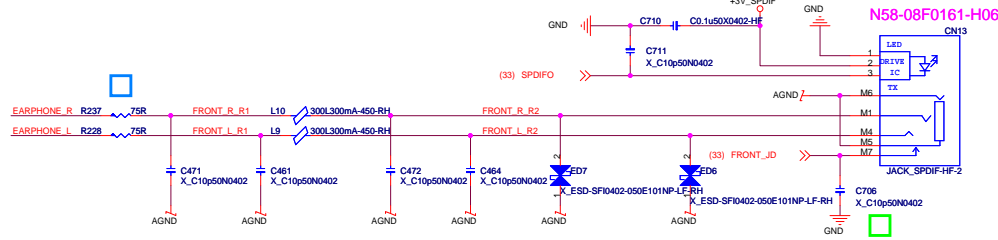
Rev **0A**

Audio CODEC/Audio AMP

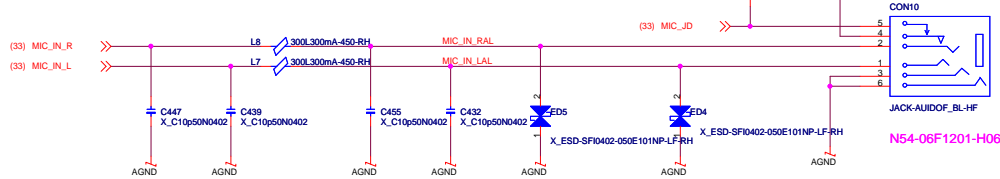


Audio CONN /Woffler

FRONT OUT



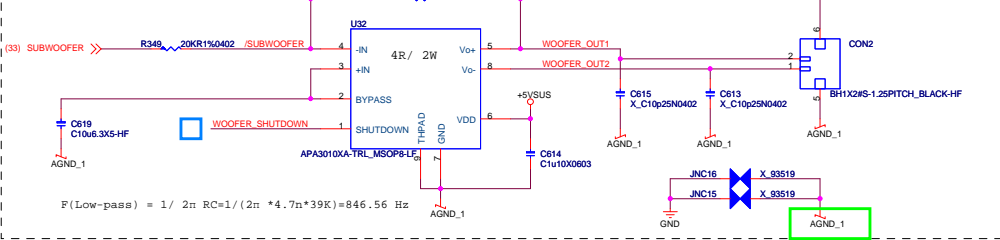
MIC IN



ALC892 SPC MAX 為 1.2Vrms
 $g_{min} = -2 * (R_{370} / R_{371}) = -2 * (40K / 20K) = -4$
 $V_{out} = 0.58V_{rms} * 4 = 2.32V_{rms}$, $P_o = (2.32^2 * 3.2) / 3.8 = 1.42W$

Woffler SPEC
 YG 3.8ohm / normal 3W, Max 3.5W
 FG 4ohm / normal 3W, Max 3.5W

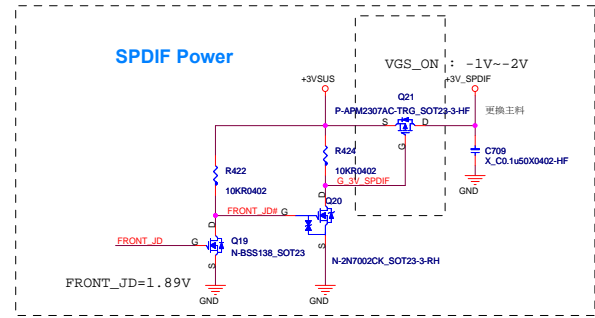
Bass Speaker



$F(Low-pass) = 1 / (2\pi RC) = 1 / (2\pi * 4.7n * 39K) = 846.56 Hz$

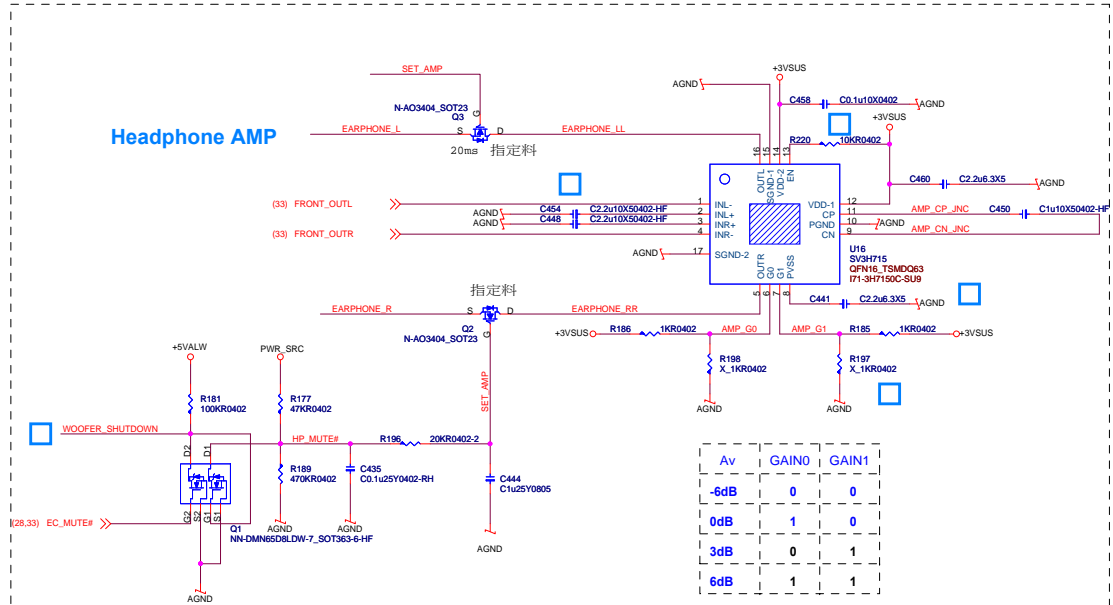
WOFFLER AMP 擺太遠獨立切AGND_1

SPDIF Power

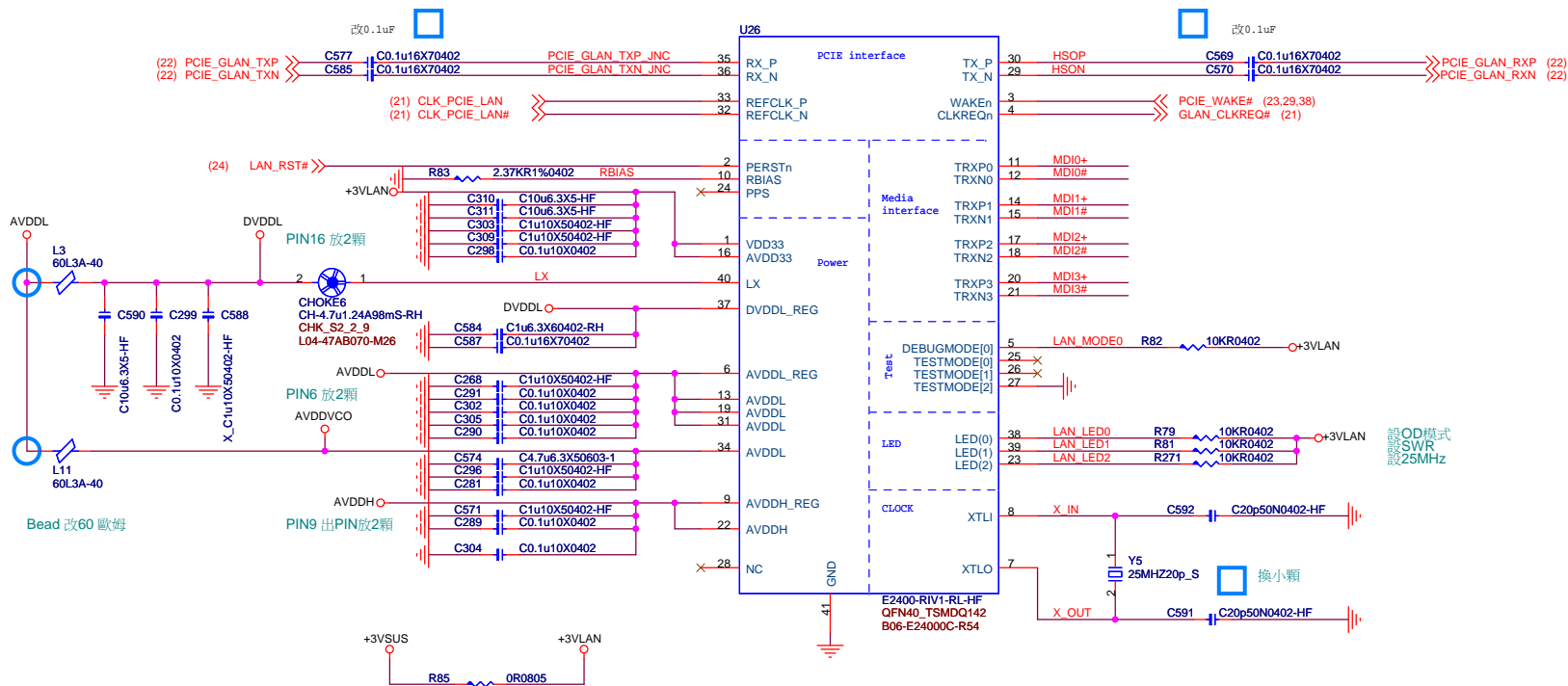


FRONT_JD=1.89V

Headphone AMP

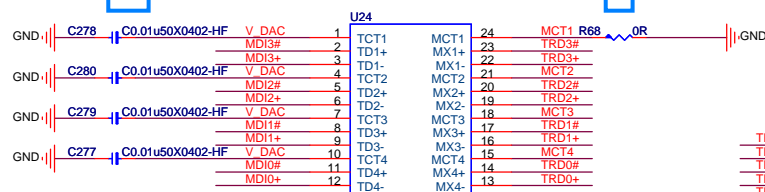


GIGA LAN(BigFoot BFN2400B)

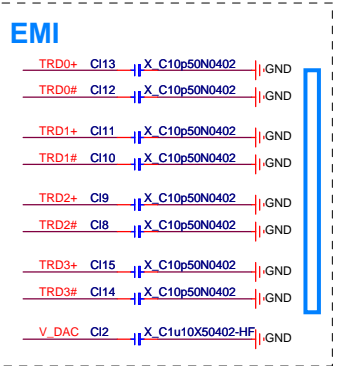
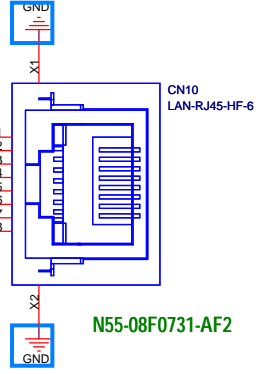


請OD模式
設置SWR
設25MHz

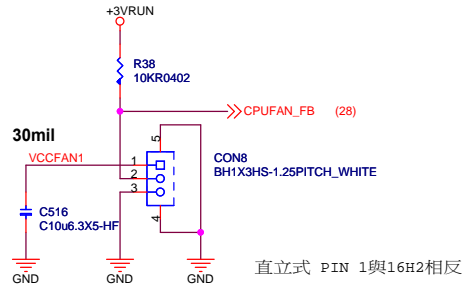
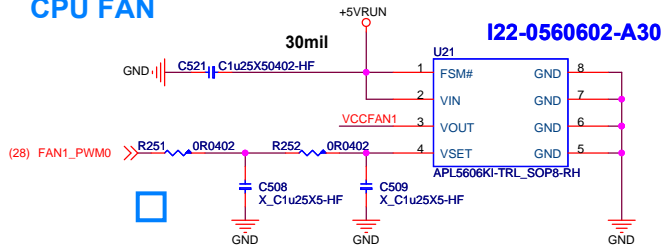
24pin使用25MIL的線寬, 線長小於5mm連接GND



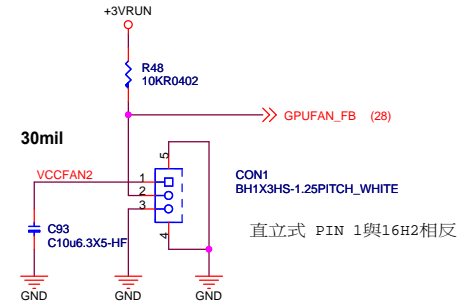
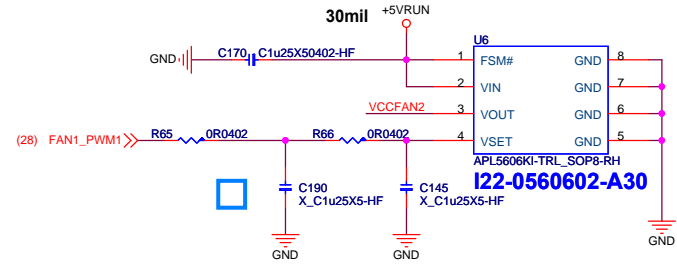
OL5-7966001
FOOTPRINT 不改



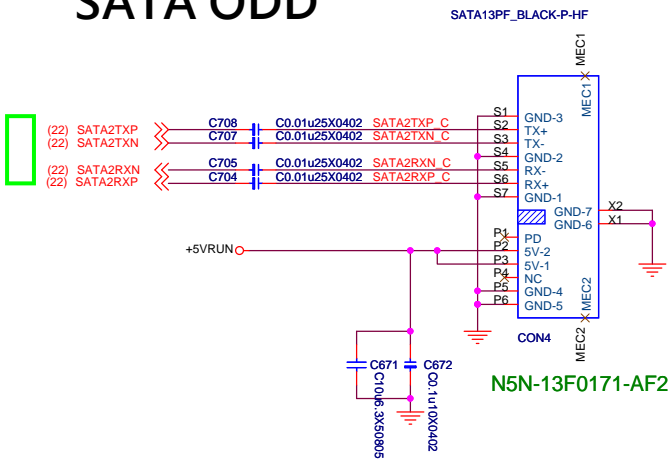
CPU FAN



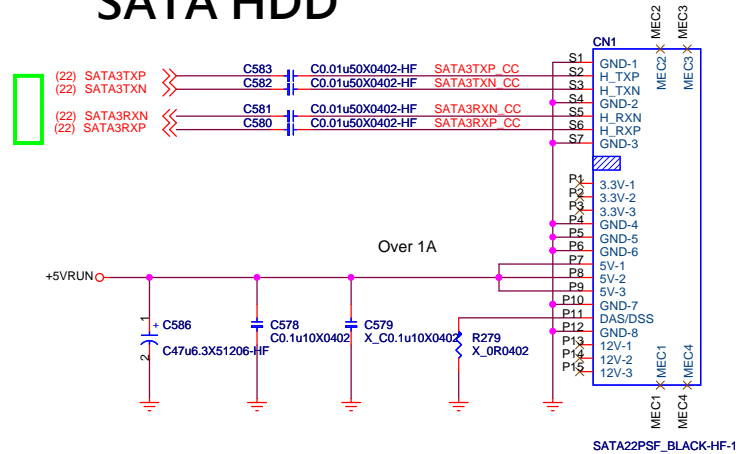
DGPU FAN



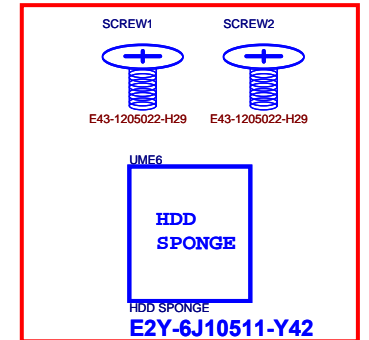
SATA ODD



SATA HDD

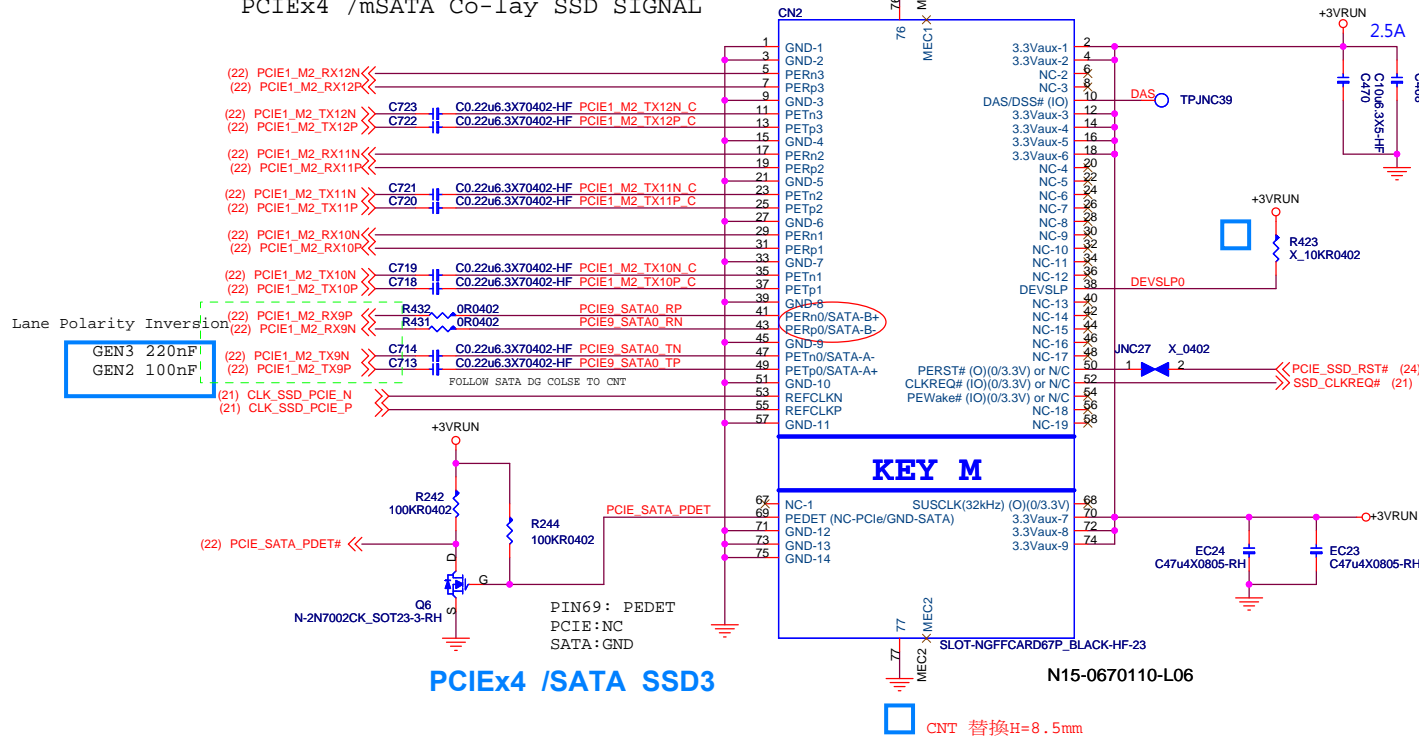


- 22. GND
- 21. TX
- 20. TX#
- 19. GND
- 18. RX#
- 17. RX
- 16. GND
- 15. V33
- 14. V33
- 13. V33
- 12. GND
- 11. GND
- 10. GND
- 9. V5
- 8. V5
- 7. V5
- 6. GND
- 5. Reserved
- 4. GND
- 3. V12
- 2. V12
- 1. V12

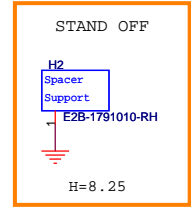
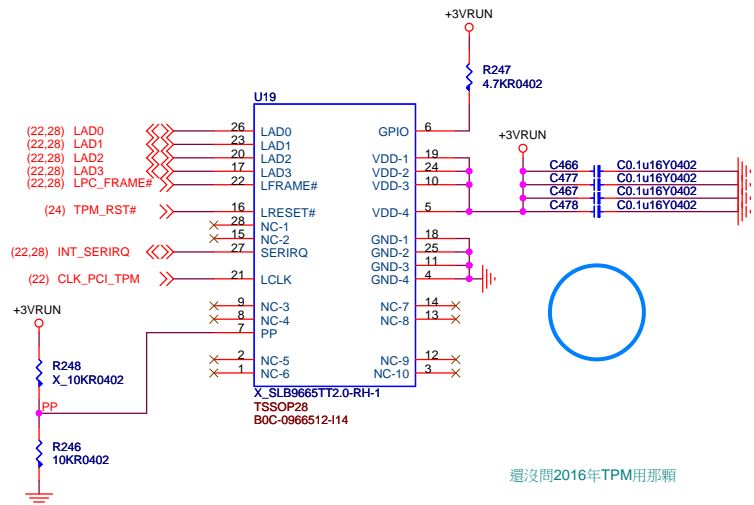


Title		
ODD/HDD/FAN		
Size	Document Number	Rev
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PCIEx4 /mSATA Co-lay SSD SIGNAL

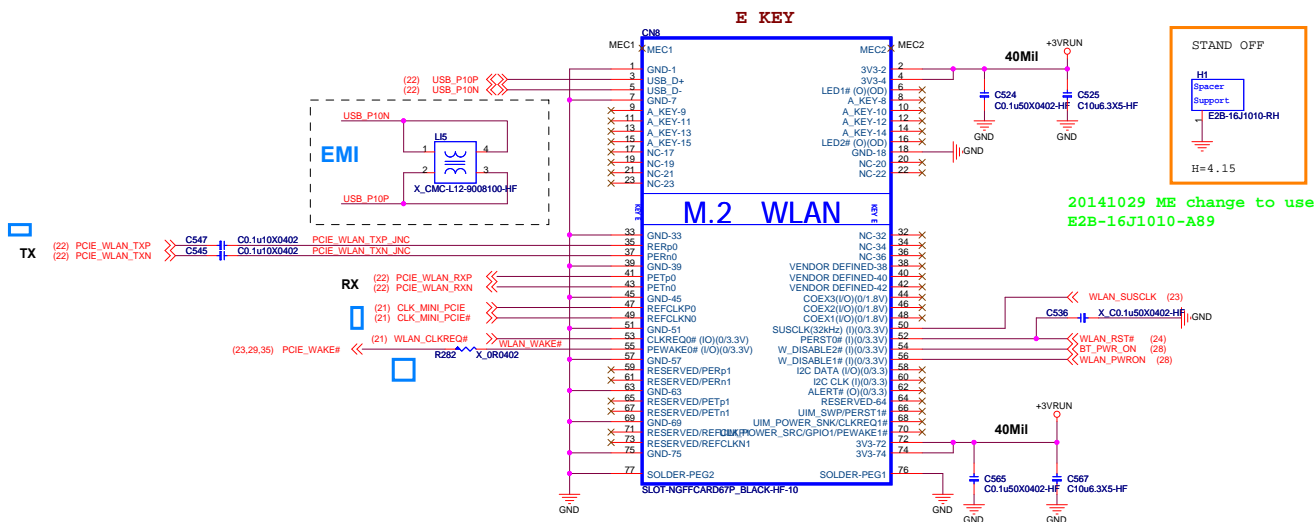


TPM

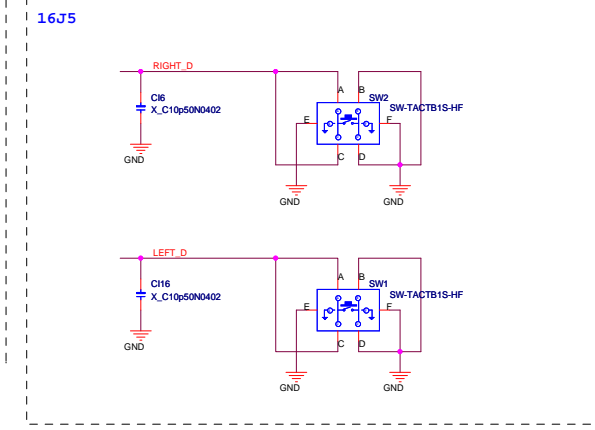
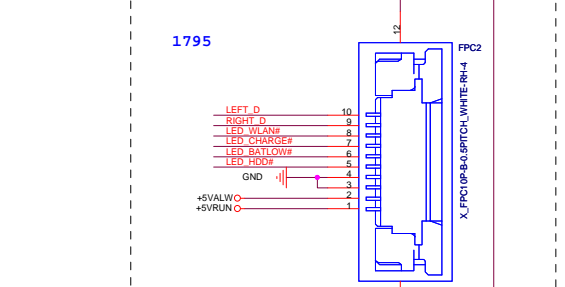
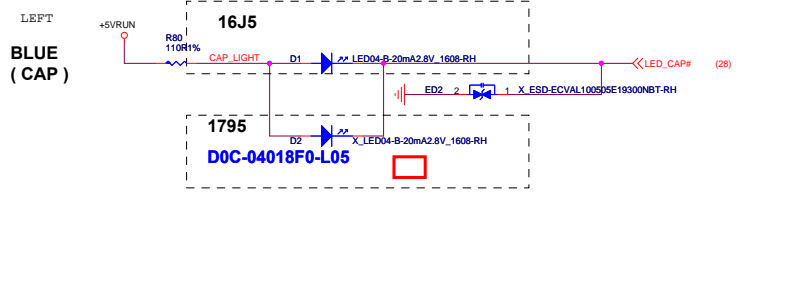
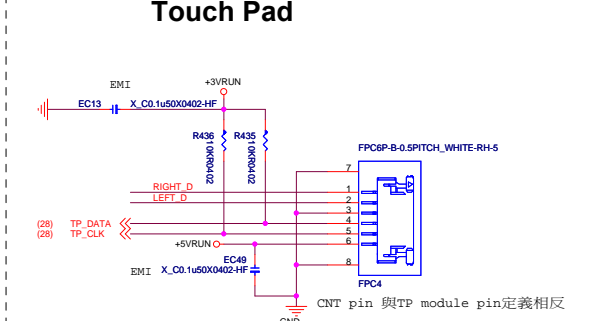
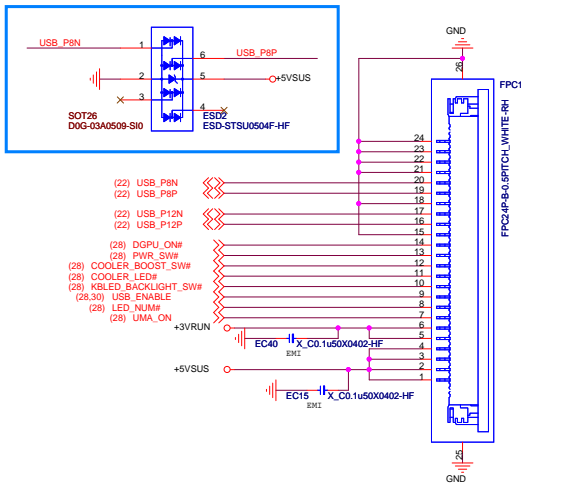
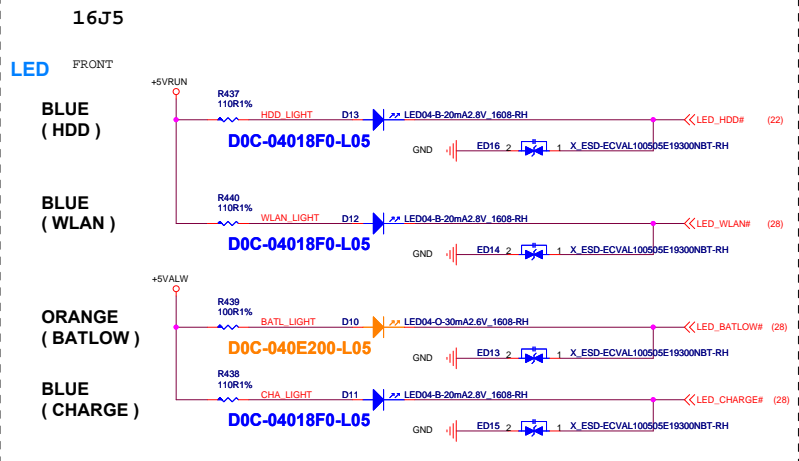


WLAN

WLAN/LED

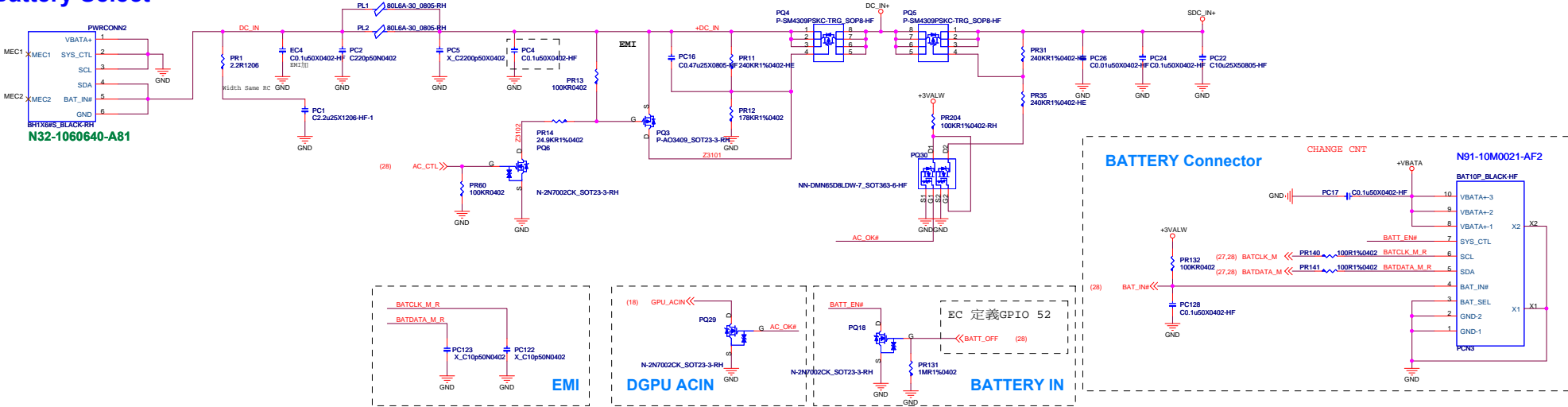


Pin 1	GND	Pin 2	3.3V
Pin 3	USB_D+	Pin 4	3.3V
Pin 5	USB_D-	Pin 6	LED1#
Pin 7	GND	Pin 8	Module Key
Pin 9	Module Key	Pin 10	Module Key
Pin 11	Module Key	Pin 12	Module Key
Pin 13	Module Key	Pin 14	Module Key
Pin 15	Module Key	Pin 16	Module Key
Pin 17	N/C	Pin 17	LED2#
Pin 18	N/C	Pin 18	GND
Pin 19	N/C	Pin 19	N/C
Pin 20	N/C	Pin 20	N/C
Pin 21	N/C	Pin 21	N/C
Pin 22	N/C	Pin 22	N/C
Pin 23	Module Key	Pin 23	N/C
Pin 24	Module Key	Pin 24	Module Key
Pin 25	Module Key	Pin 25	Module Key
Pin 26	Module Key	Pin 26	Module Key
Pin 27	Module Key	Pin 27	Module Key
Pin 28	Module Key	Pin 28	Module Key
Pin 29	Module Key	Pin 29	Module Key
Pin 30	Module Key	Pin 30	Module Key
Pin 31	Module Key	Pin 31	Module Key
Pin 32	N/C	Pin 32	N/C
Pin 33	GND	Pin 33	N/C
Pin 34	PERP0	Pin 34	N/C
Pin 35	PERP0	Pin 35	N/C
Pin 36	PERP0	Pin 36	N/C
Pin 37	PERP0	Pin 37	N/C
Pin 38	GND	Pin 38	Clink Reset (1 3.3V)
Pin 39	GND	Pin 39	N/C
Pin 40	PETP0	Pin 40	N/C
Pin 41	PETP0	Pin 41	N/C
Pin 42	PETN0	Pin 42	N/C
Pin 43	PETN0	Pin 43	N/C
Pin 44	GND	Pin 44	N/C
Pin 45	GND	Pin 45	N/C
Pin 46	REFCLKP0	Pin 46	N/C
Pin 47	REFCLKP0	Pin 47	N/C
Pin 48	REFCLKN0	Pin 48	N/C
Pin 49	REFCLKN0	Pin 49	N/C
Pin 50	GND	Pin 50	N/C (SUSCLK (32kHz) for DsX)
Pin 51	GND	Pin 51	N/C
Pin 52	CLKREQ0#	Pin 52	PERST0#
Pin 53	PERWAKE0#	Pin 53	BT_EN (W_DISABLE#)
Pin 54	GND	Pin 54	WLAN_EN (W_DISABLE#)
Pin 55	GND	Pin 55	N/C
Pin 56	GND	Pin 56	N/C
Pin 57	GND	Pin 57	N/C
Pin 58	GND	Pin 58	N/C
Pin 59	GND	Pin 59	N/C
Pin 60	GND	Pin 60	N/C
Pin 61	GND	Pin 61	N/C
Pin 62	GND	Pin 62	N/C
Pin 63	GND	Pin 63	N/C
Pin 64	GND	Pin 64	N/C
Pin 65	GND	Pin 65	N/C
Pin 66	GND	Pin 66	N/C
Pin 67	GND	Pin 67	N/C
Pin 68	GND	Pin 68	N/C
Pin 69	GND	Pin 69	N/C
Pin 70	GND	Pin 70	N/C
Pin 71	GND	Pin 71	N/C
Pin 72	GND	Pin 72	N/C
Pin 73	N/C	Pin 73	3.3V
Pin 74	GND	Pin 74	3.3V

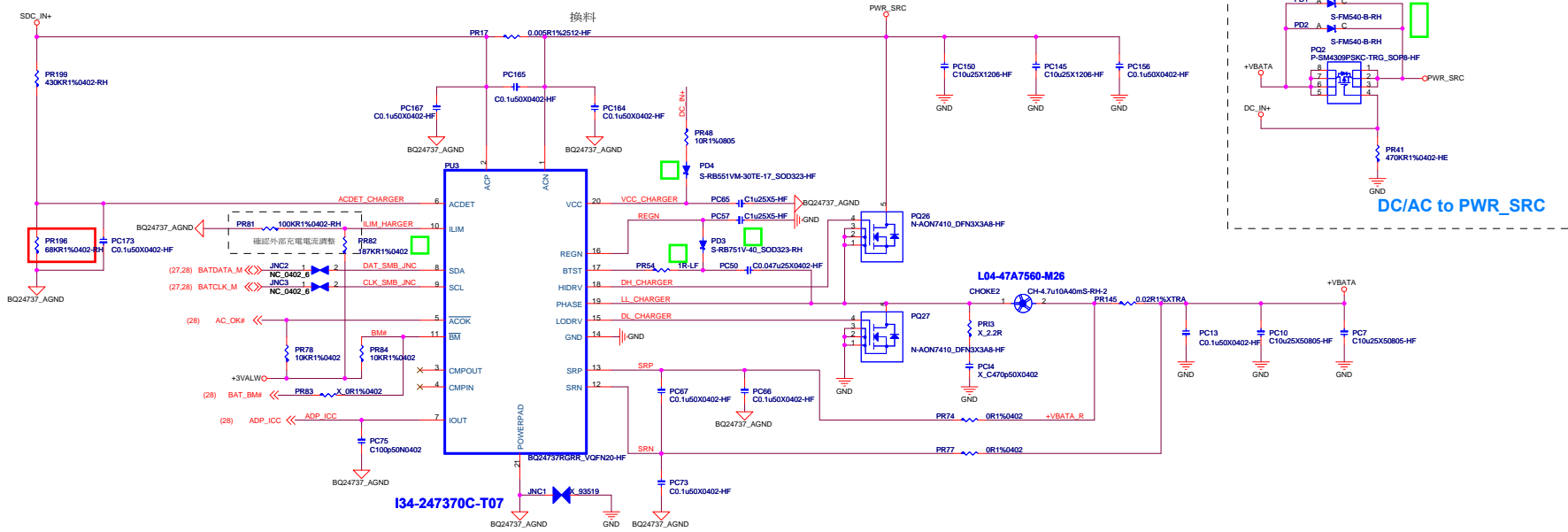


Battery Select/Charger

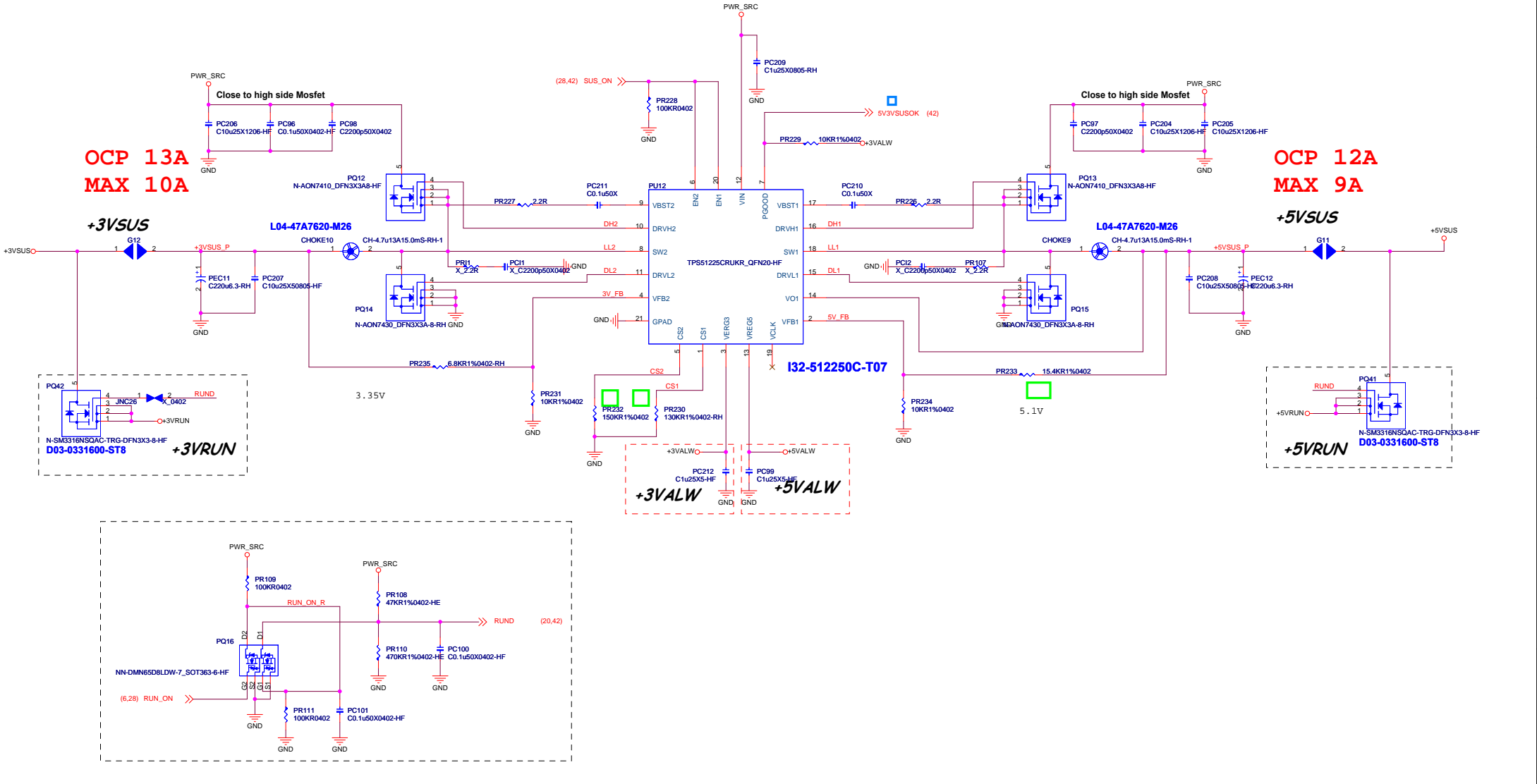
Battery Select



Battery Charger



System Power



**OCF 13A
MAX 10A**

**OCF 12A
MAX 9A**

+3VSUS

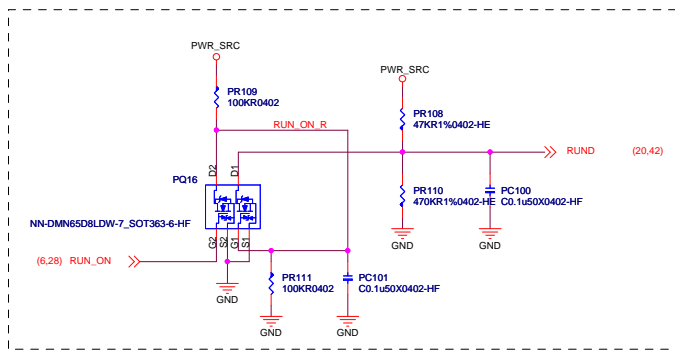
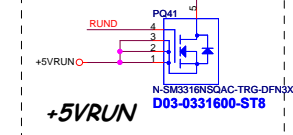
+5VSUS

+3VRUN

+5VRUN

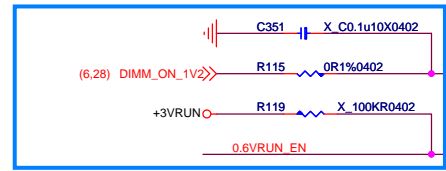
+3VALW

+5VALW



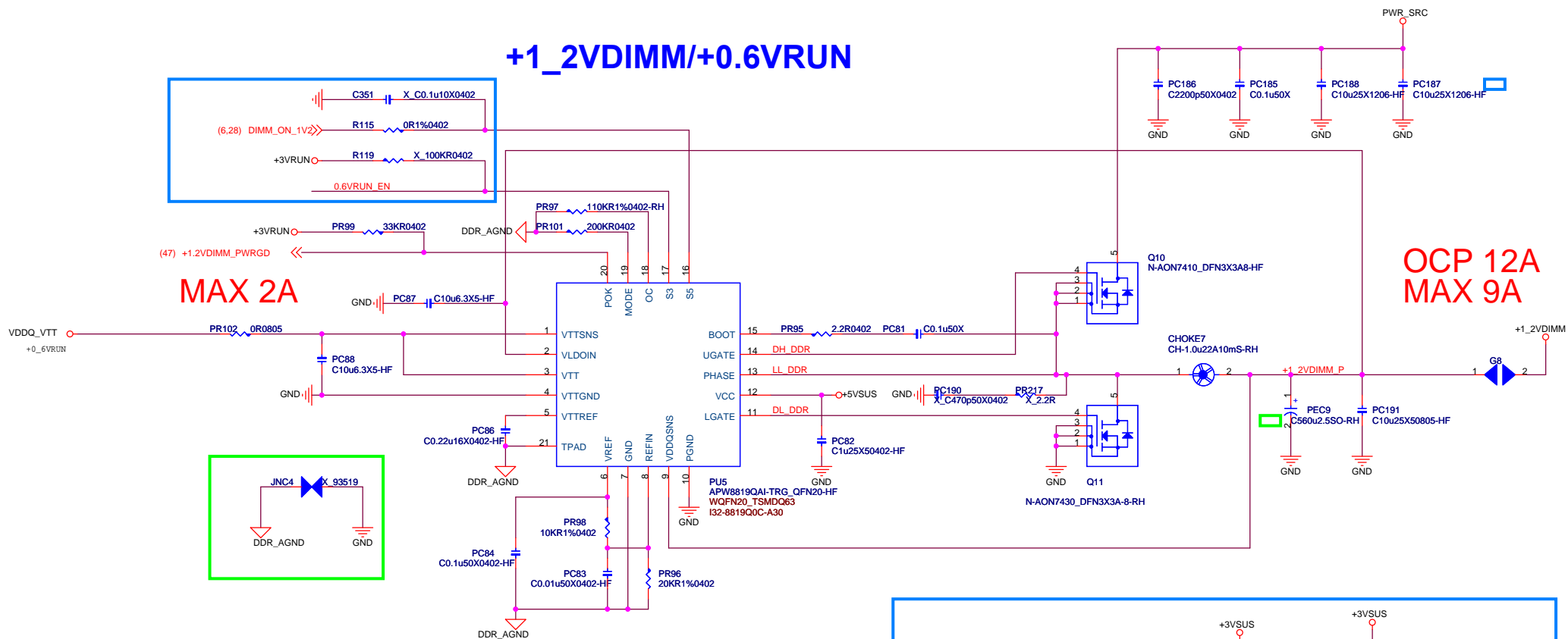
msi MICRO-STAR INT'L CO.,LTD.	
Title System Power	
Size	Document Number
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+1_2VDIMM/+0.6VRUN



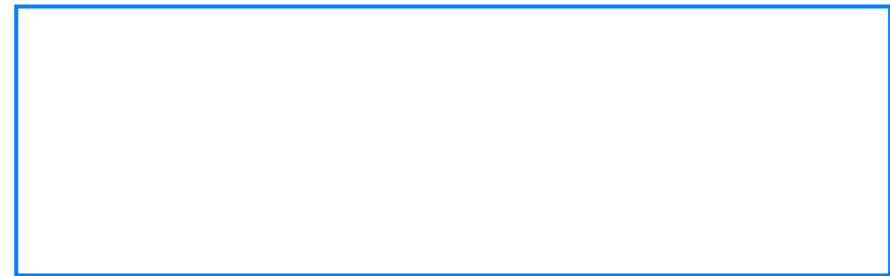
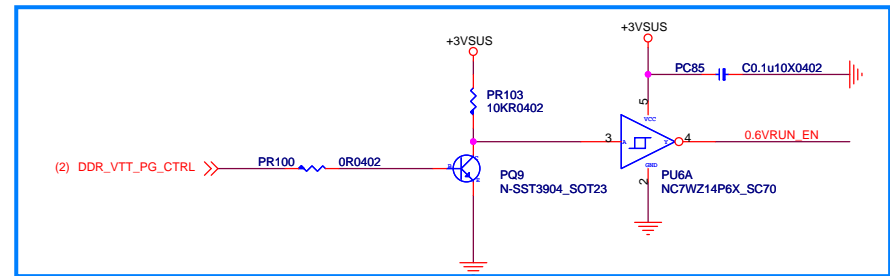
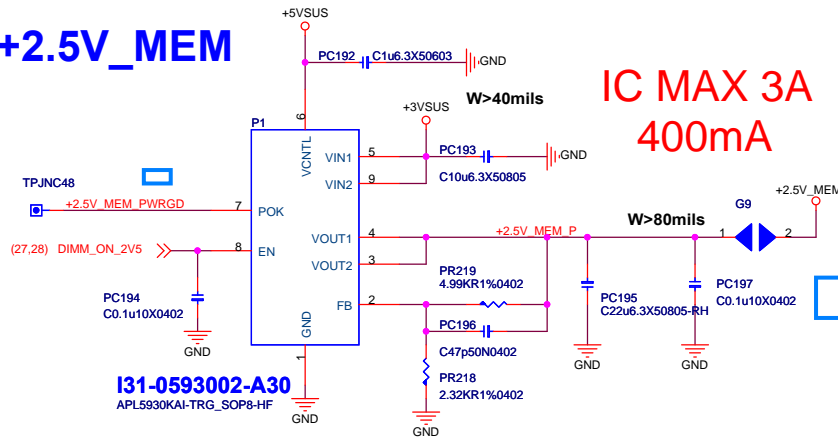
MAX 2A

OCP 12A
MAX 9A

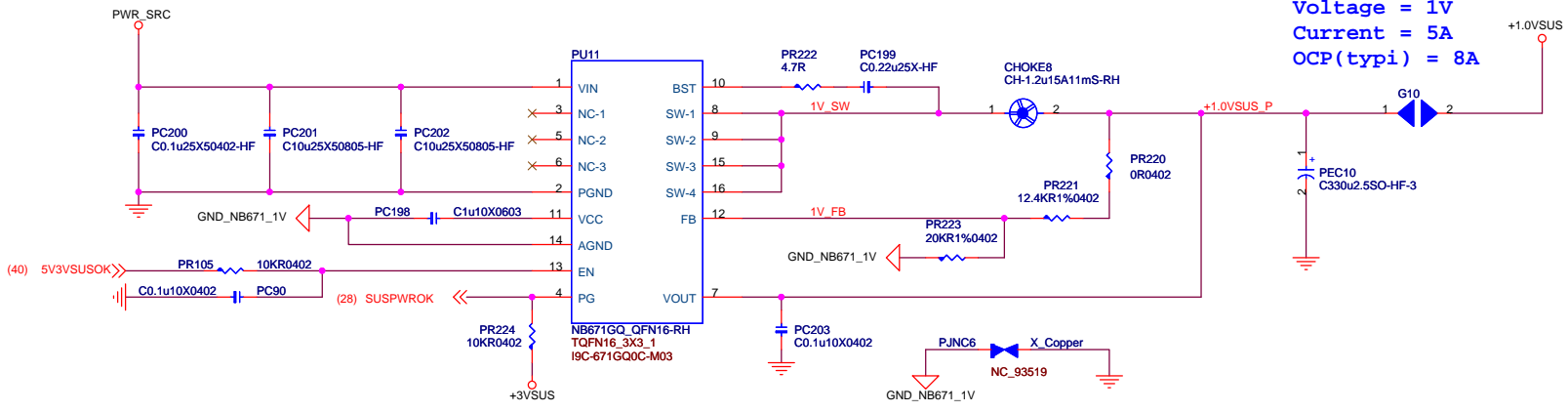


+2.5V_MEM

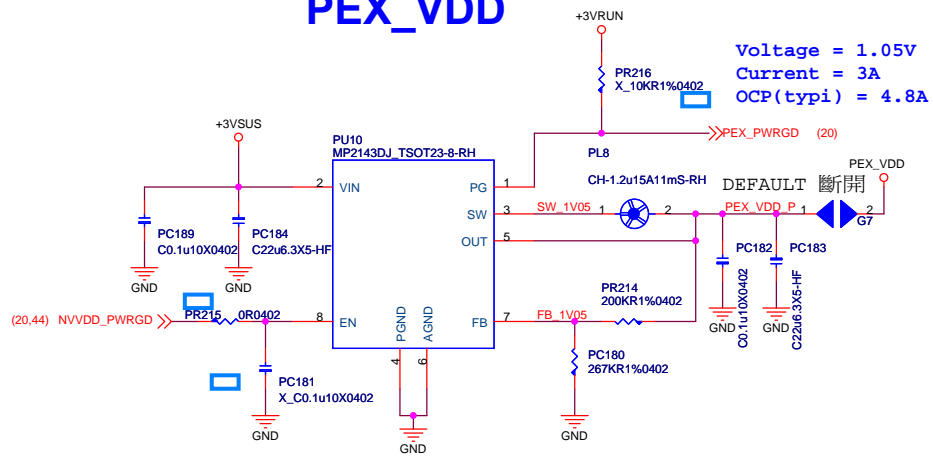
IC MAX 3A
400mA



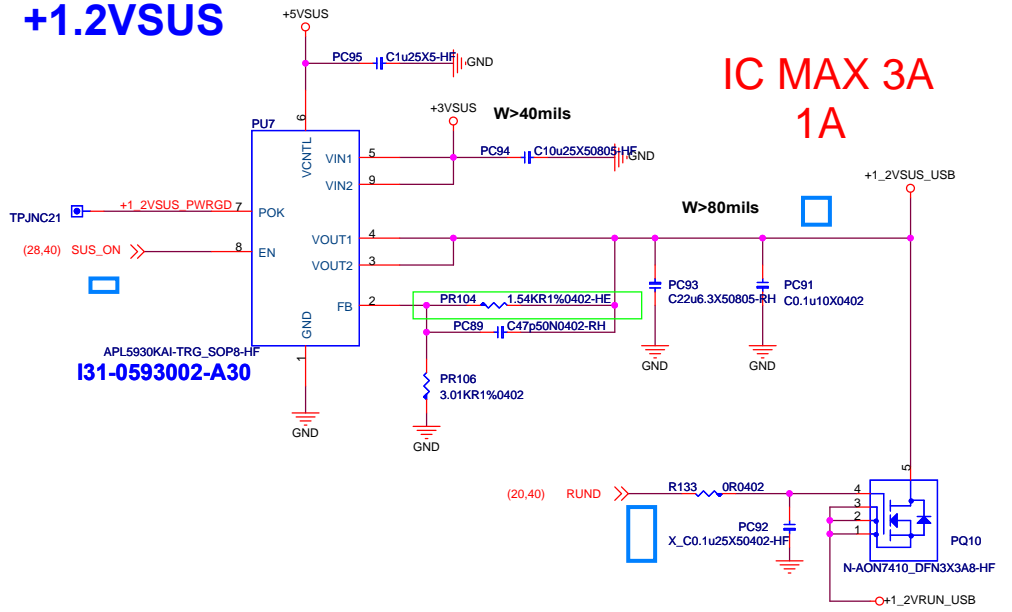
+1VSUS



PEX_VDD



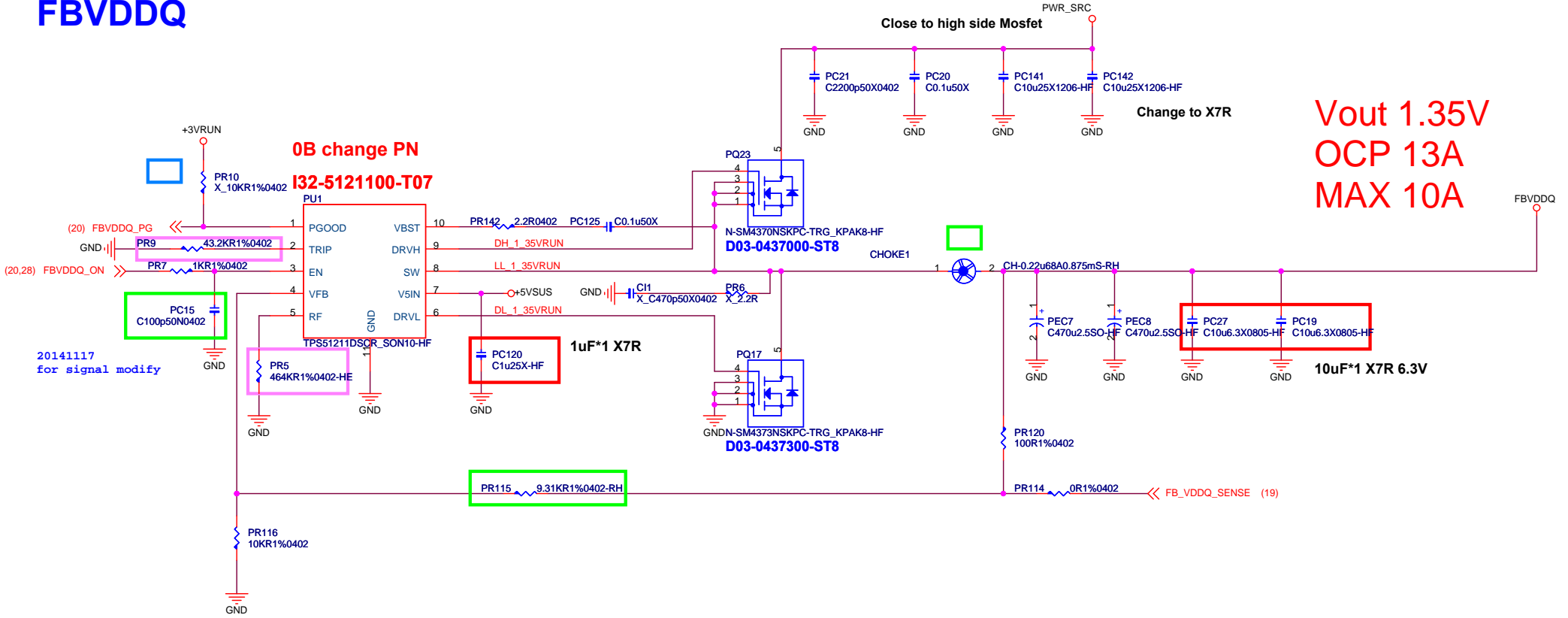
+1.2VSUS



msi MICRO-STAR INT'L CO.,LTD.		
Title 1VSUS / PEX_VDD/1.2VSUS		
Size	Document Number MS-16J5	Rev 0A
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DGPU POWER FBVDDQ

FBVDDQ



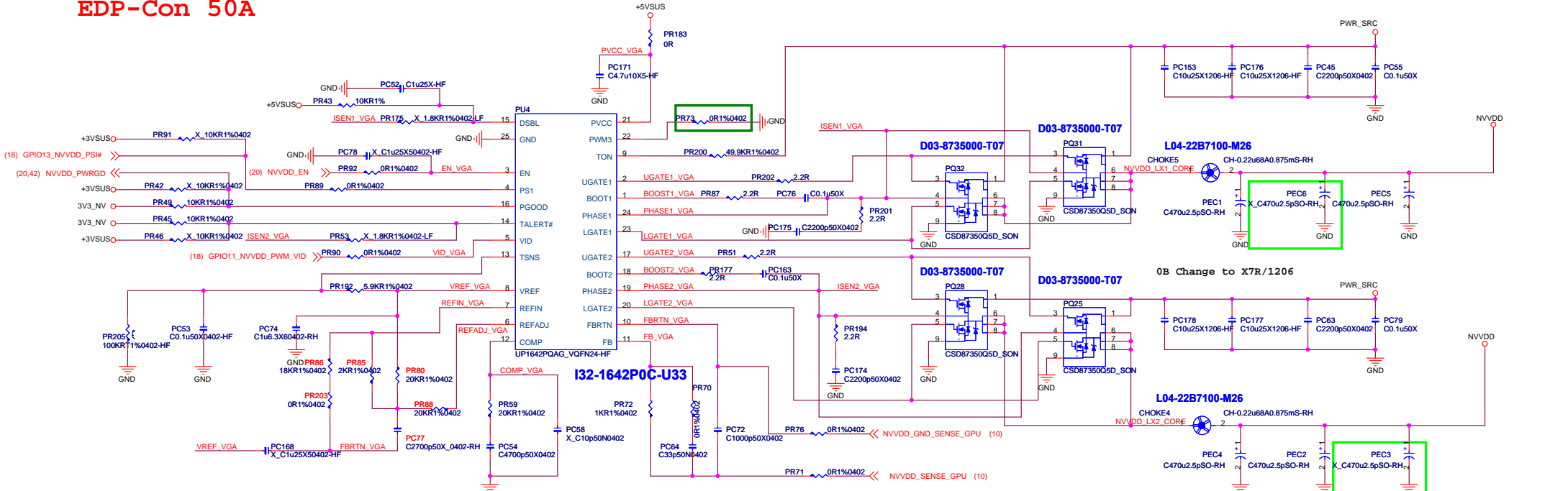
msi MICRO-STAR INT'L CO.,LTD.		
Title DGPU POWER FBVDDQ		
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DGPU POWER / UP1642PQAG

EDP-Peak 87A
EDP-Con 50A

DGPU POWER NVVDD

CONFIG A
VBoot:0.875V
Vmin:0.6V / Vmax:1.2V



	PR56	PR52	PR53	PR54	PR121	PC45
CONFIG	R1	R2	R3	R4	R5	C
N16E-GT						
N16P-GX-B	20K	20K	2K	18K	0	2.7nF

20141029 power modify for GPU power setting
 PR52,PR56: 39K ohm to 20K ohm
 PR53: 1.5K ohm to 2K ohm
 PR54: 30K ohm to 18K ohm
 PR121: 1.5K ohm to 0 ohm
 PC45: 1.5nF to 2.7nF

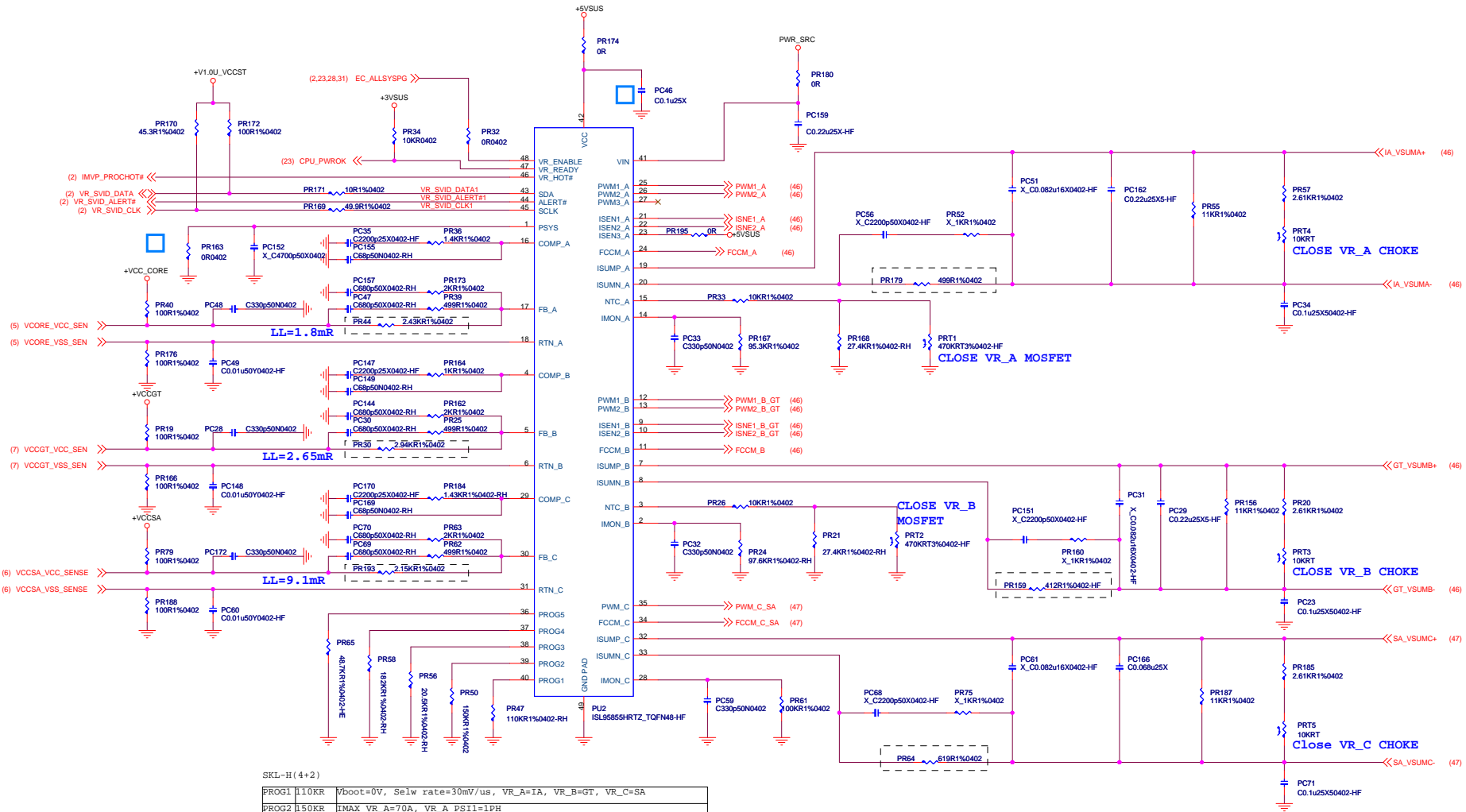
msi MICRO-STAR INT'L CO.,LTD.

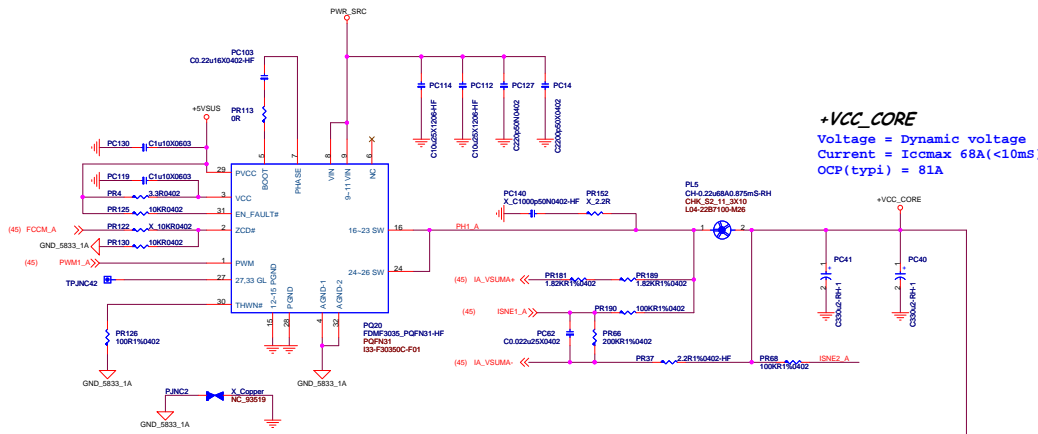
Title: **DGPU POWER NVVDD**

Size: **MS-16J5** Document Number: **MS-16J5** Rev: **0A**

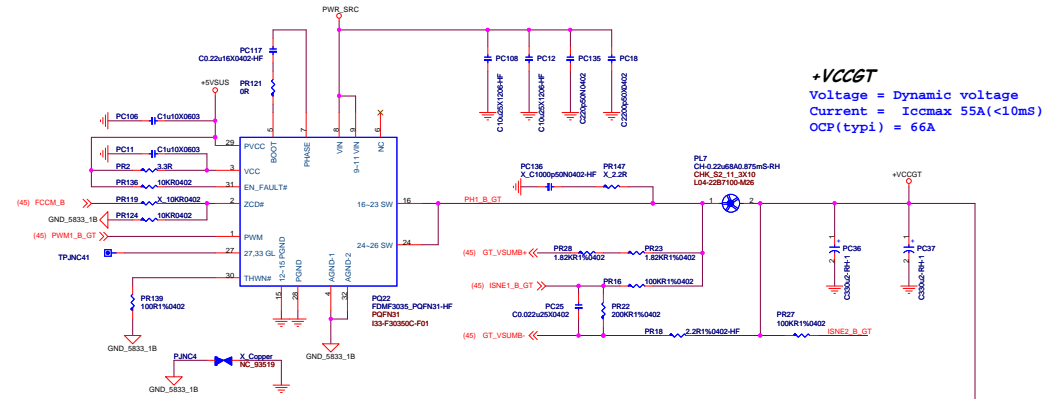
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Skylake H-line 42 45W ISL95855

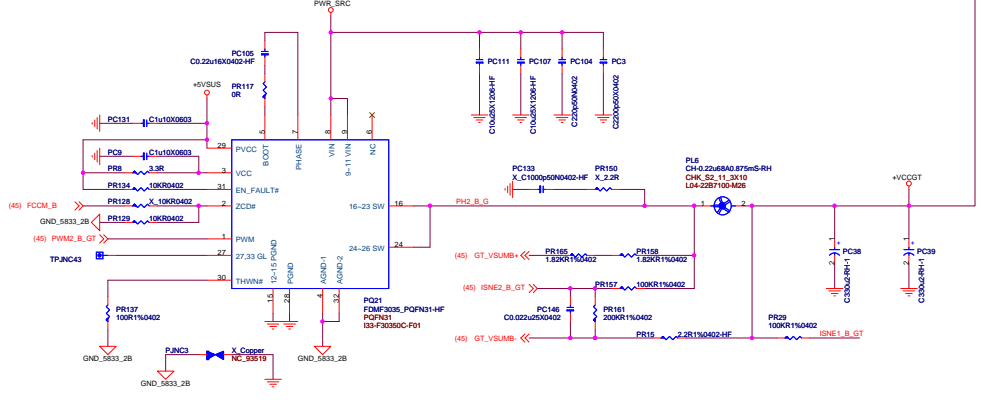
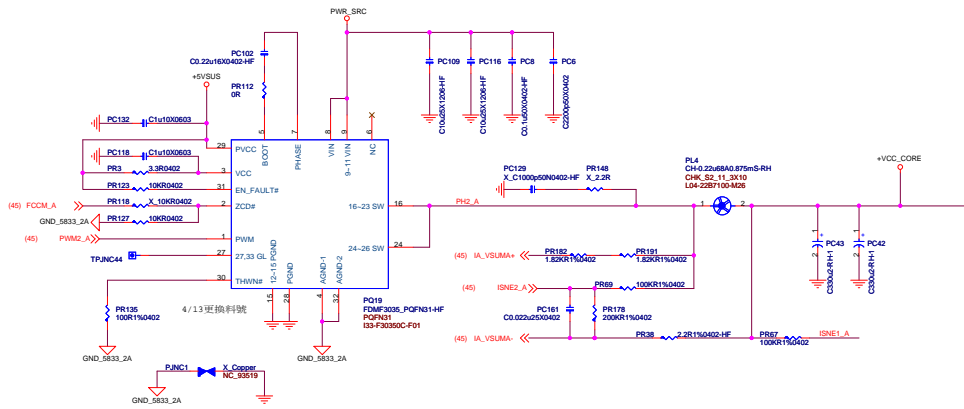




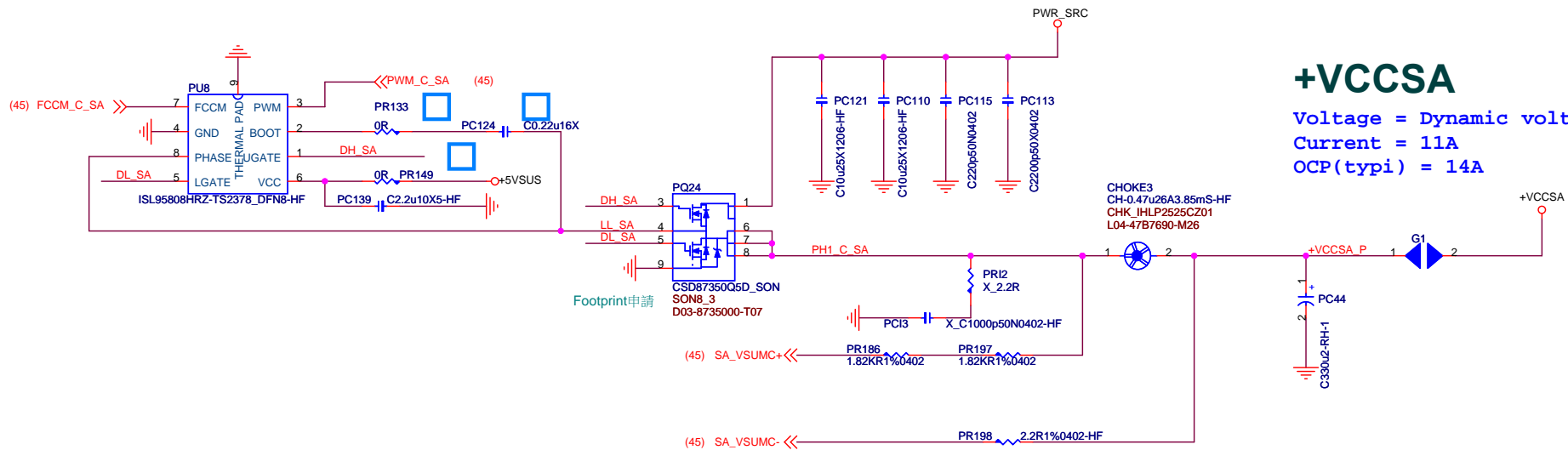
+VCC_CORE
 Voltage = Dynamic voltage
 Current = Iccmax 68A(<10ms)
 OCP(typi) = 81A



+VCCGT
 Voltage = Dynamic voltage
 Current = Iccmax 55A(<10ms)
 OCP(typi) = 66A

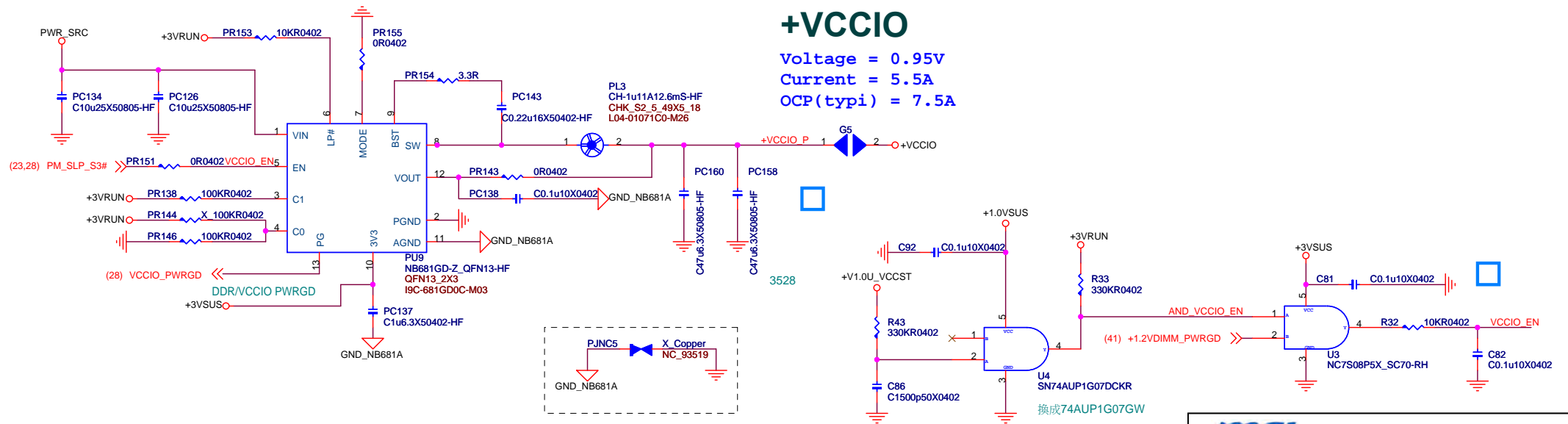


msi MICRO-STAR INT'L CO.,LTD.	
Title SkyLake VCore/VCCGT	
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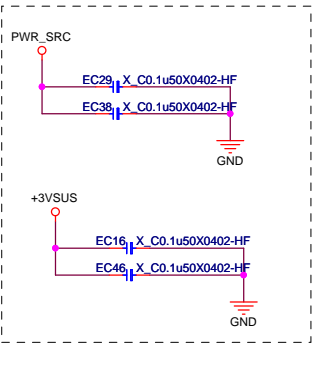
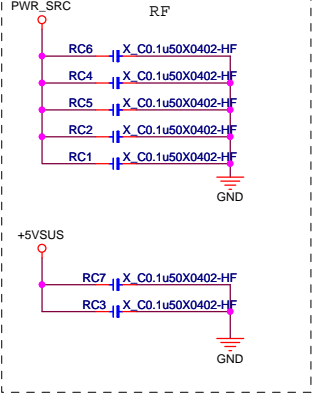
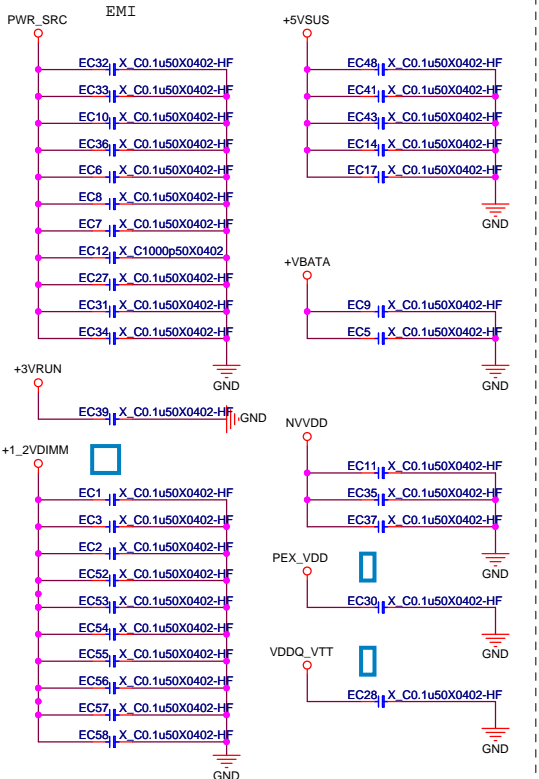


+VCCSA
 Voltage = Dynamic voltage
 Current = 11A
 OCP(typi) = 14A

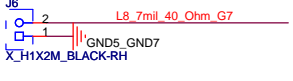
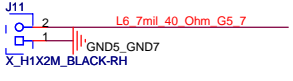
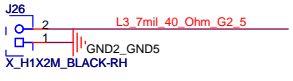
+VCCIO
 Voltage = 0.95V
 Current = 5.5A
 OCP(typi) = 7.5A



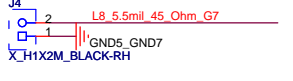
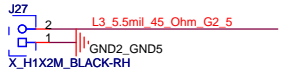
msi MICRO-STAR INT'L CO.,LTD.	
Title Skylake VCCSA/VCCIO	
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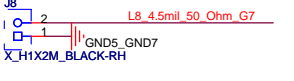
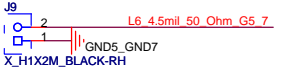
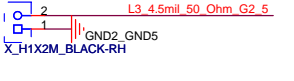
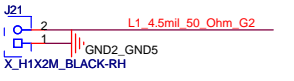
40 OHM DDR4 CMD/ DDR4 CTRL



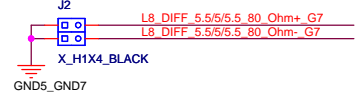
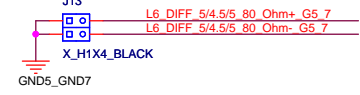
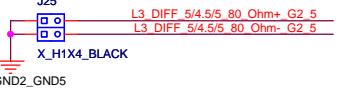
45 OHM GDDR5 CMD/DQ/DBI/EDC



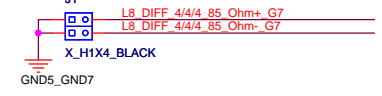
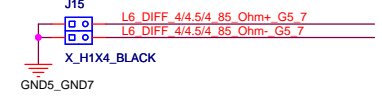
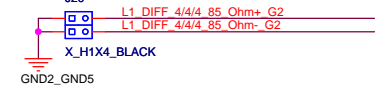
50 OHM / DDR4 DQ



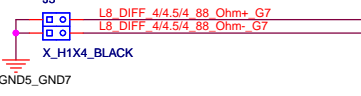
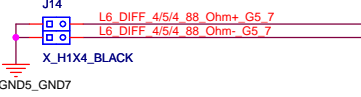
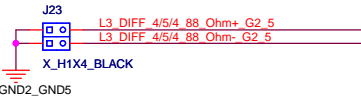
80 OHM GDDR5 (CK/WCK)



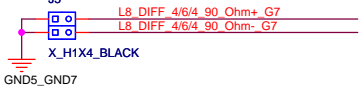
85 OHM /SATA /PCIE/ EDP /USB /DMI /HDMI /DP/CLK



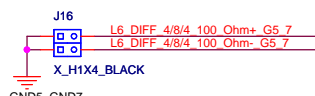
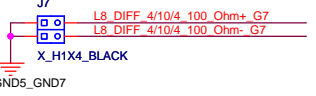
88 OHM / DDR4 (DQS/CLK)



90 OHM / XTAL(GPU)



100 OHM / LAN /HDMI (After DP139)

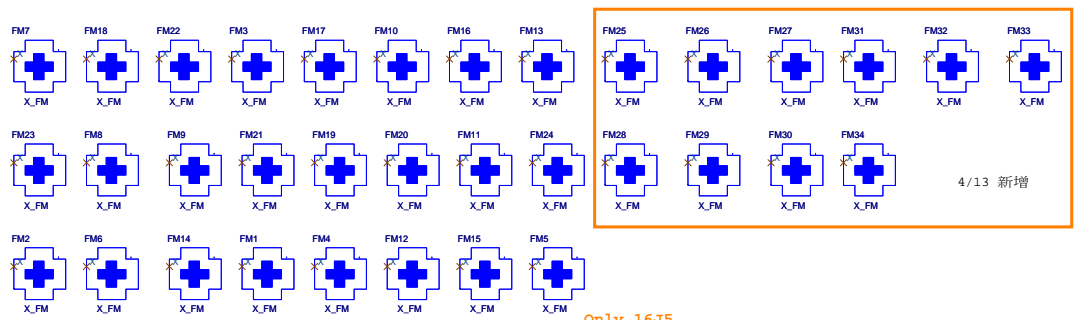
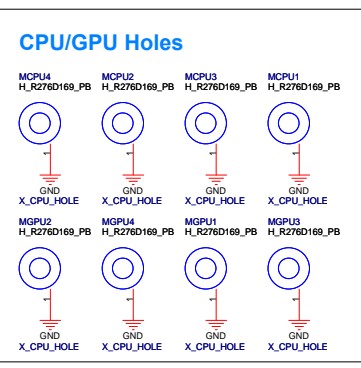


msi MICRO-STAR INT'L CO.,LTD.

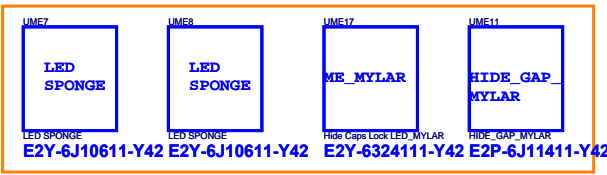
Title: **EMI / Impedance**

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Only 16J5



Only 1795

