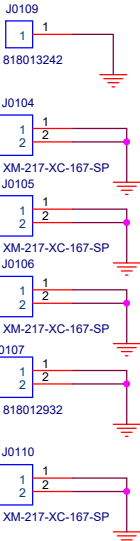
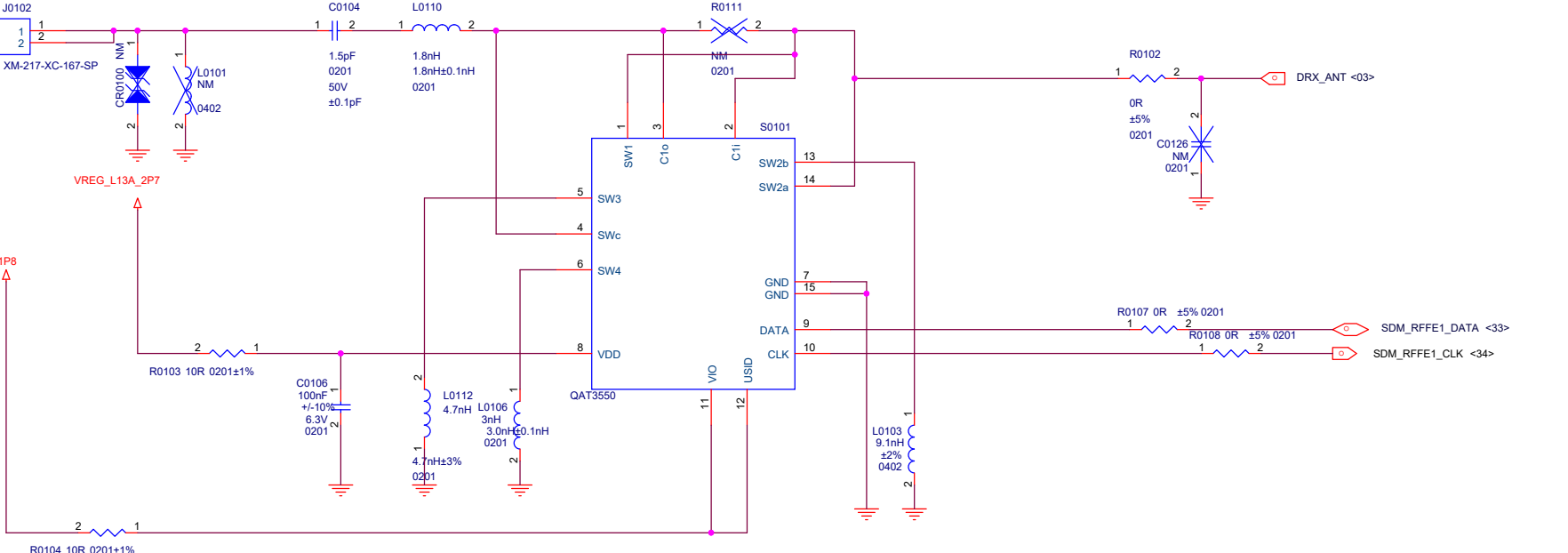
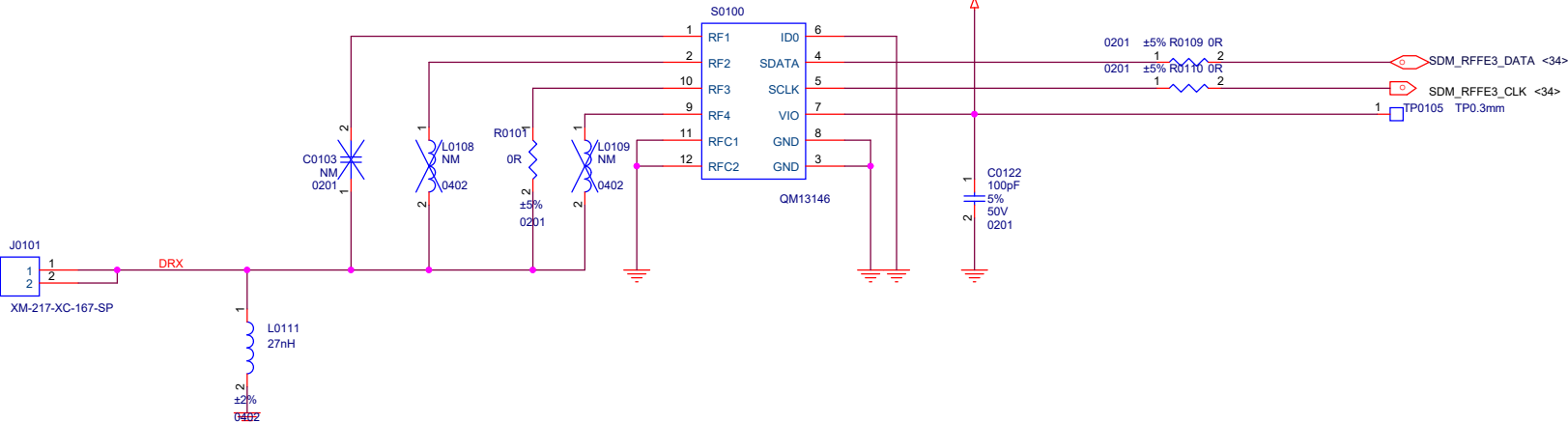
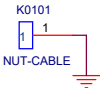
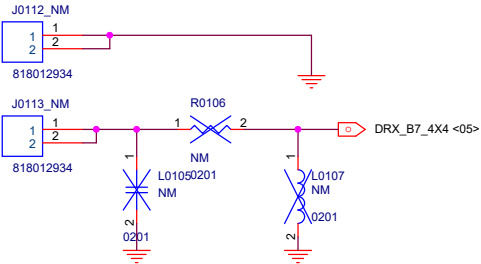
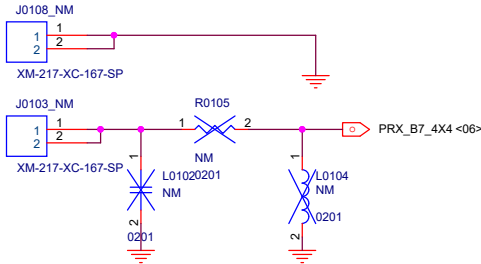


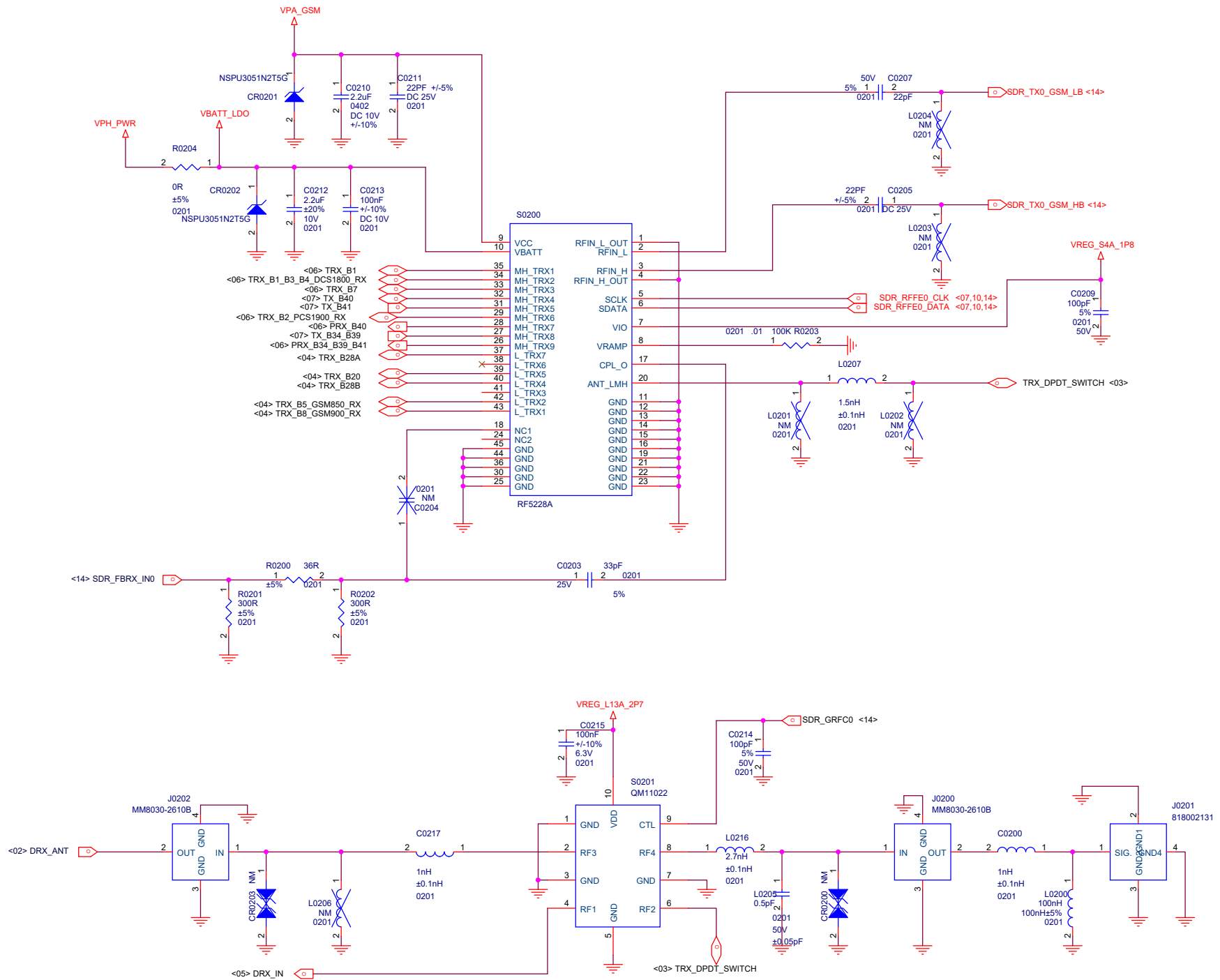
DRX\_ANT

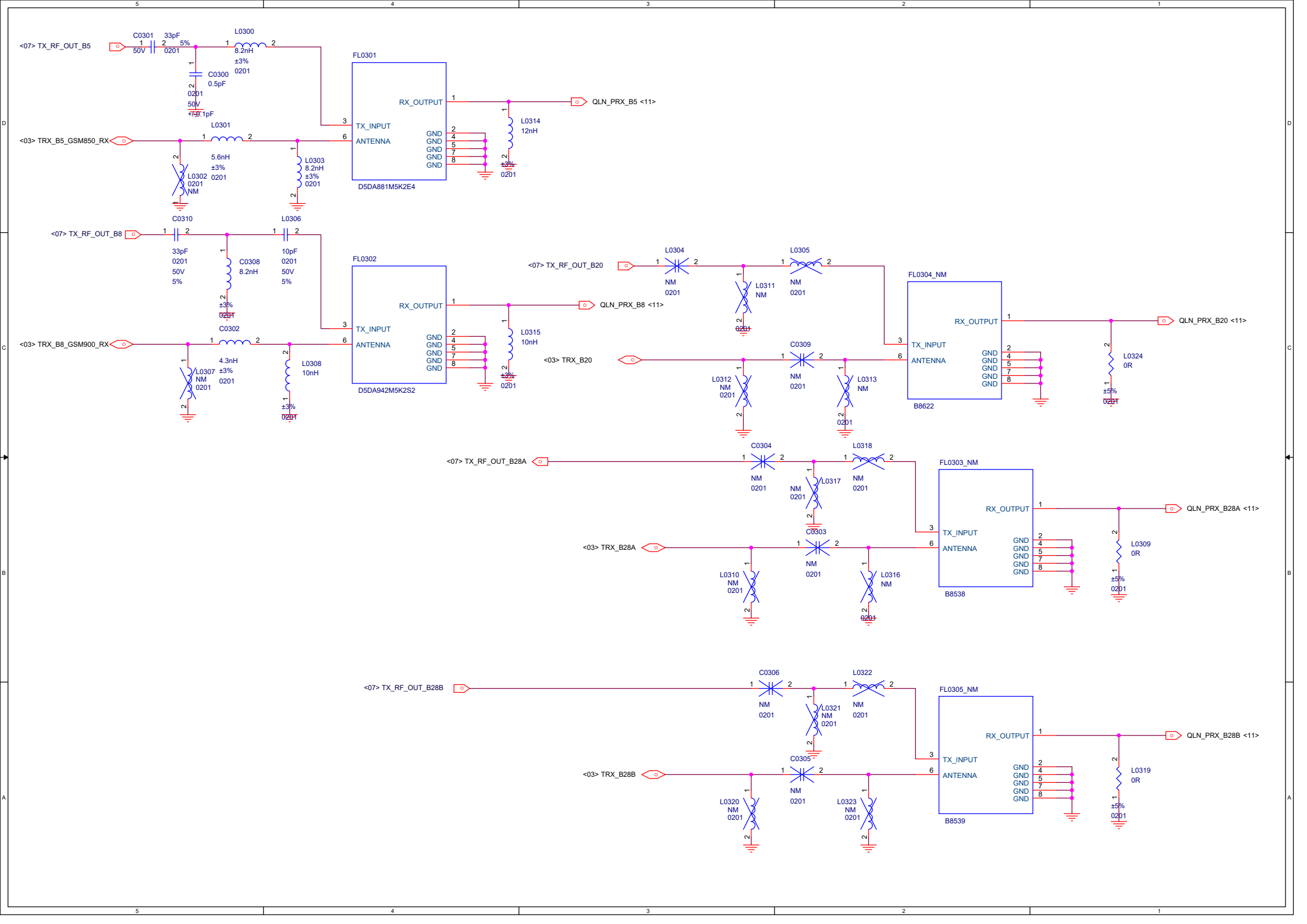


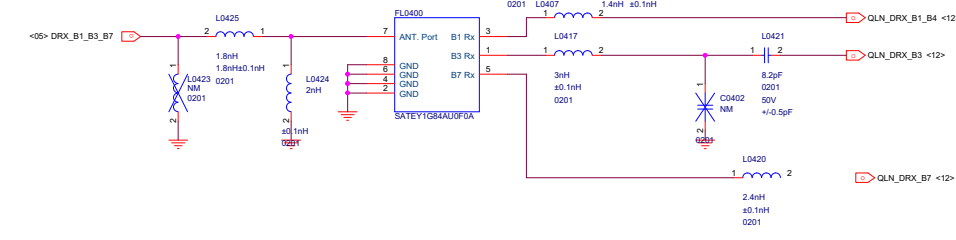
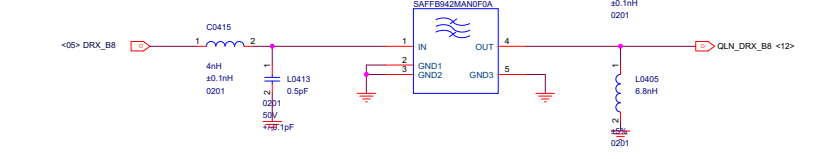
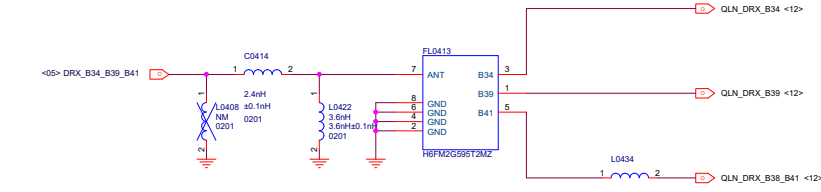
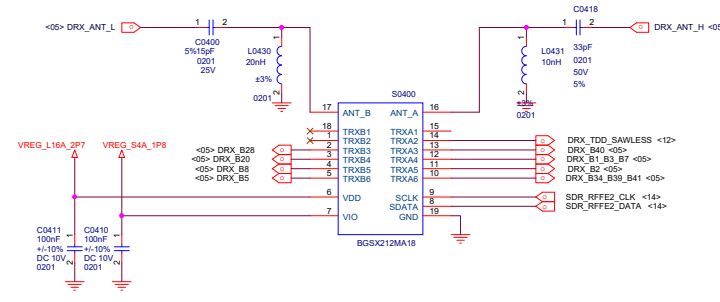
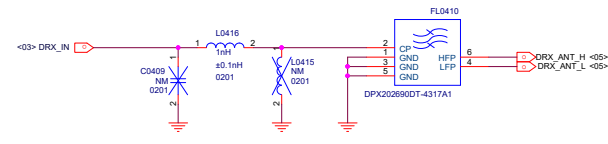
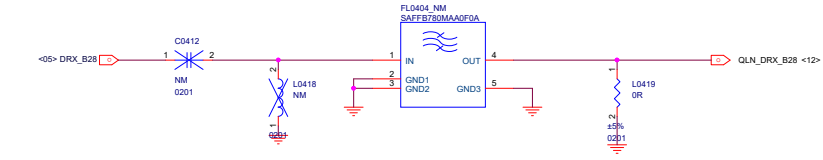
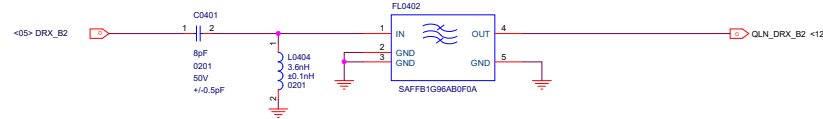
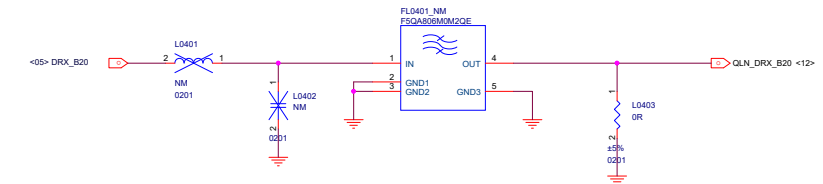
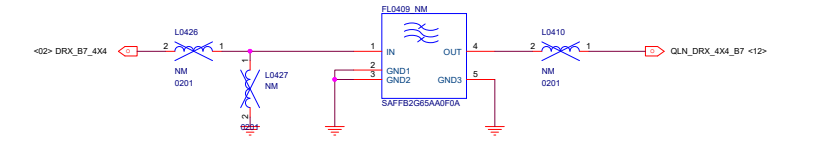
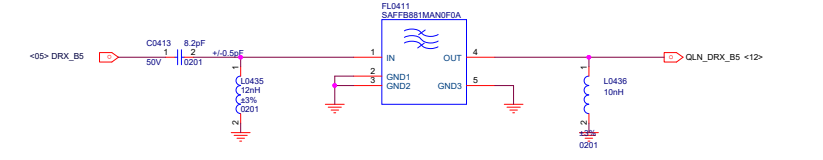
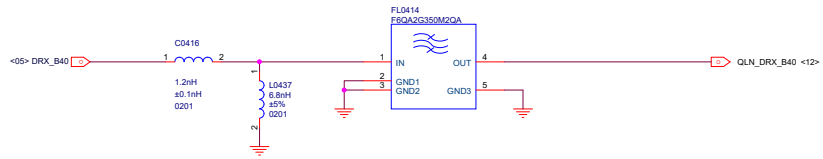
4X4\_MIMO\_ANT3

4X4\_MIMO\_ANT4

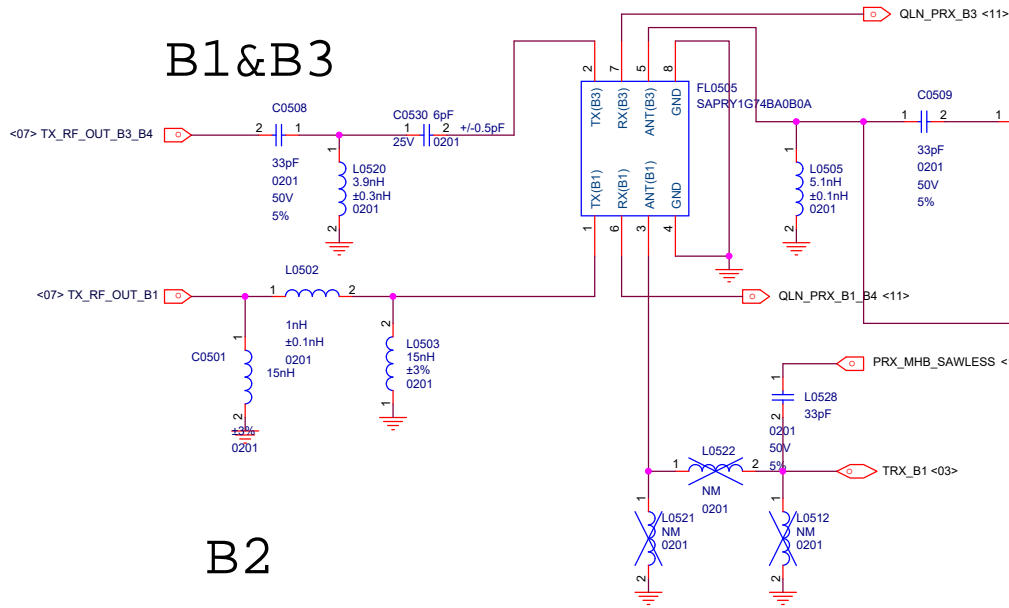




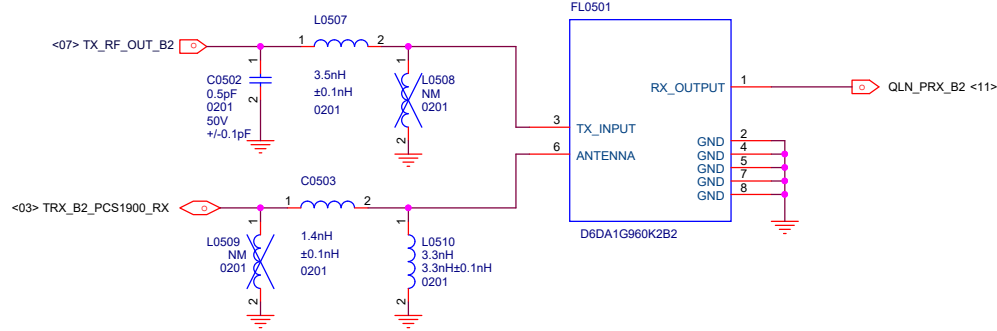




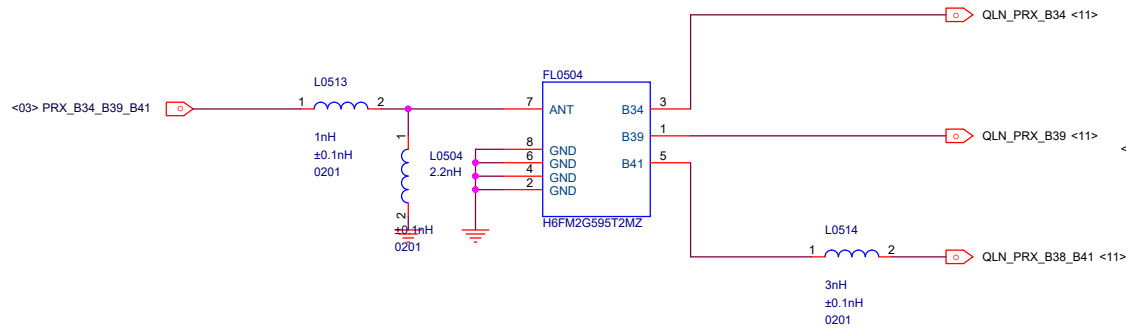
# B1&B3



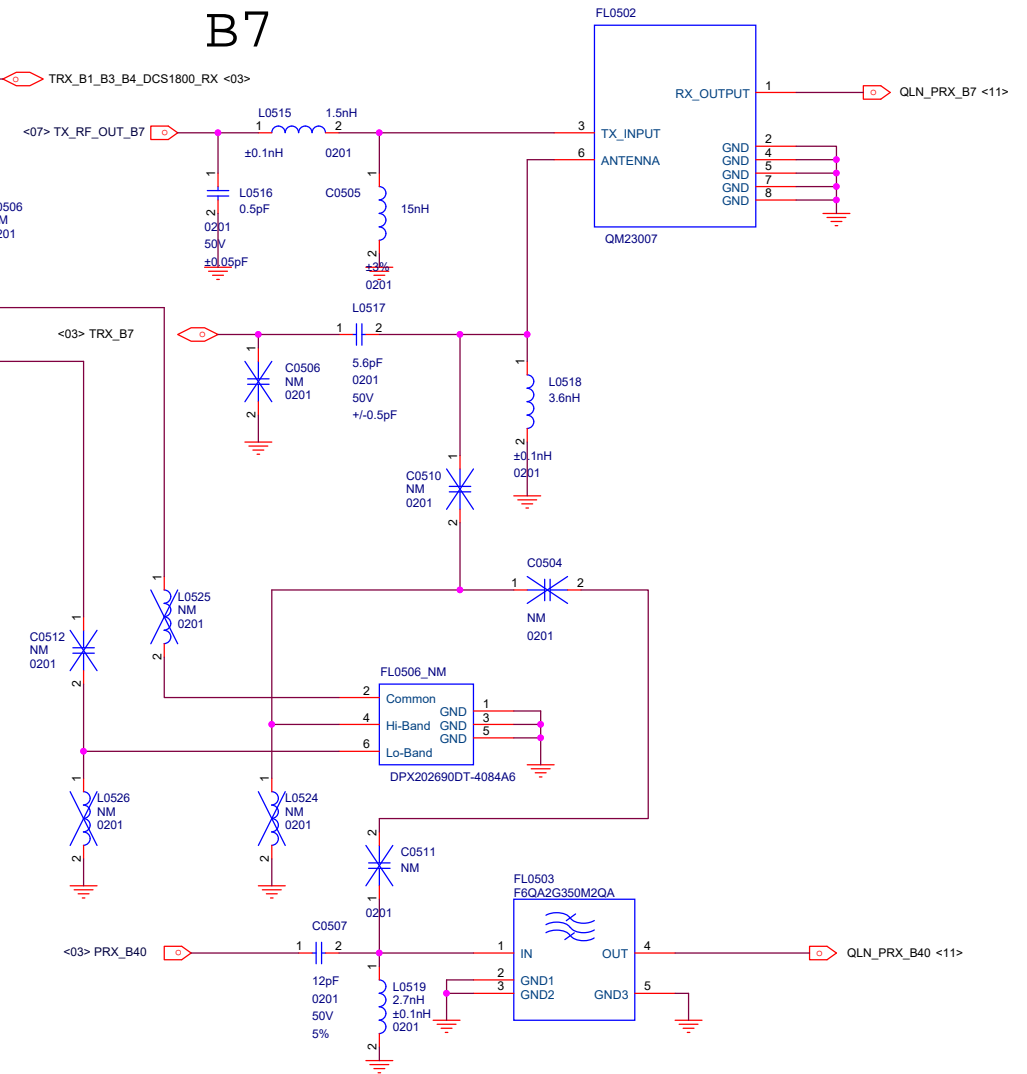
# B2



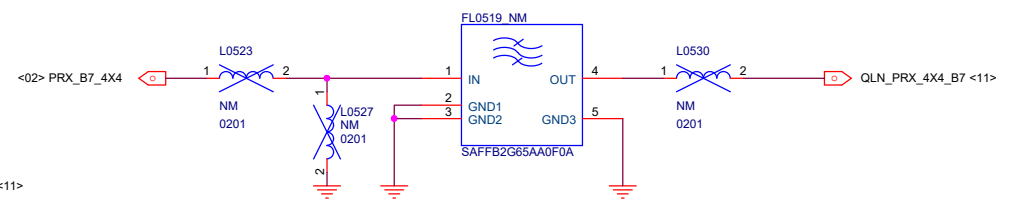
# PRX B34\_B39\_B41



# B7



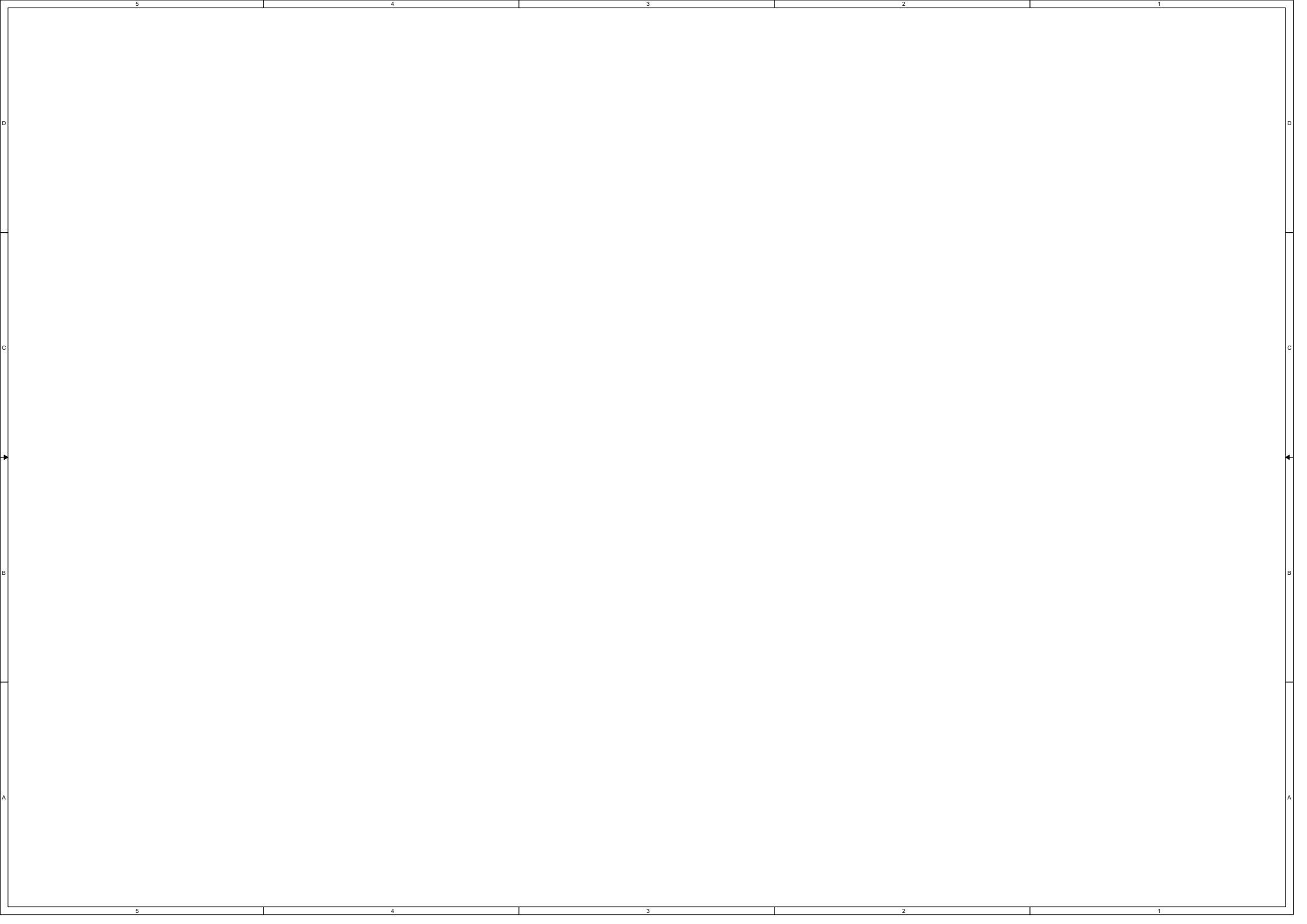
# PRX MIMO B7

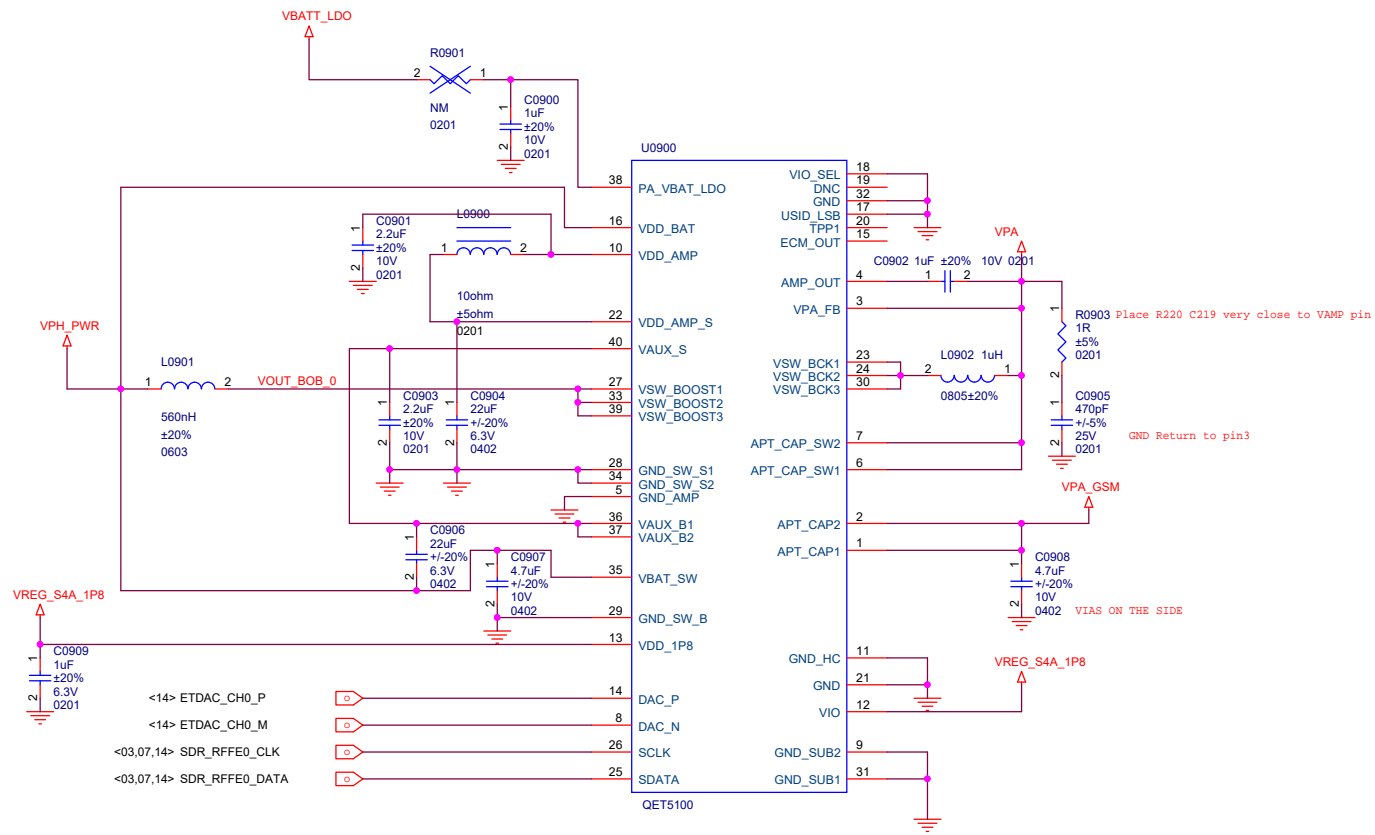


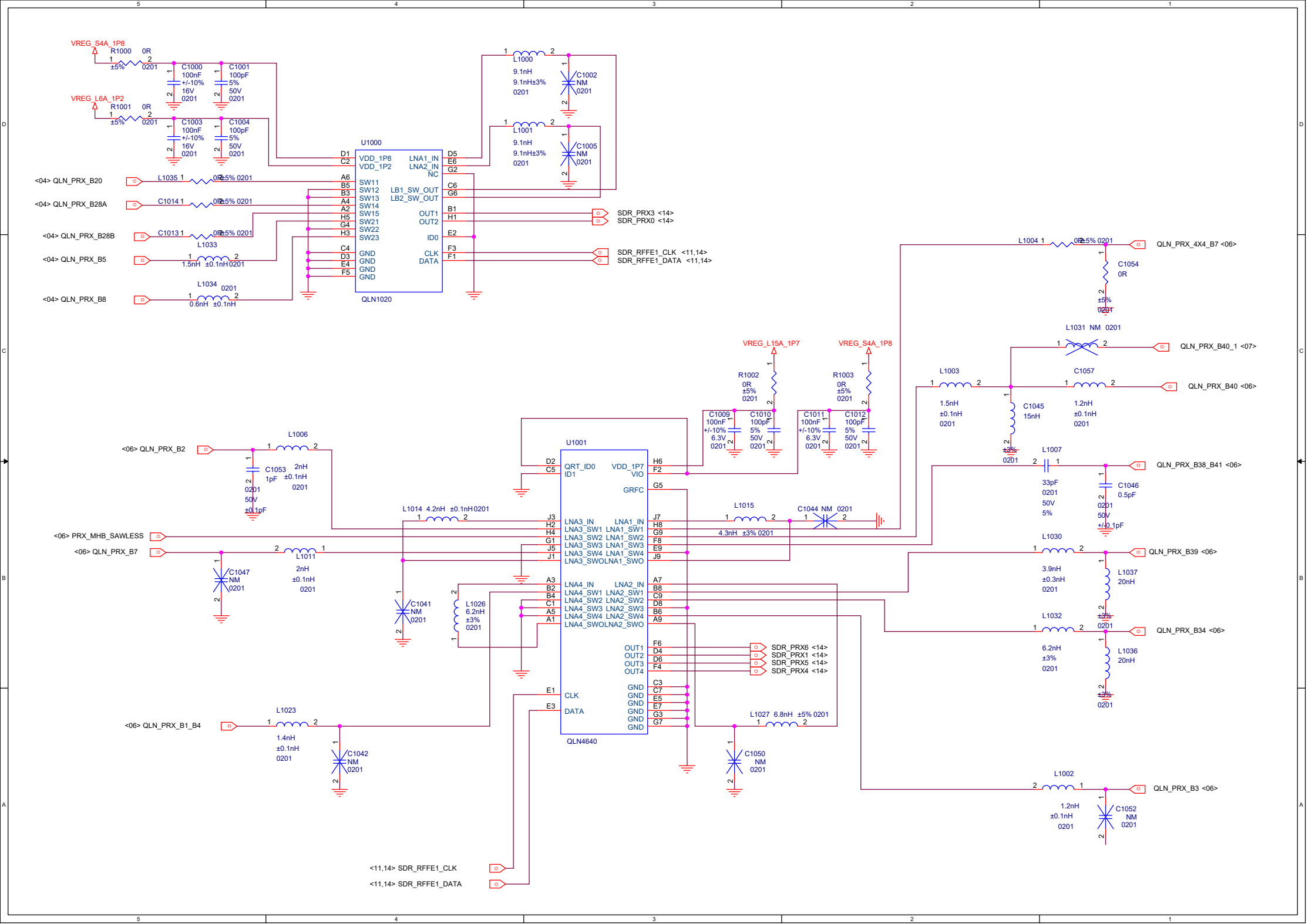


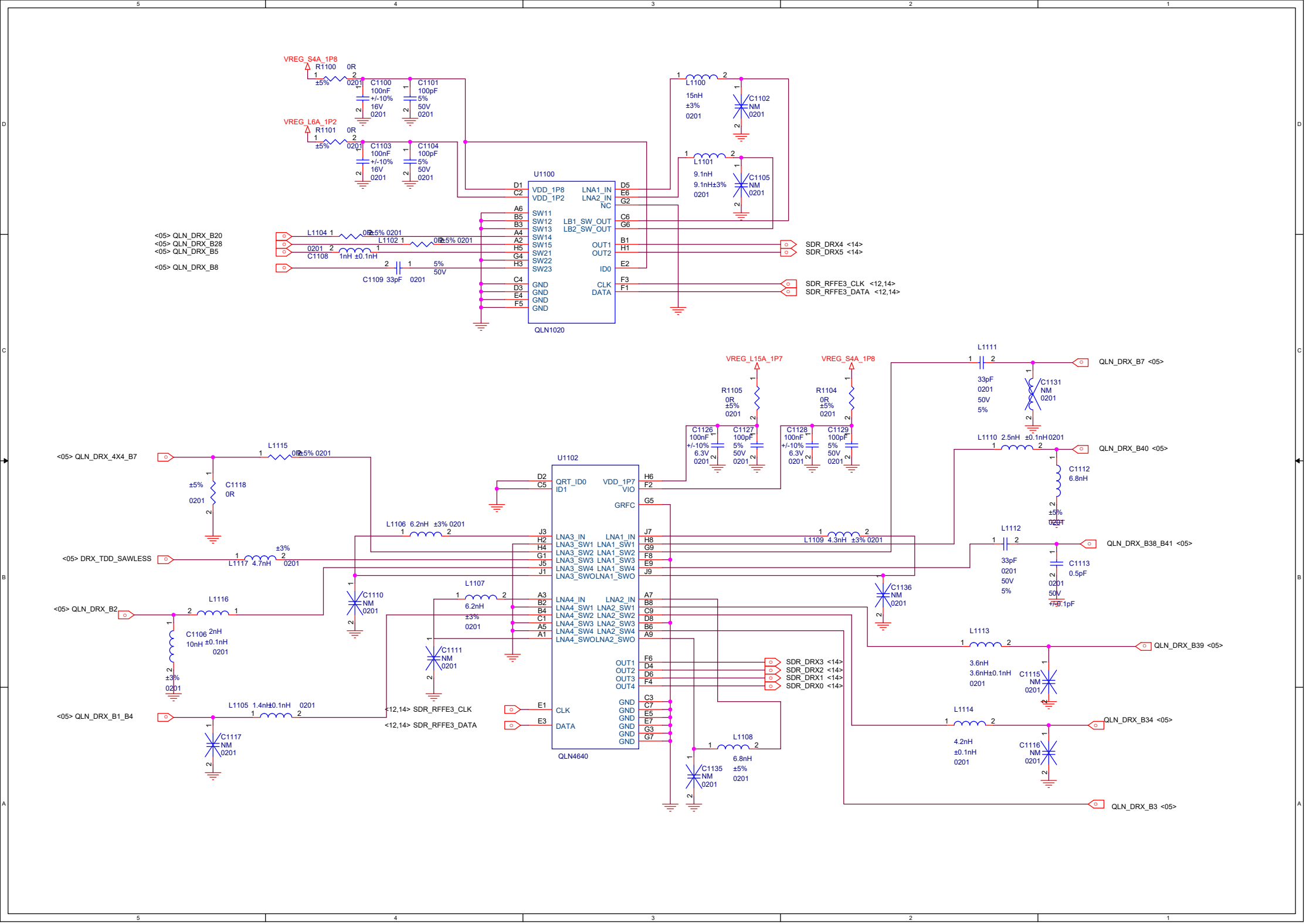


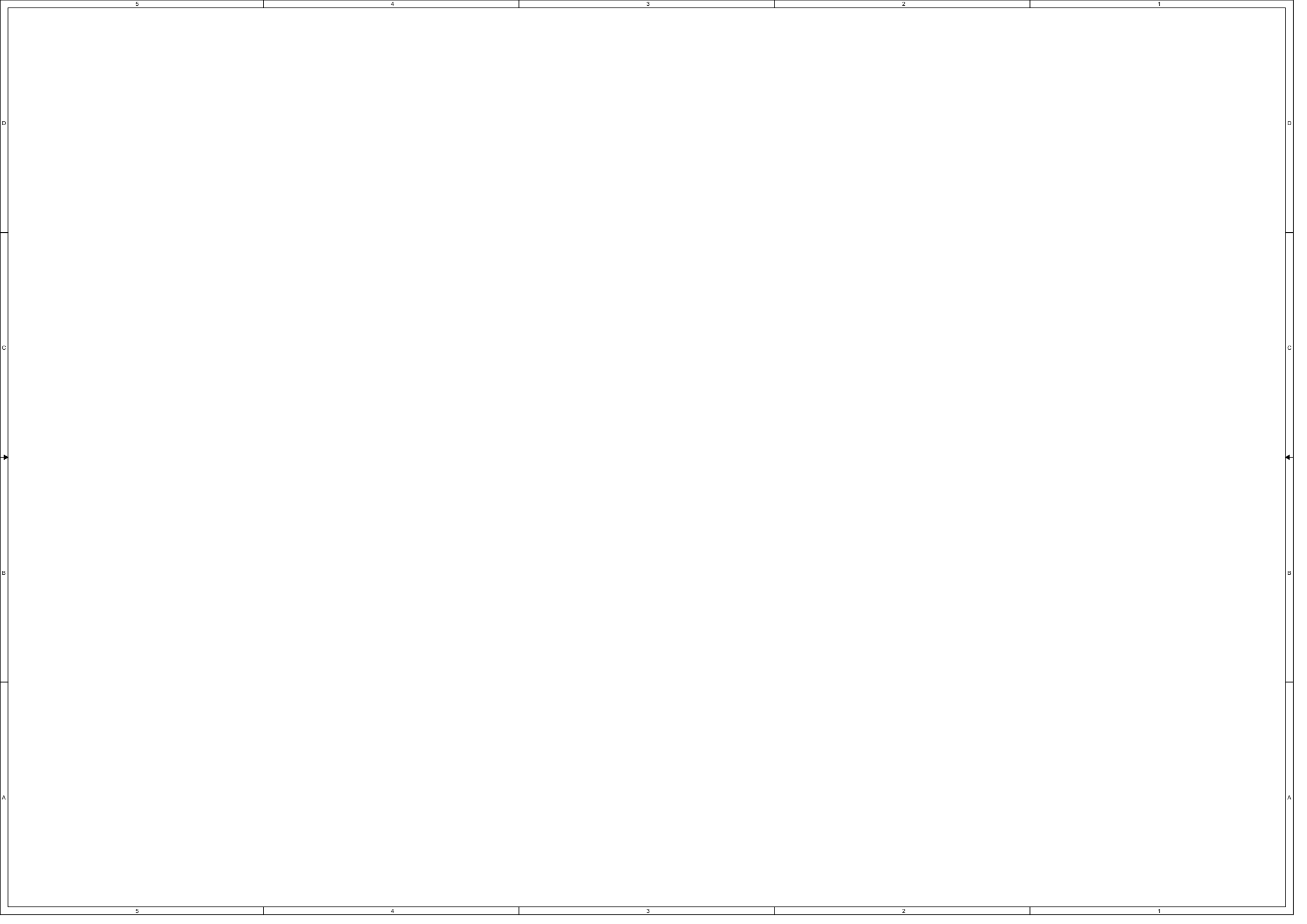


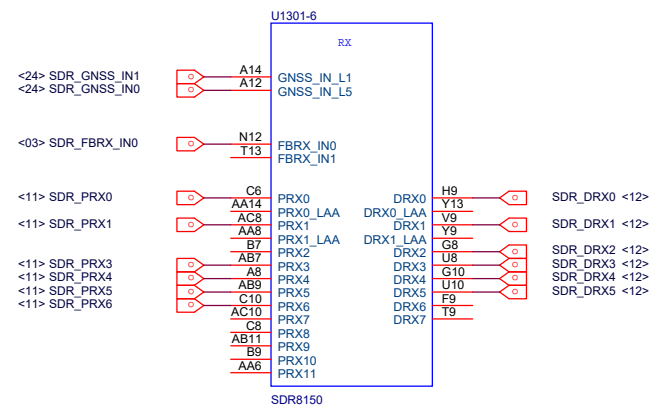
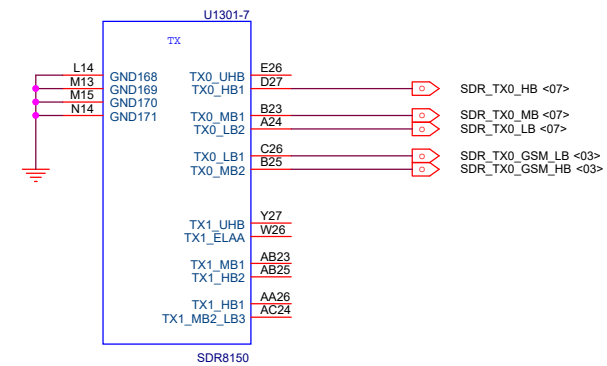
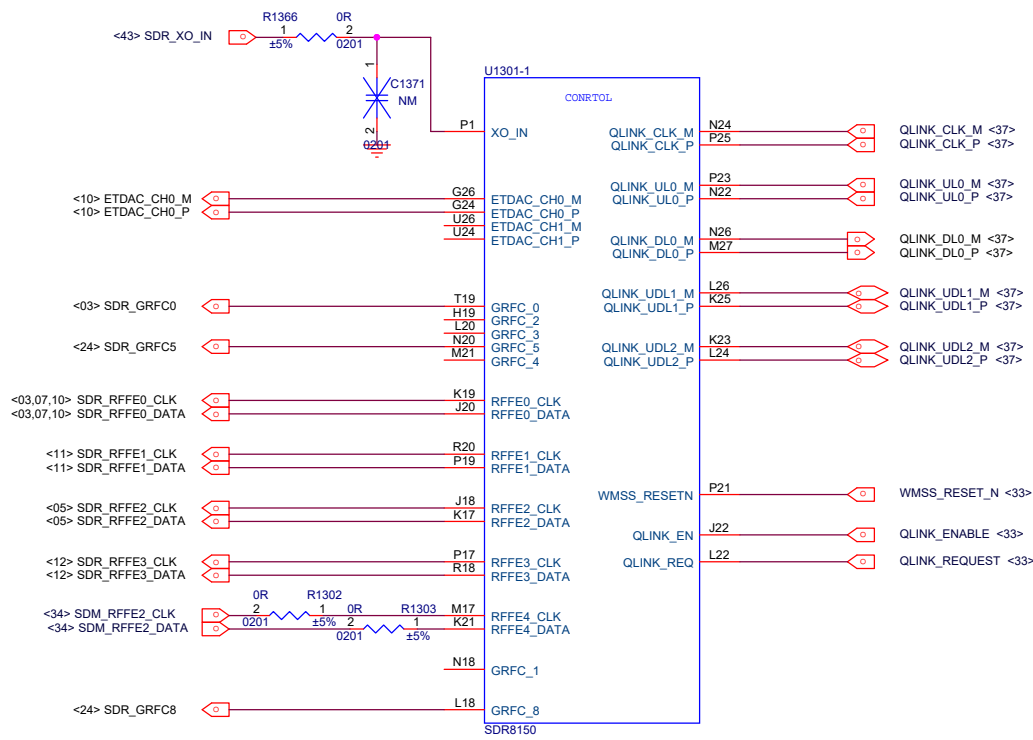


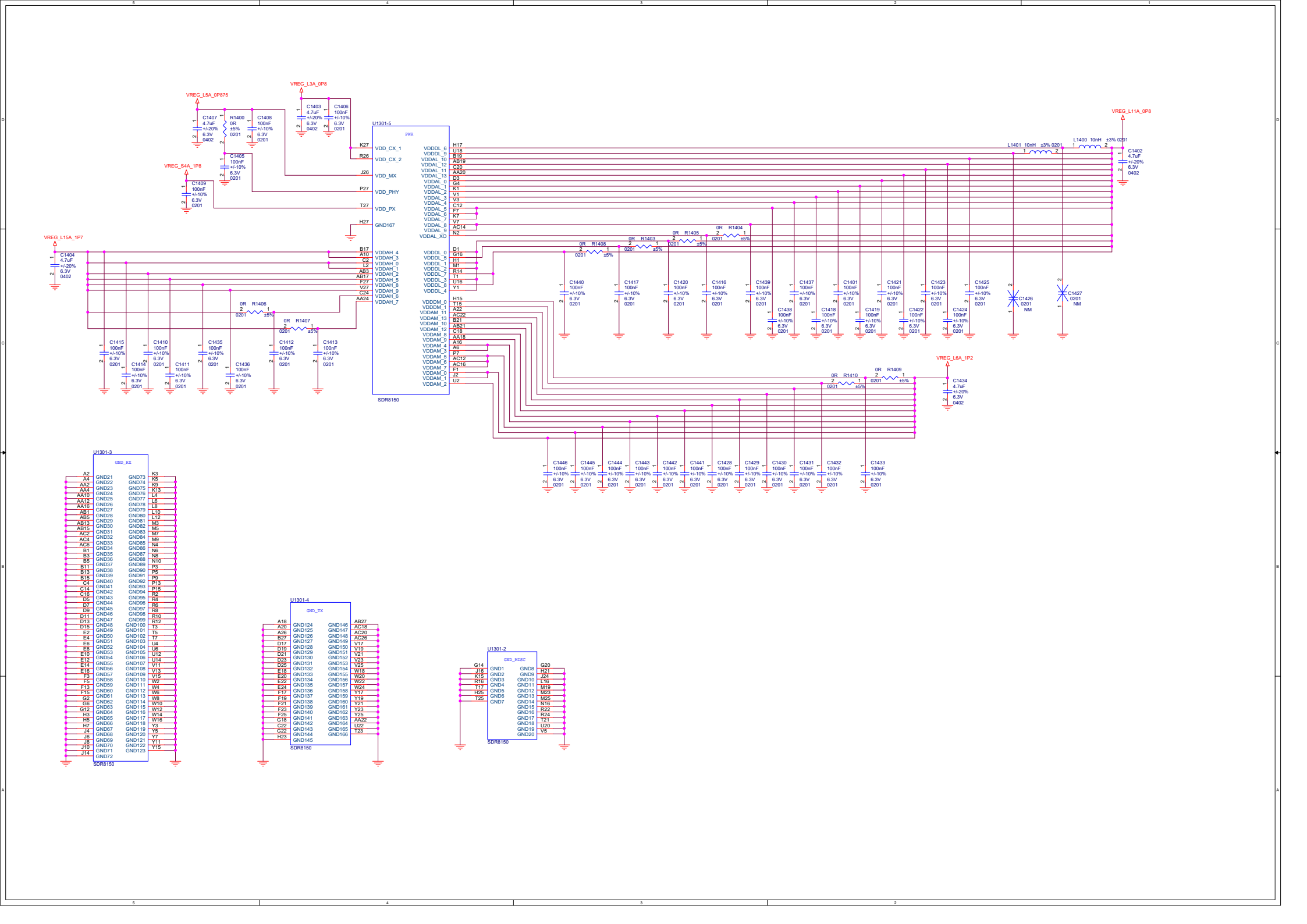


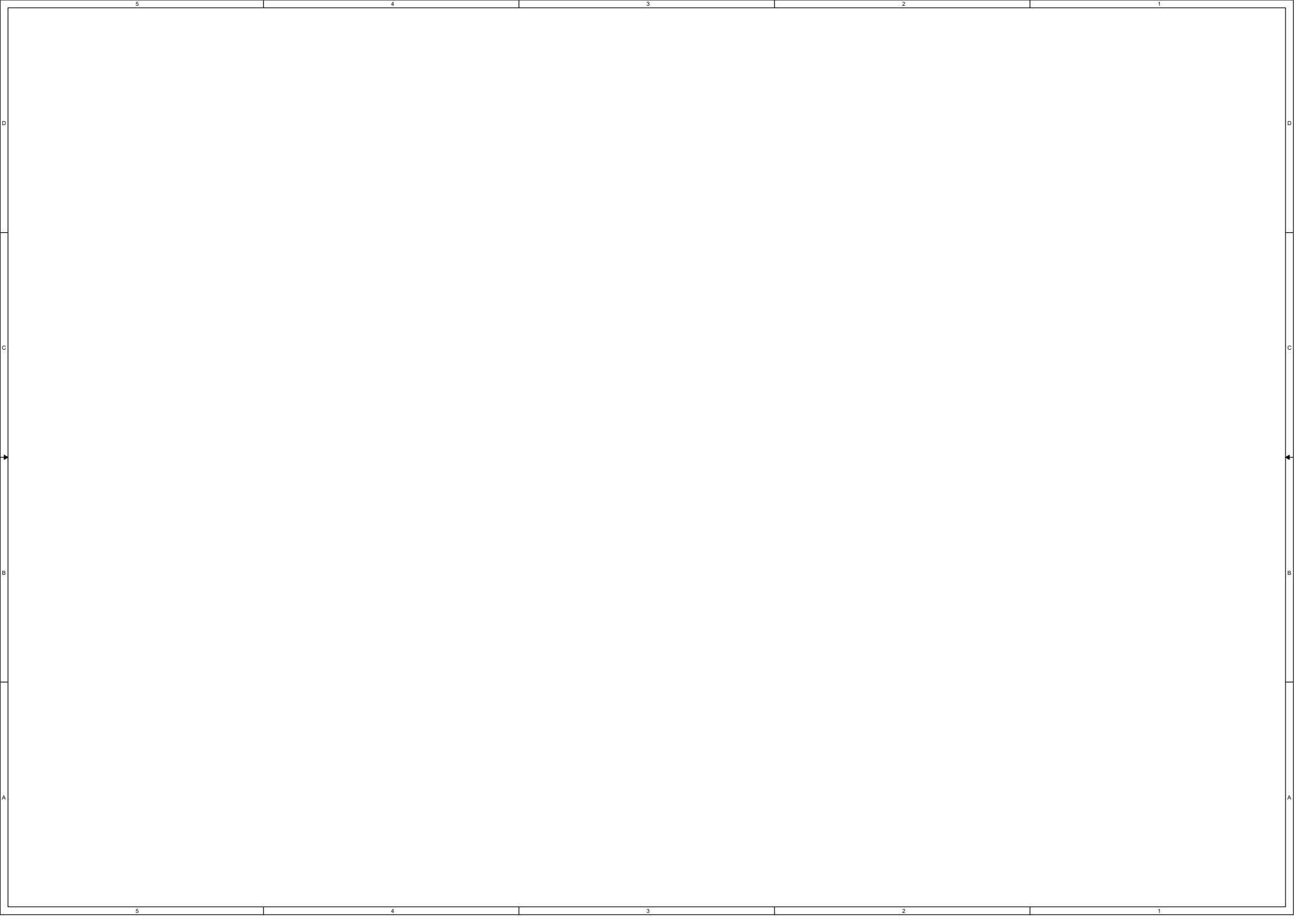




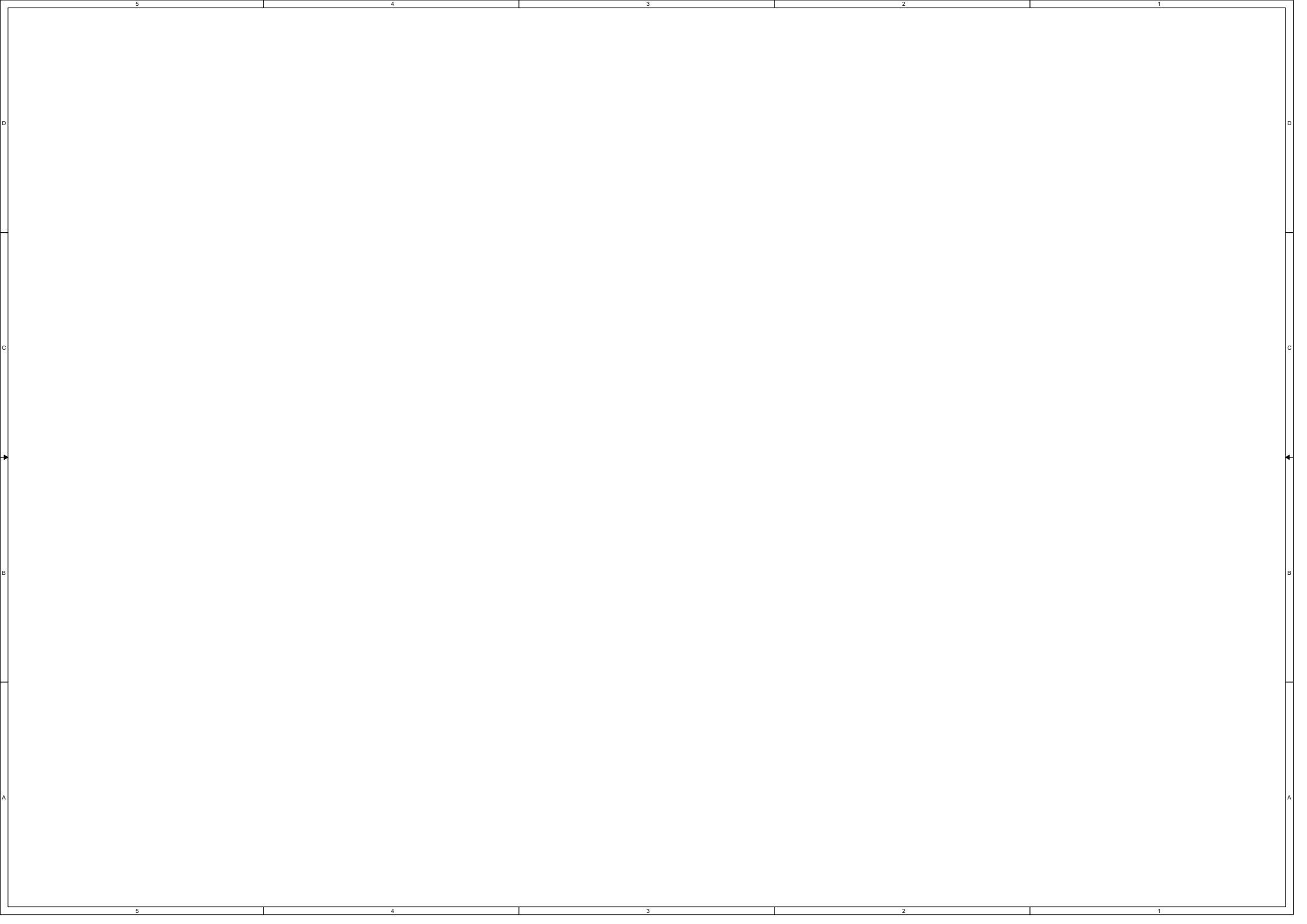


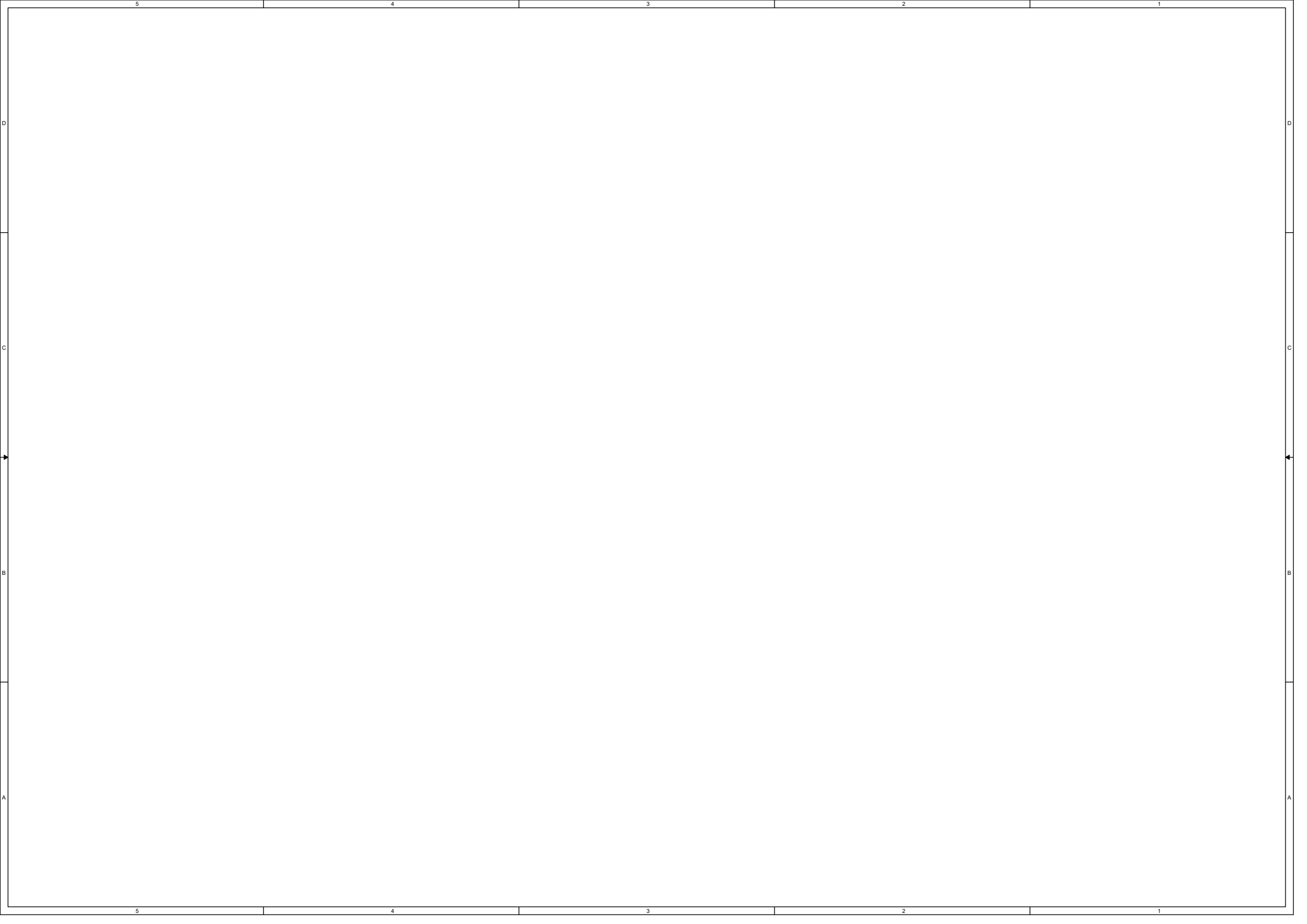


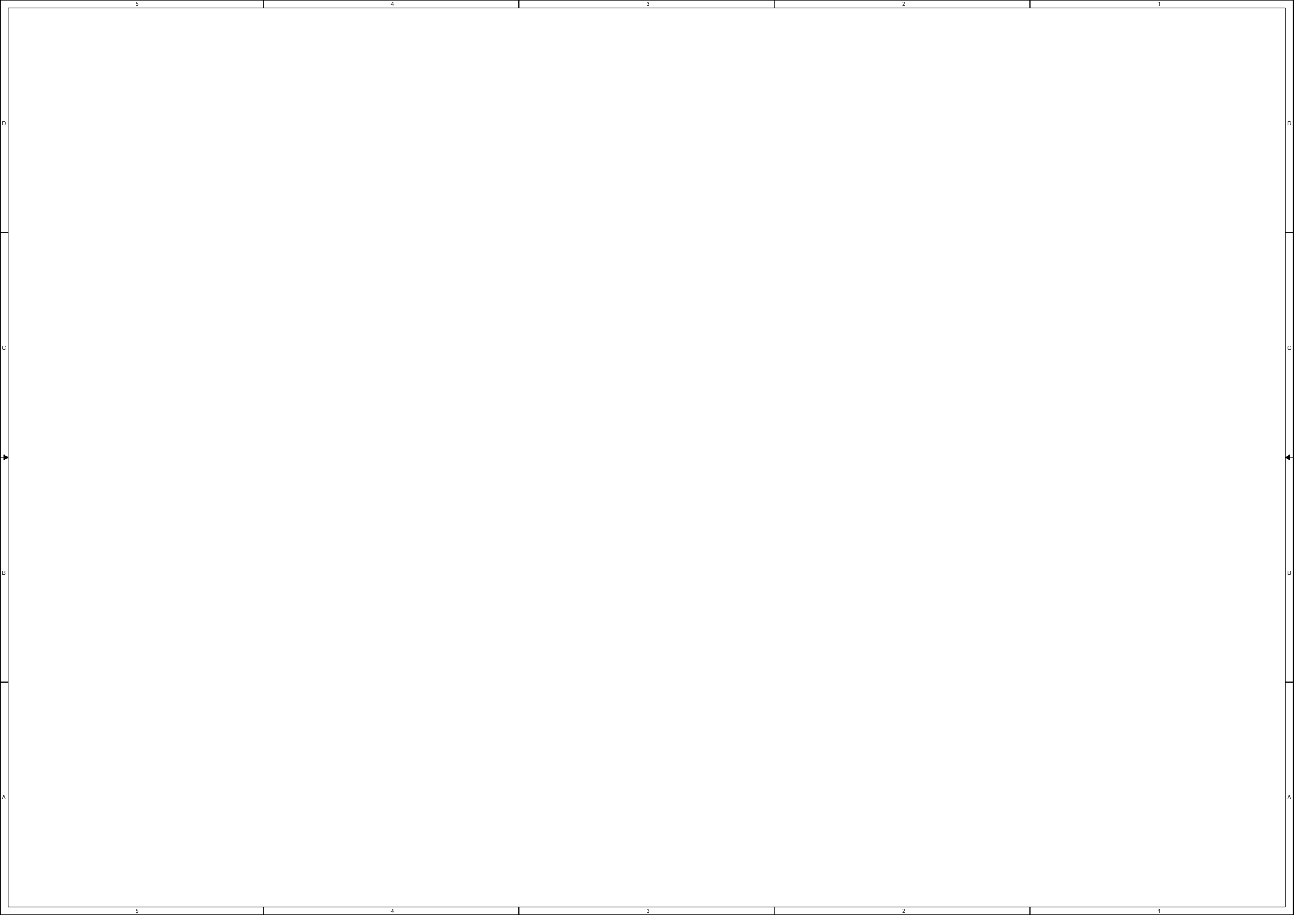


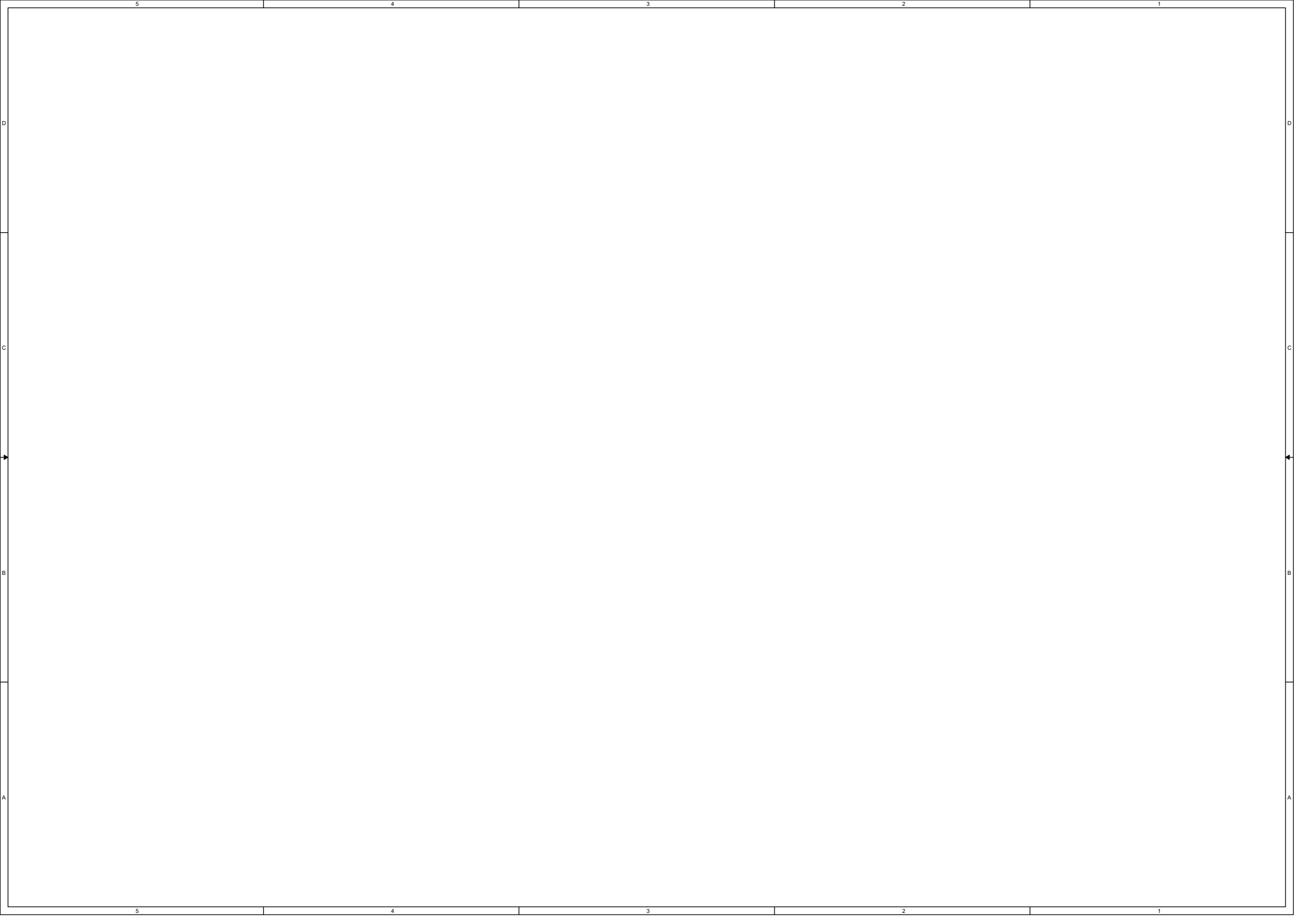


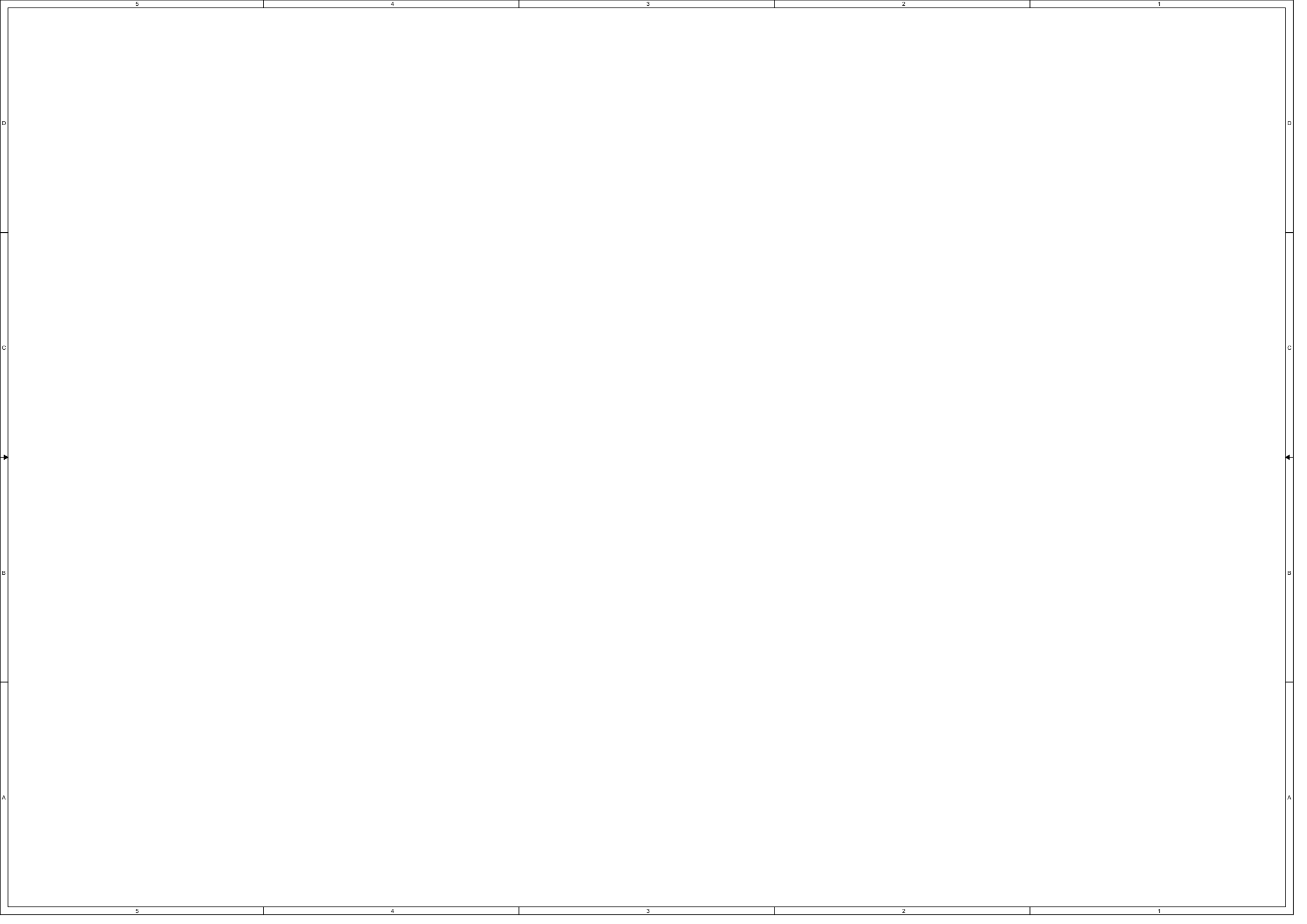


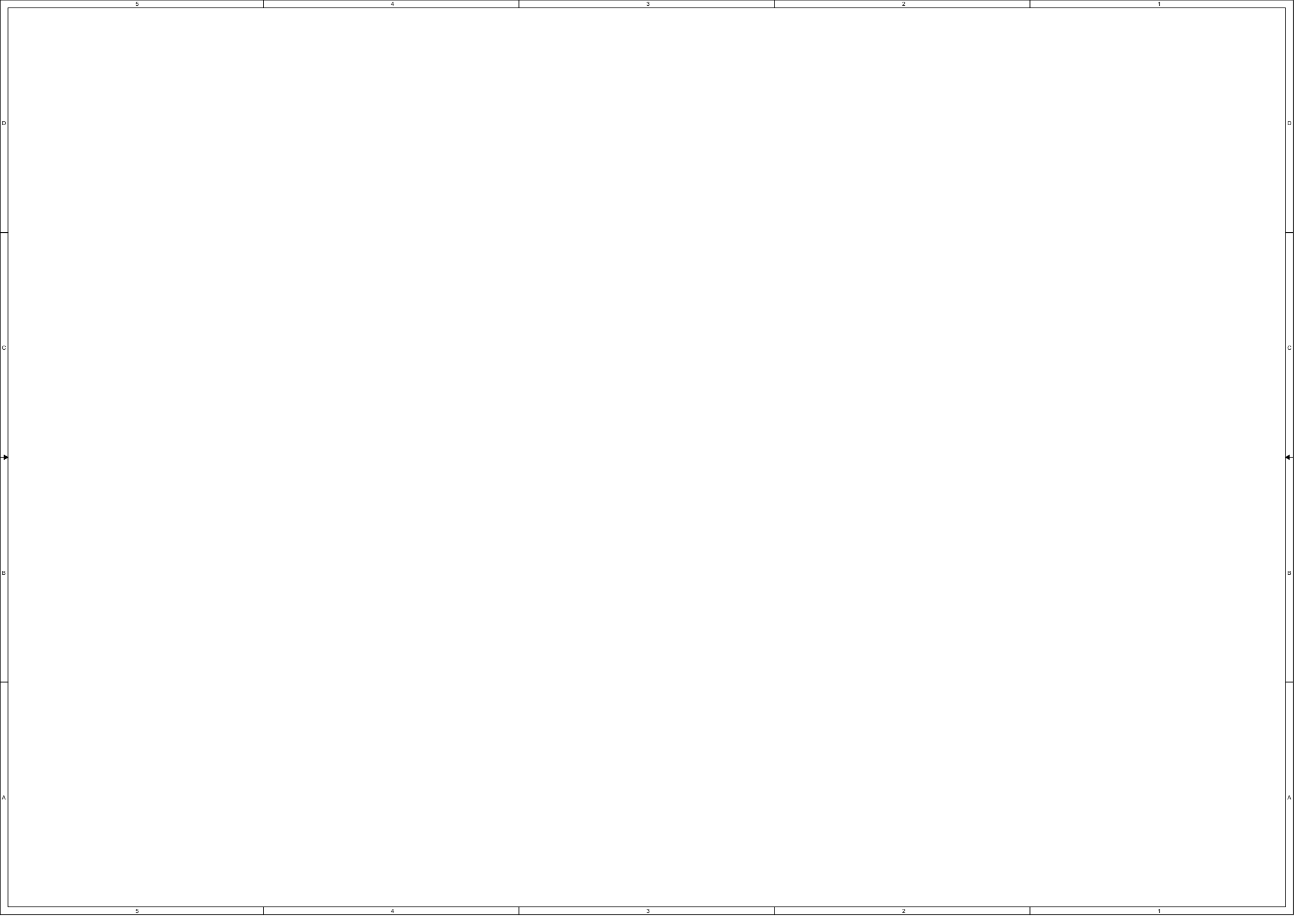




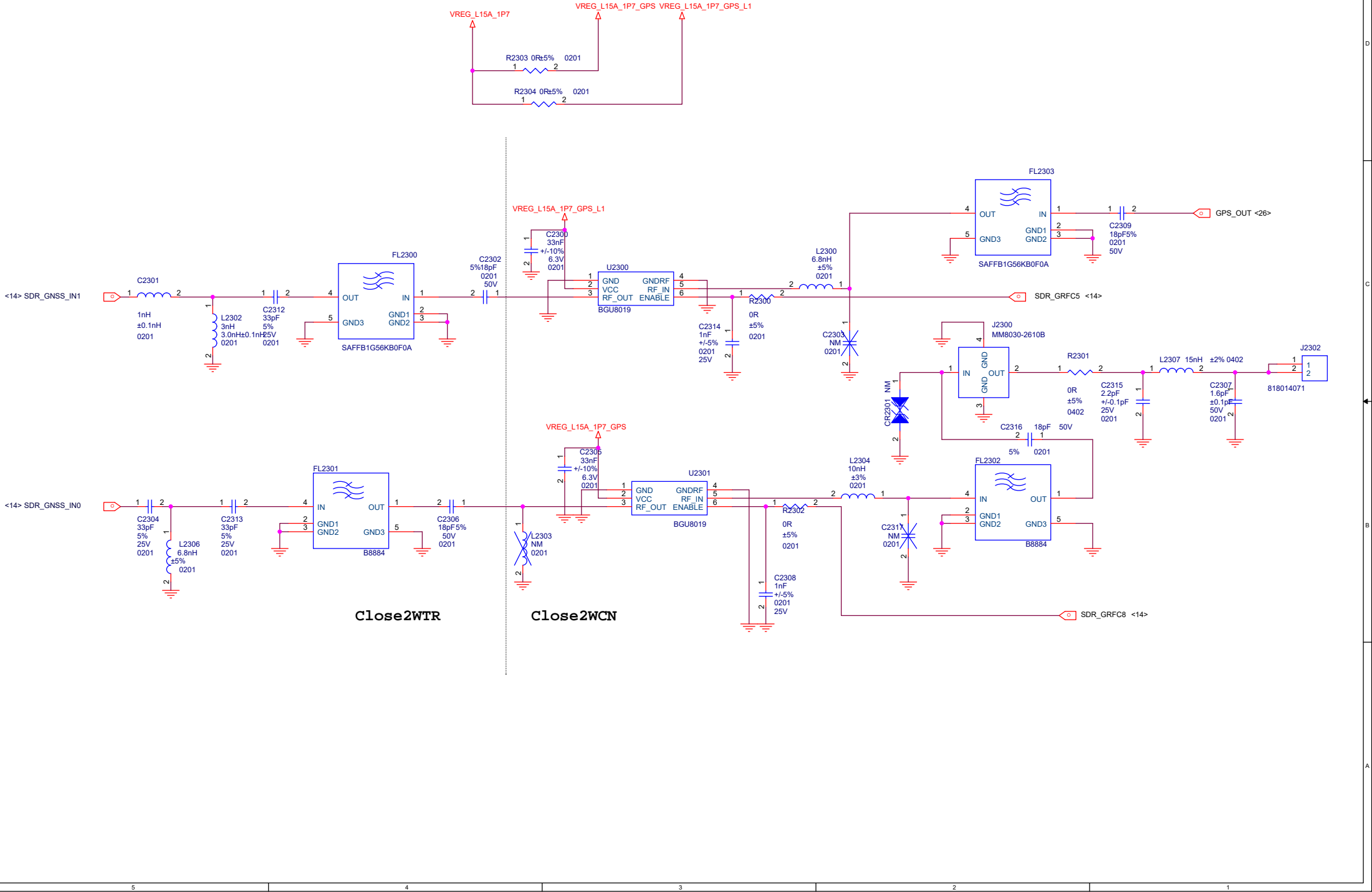




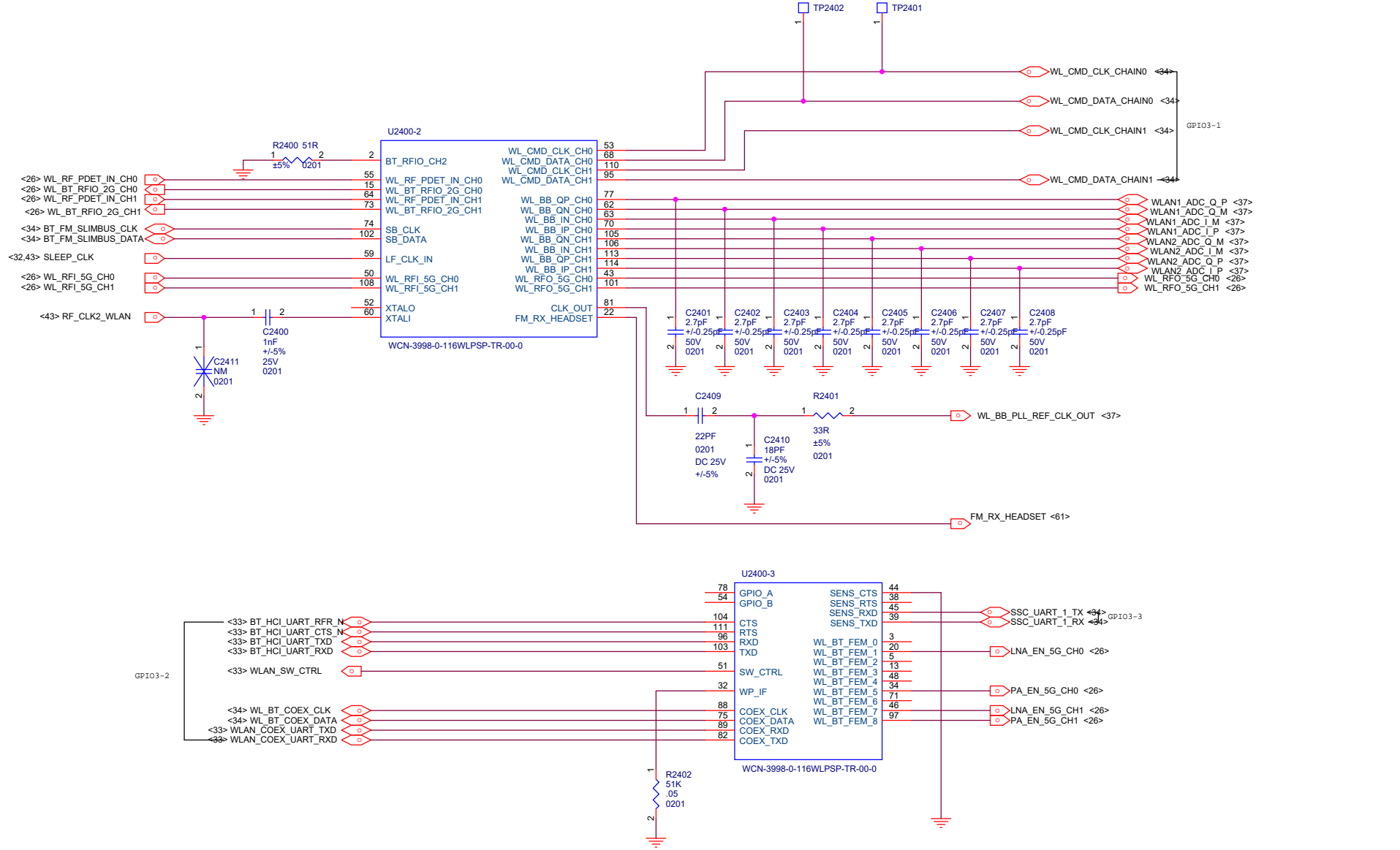


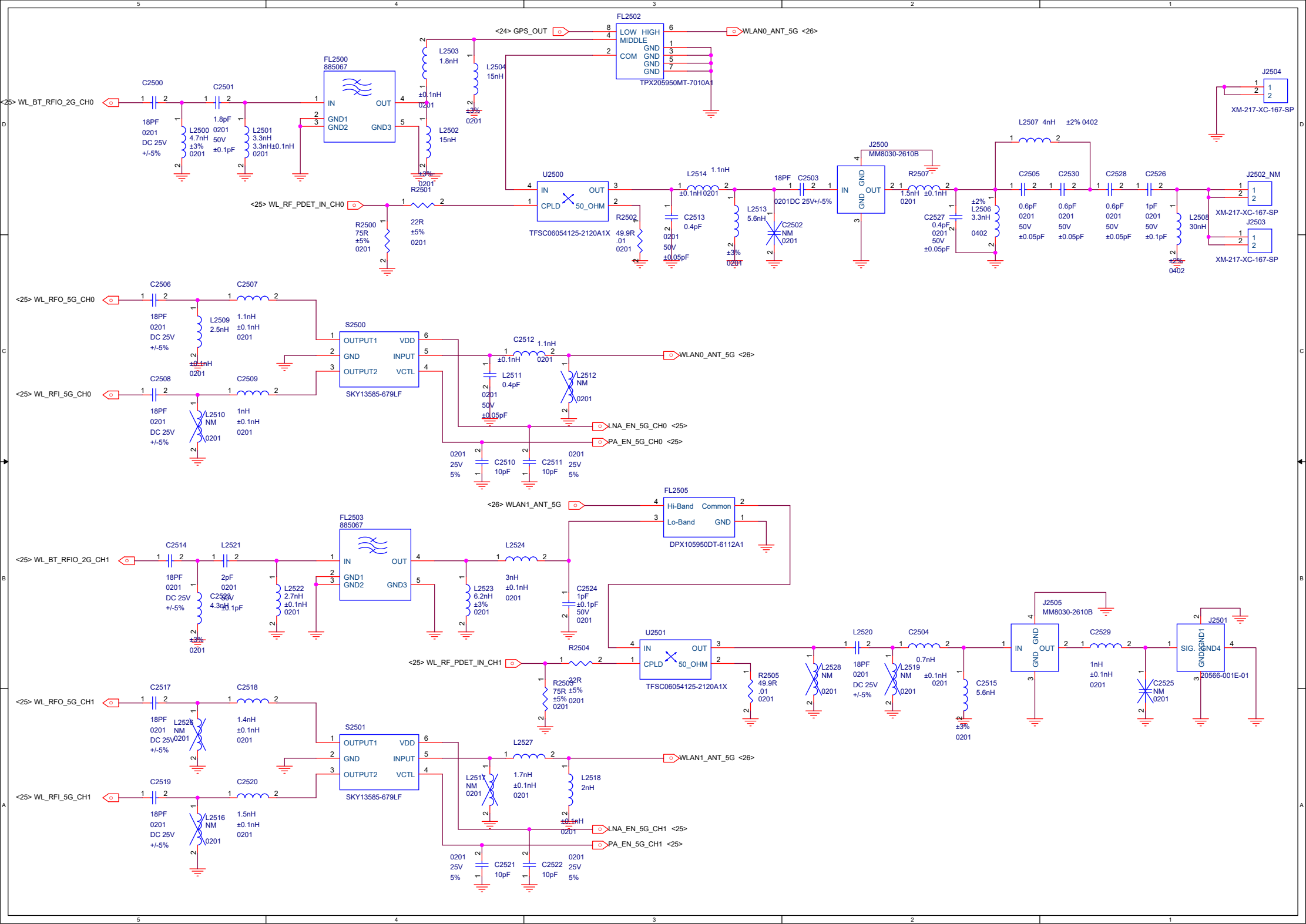


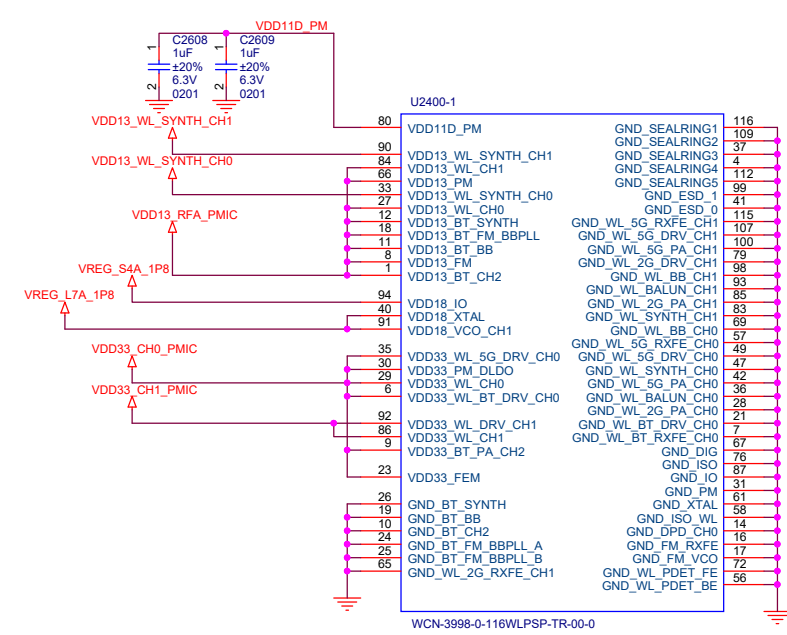
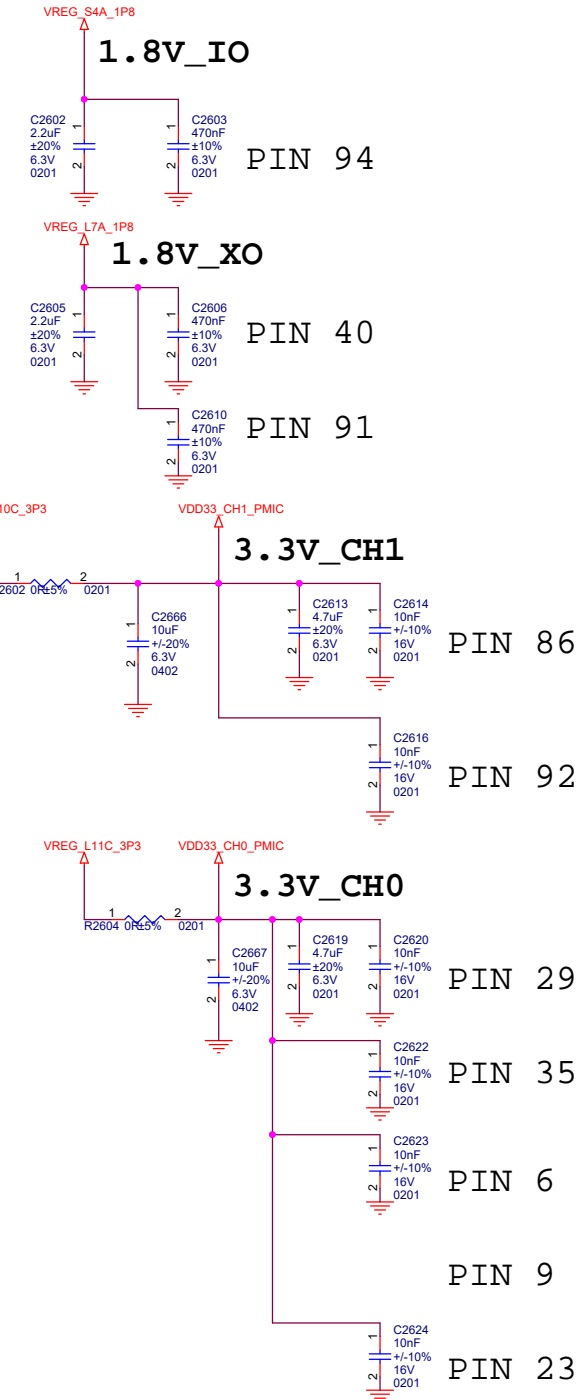
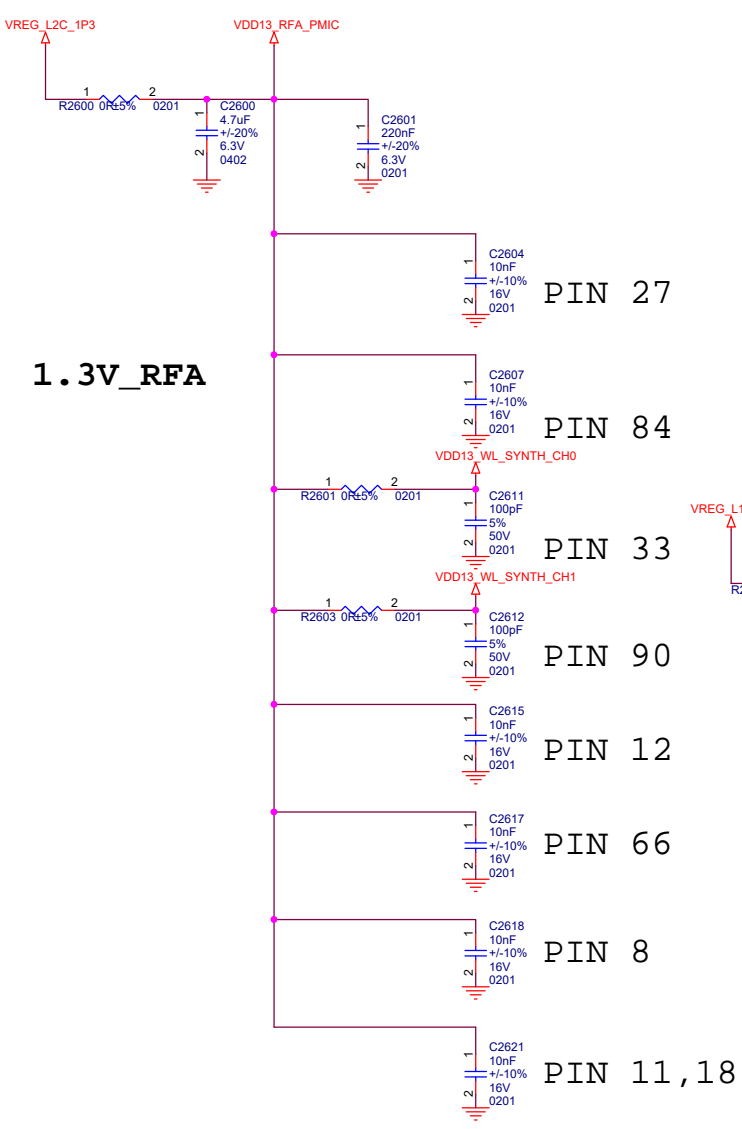


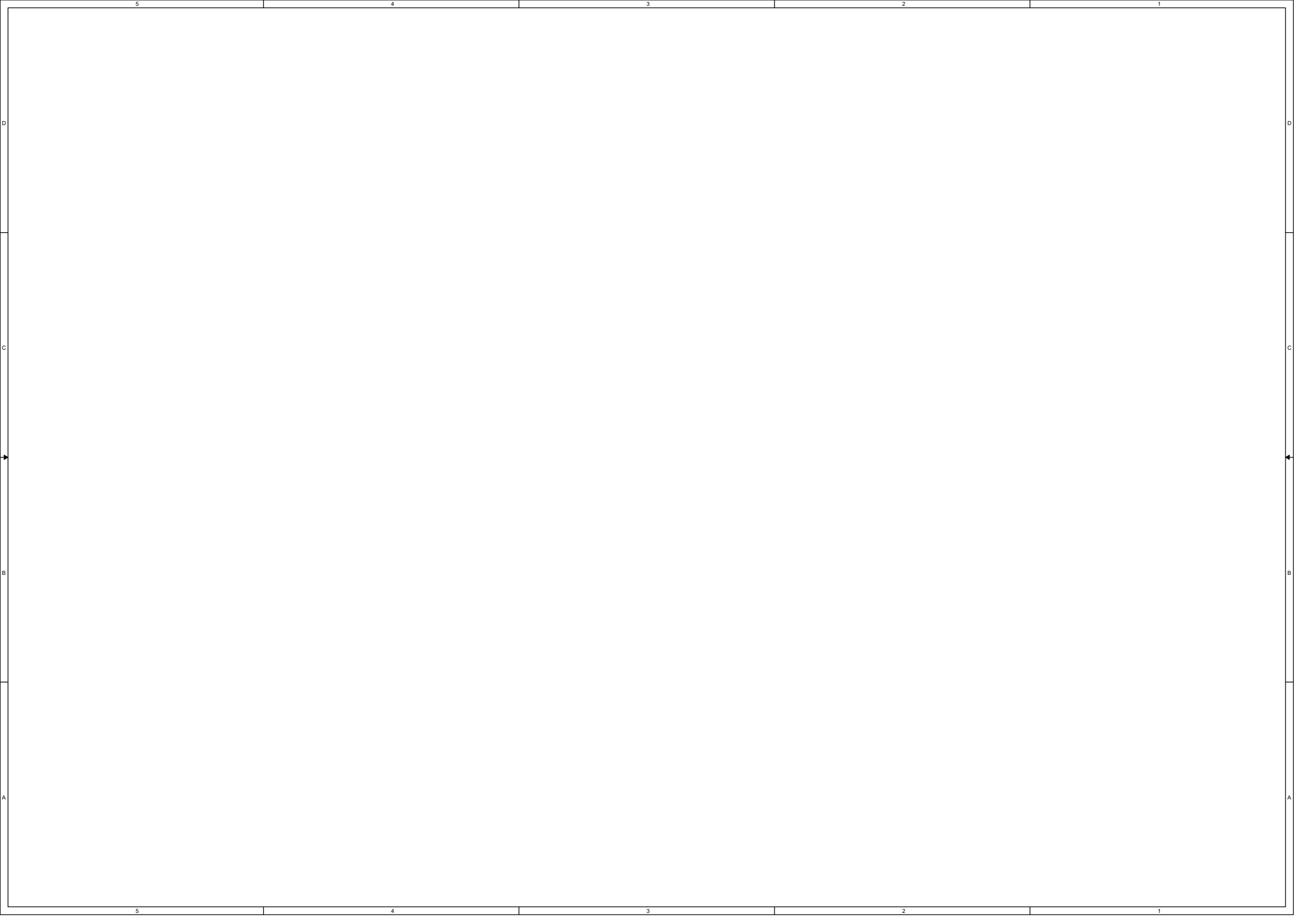


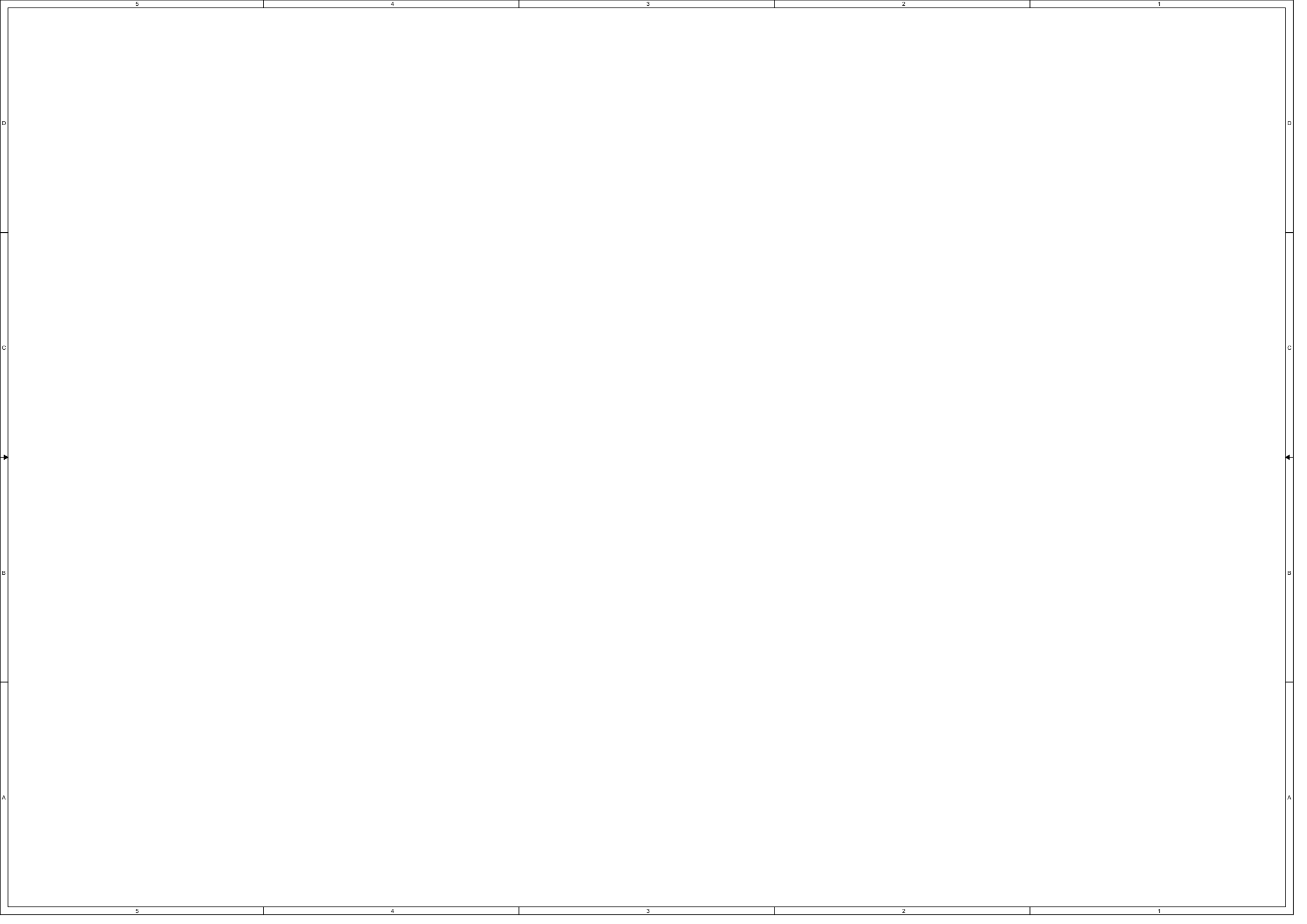


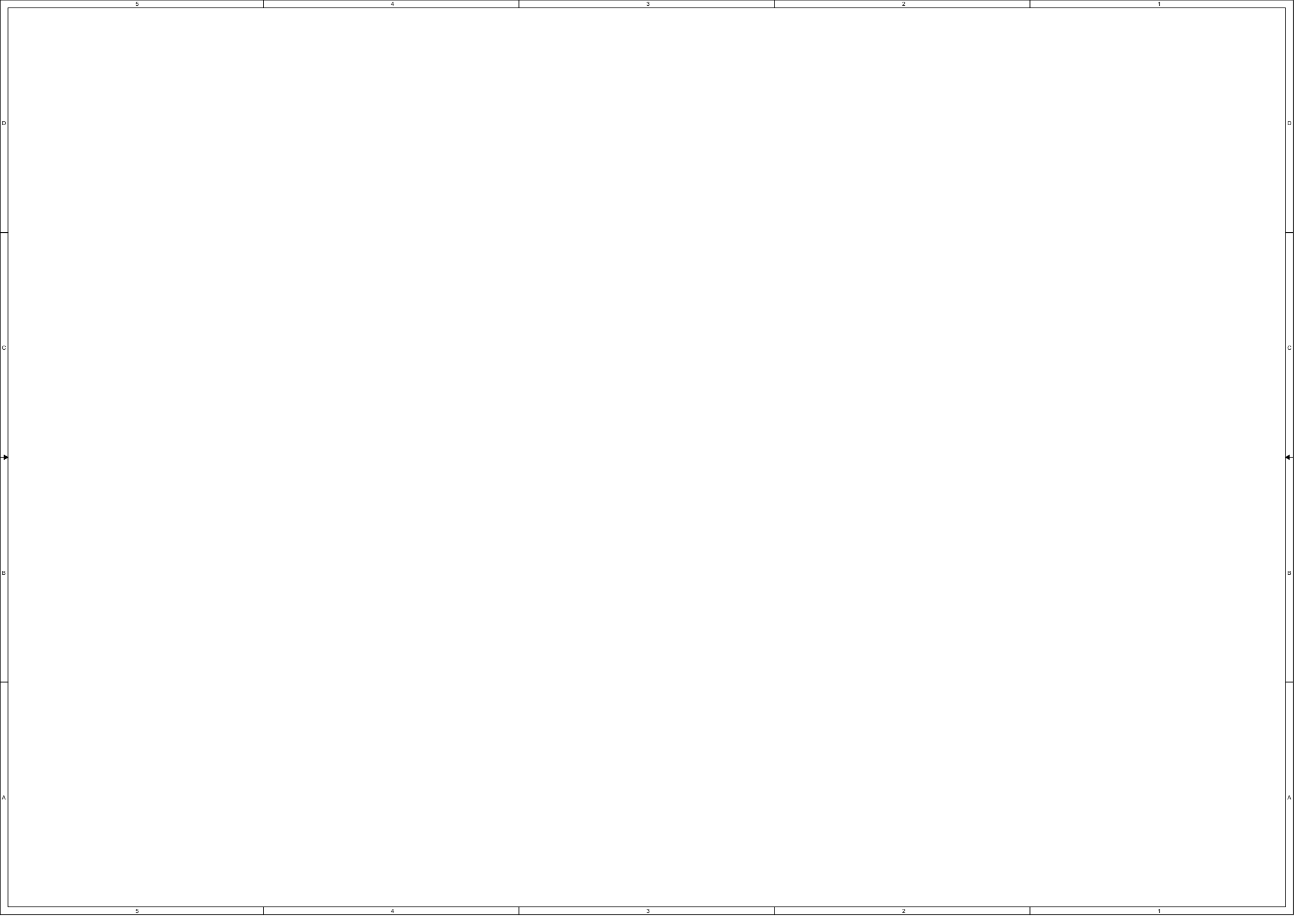


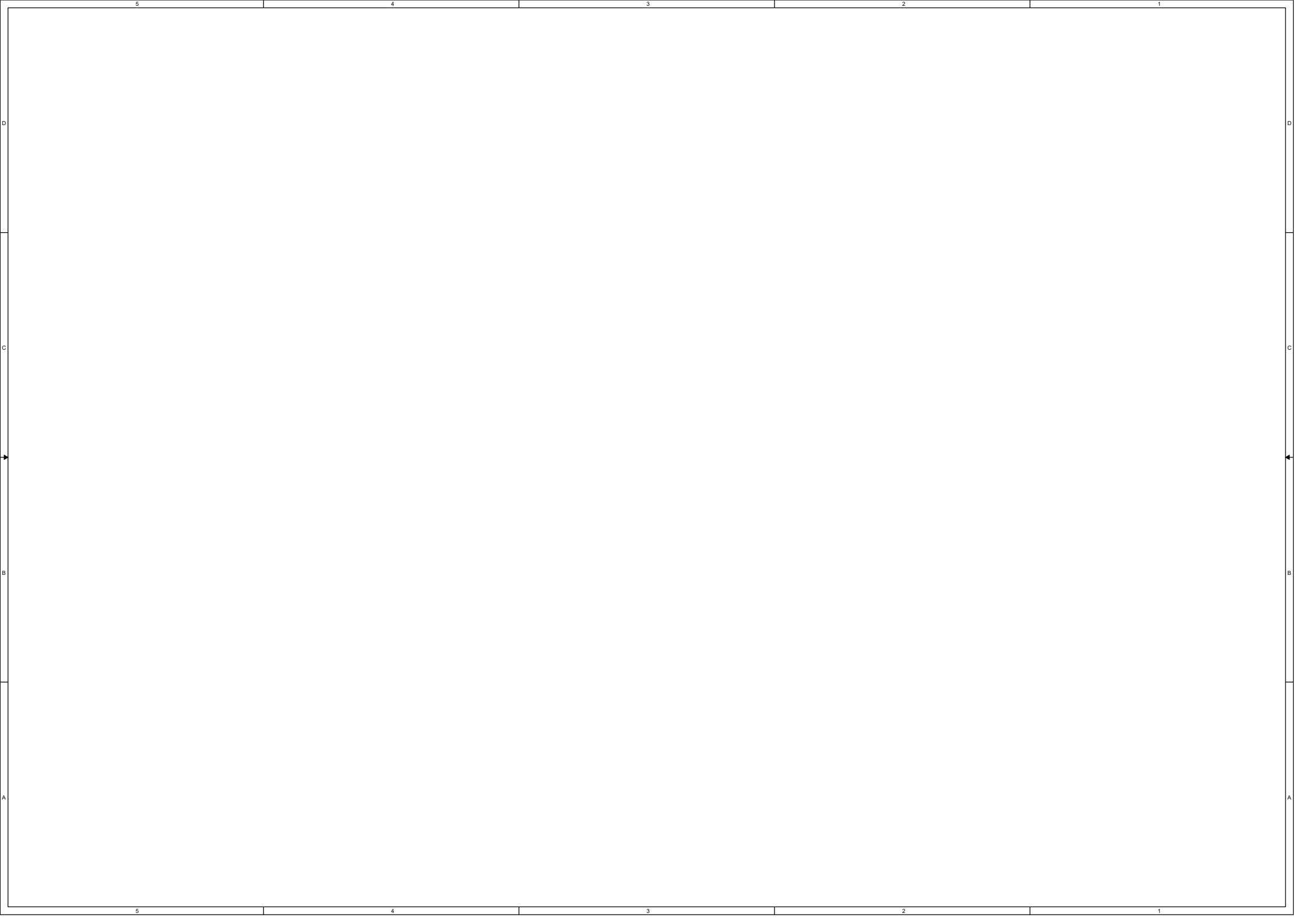


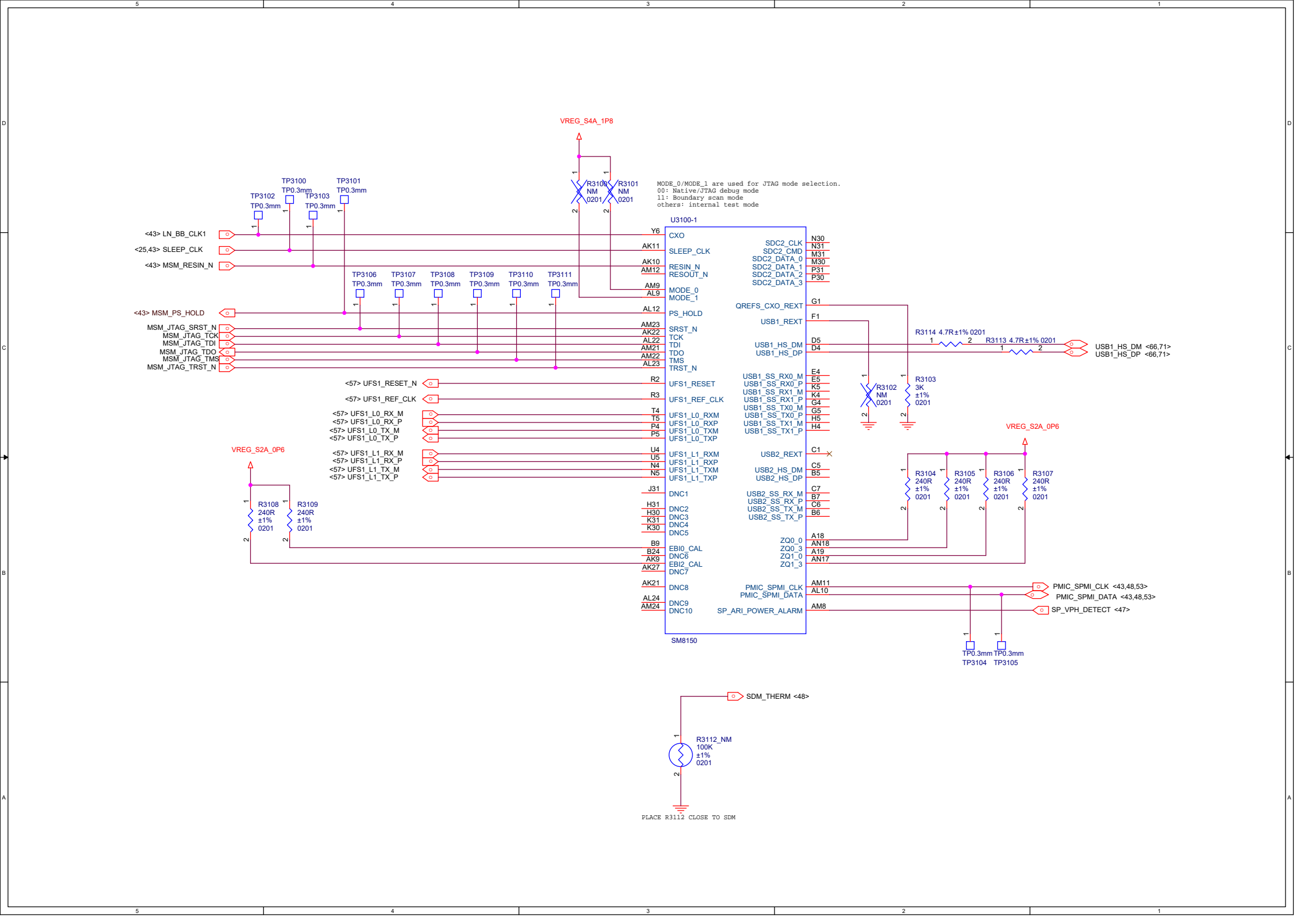




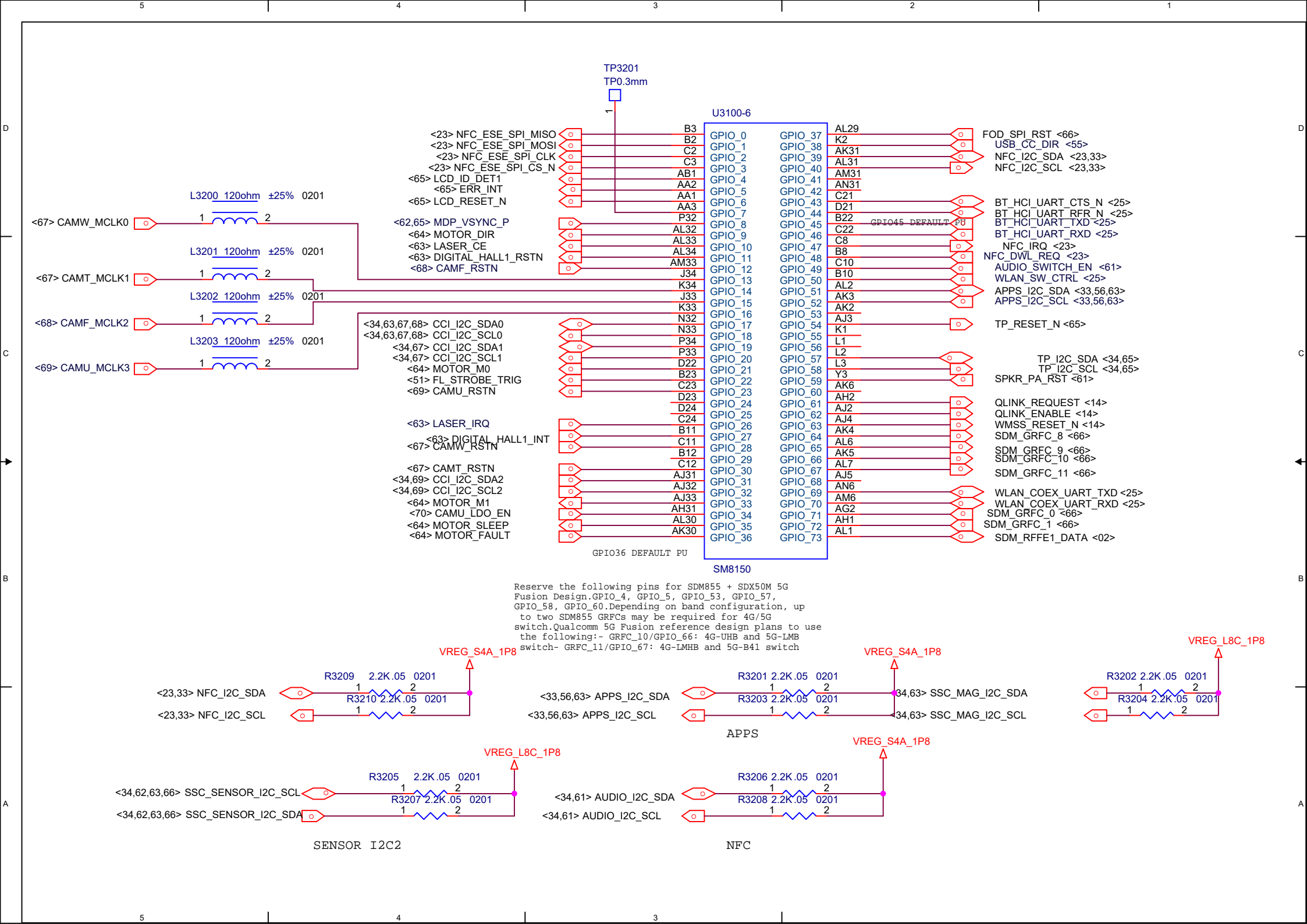


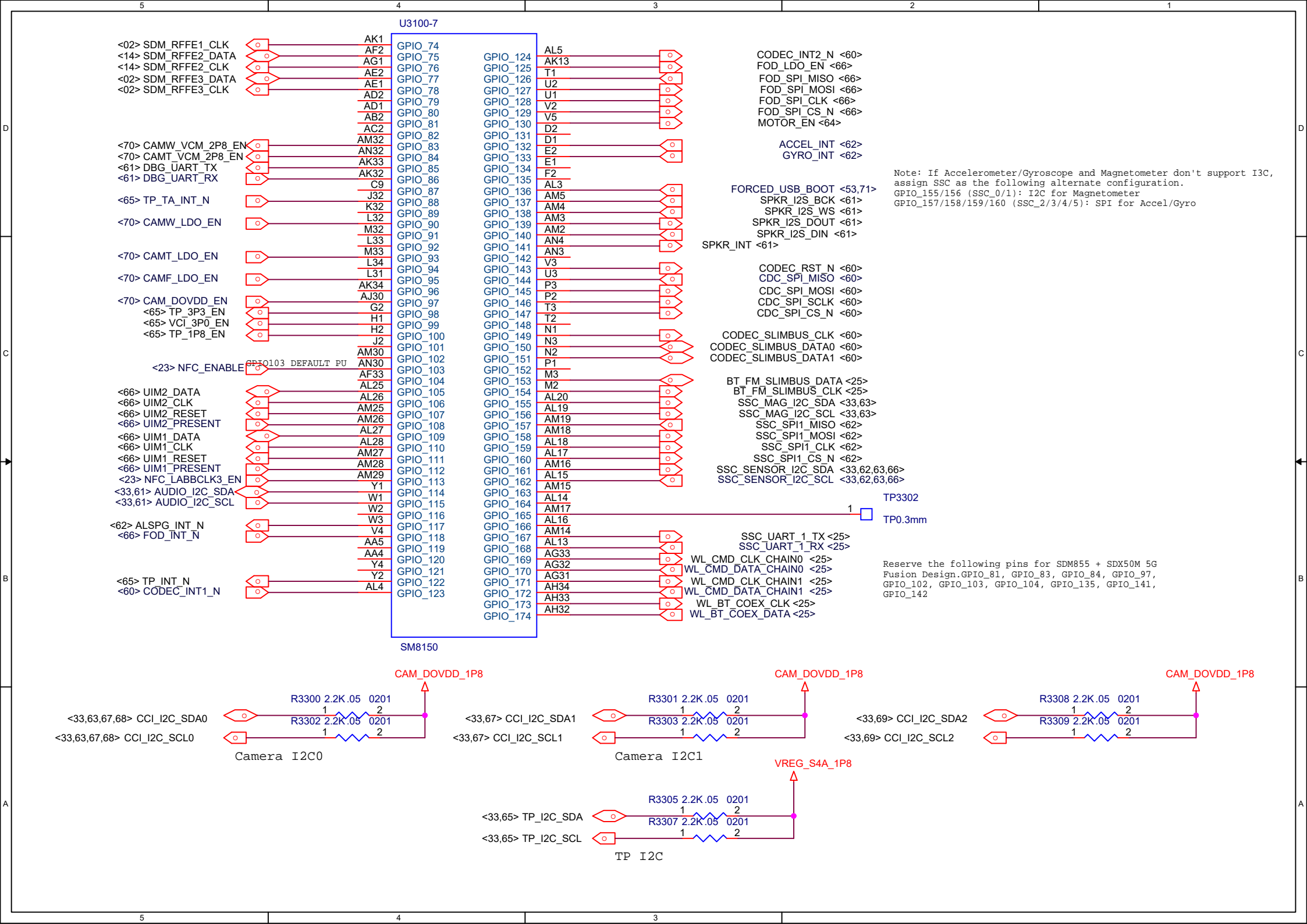


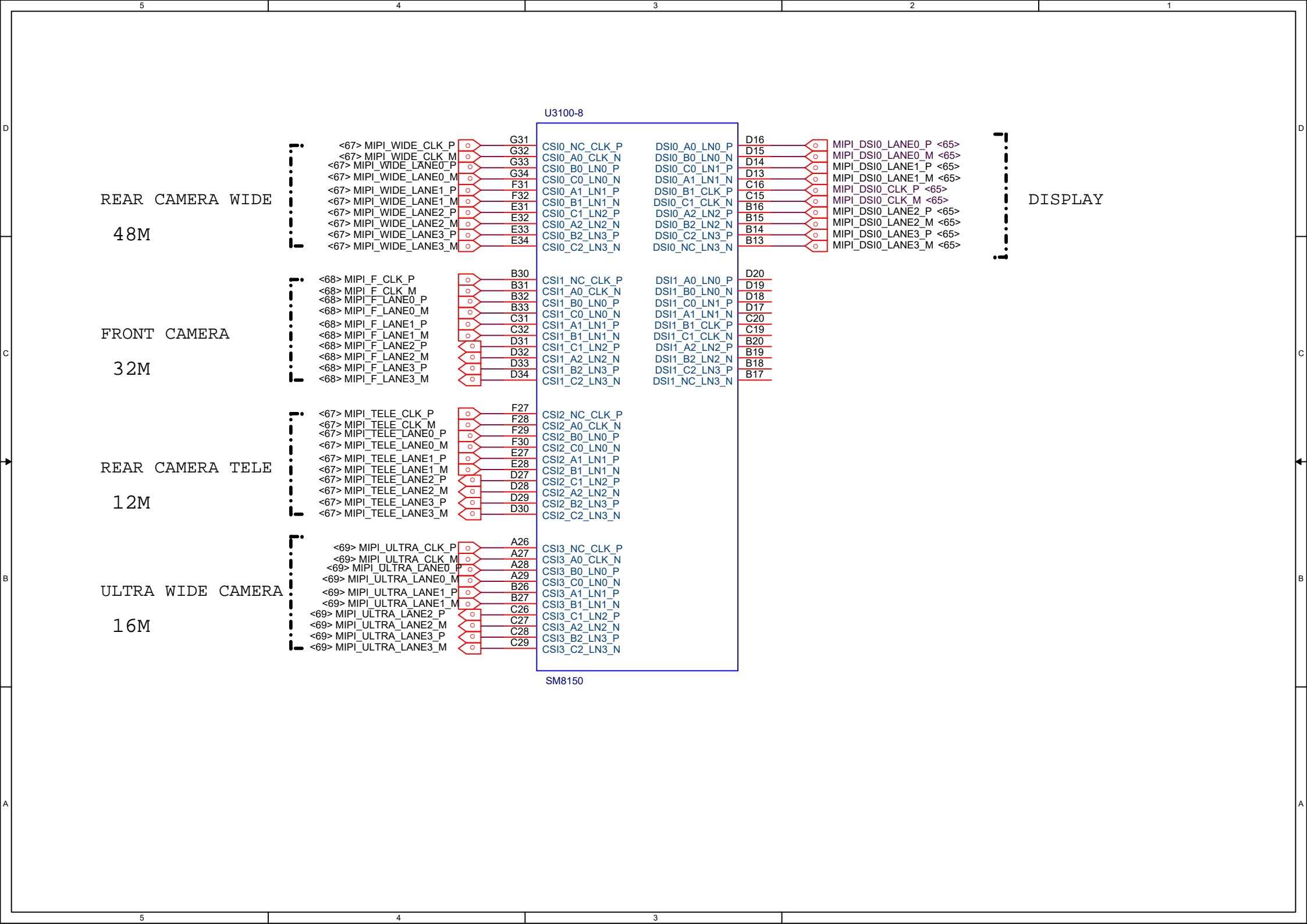


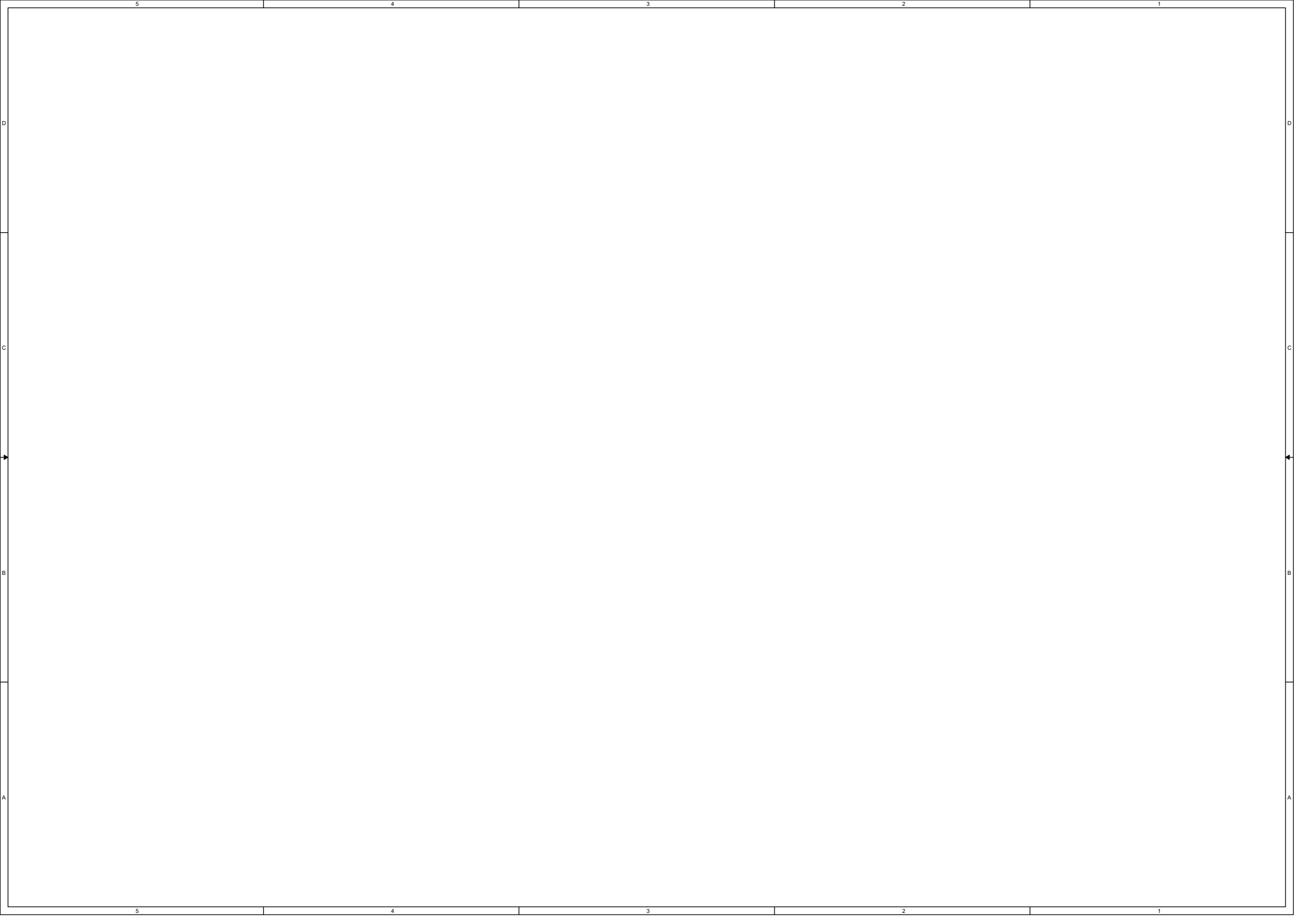


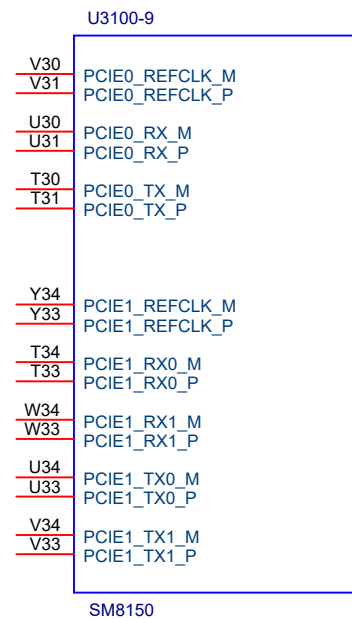
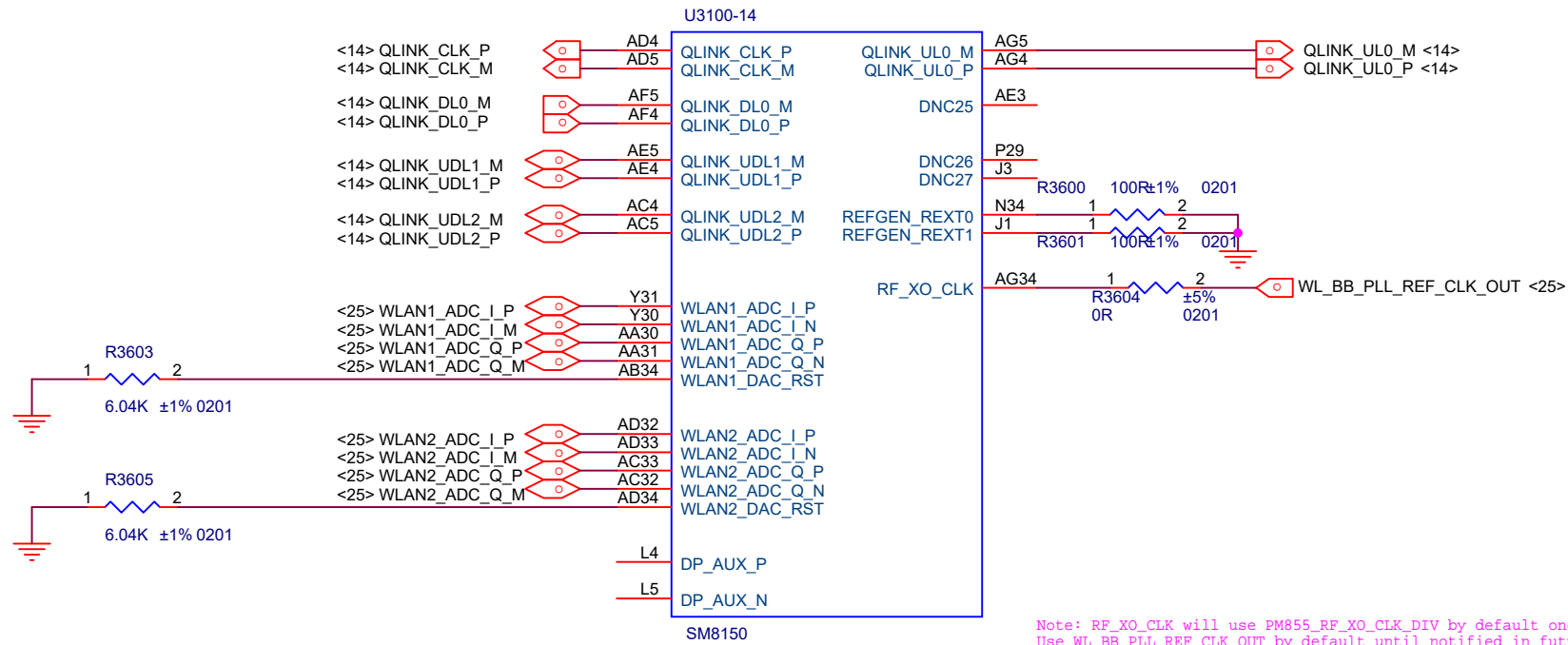






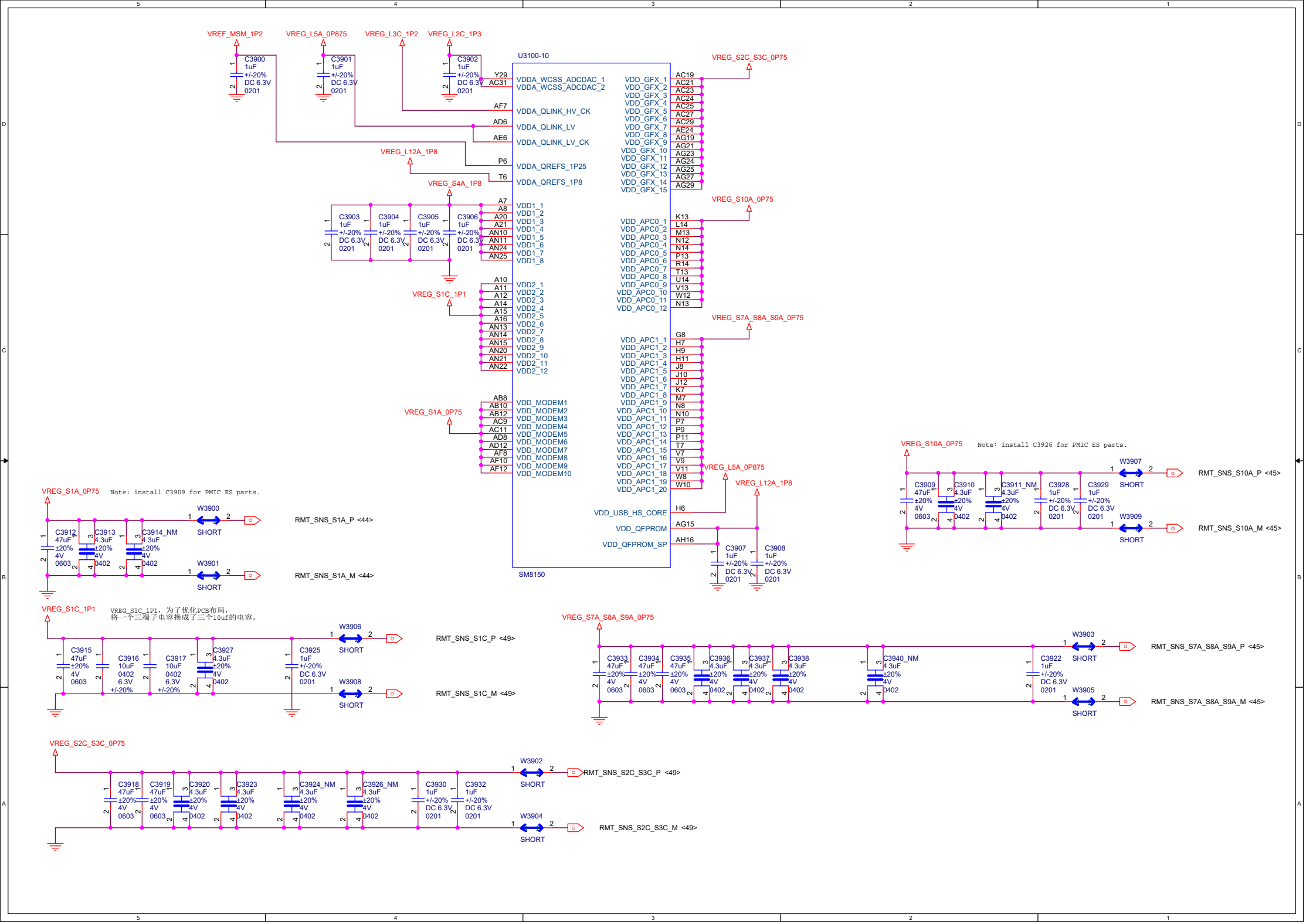




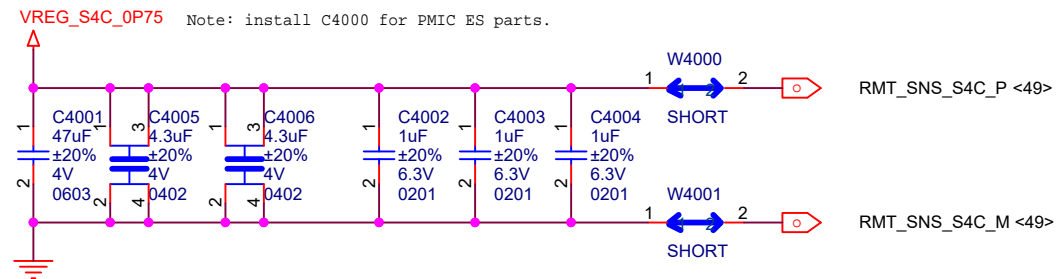
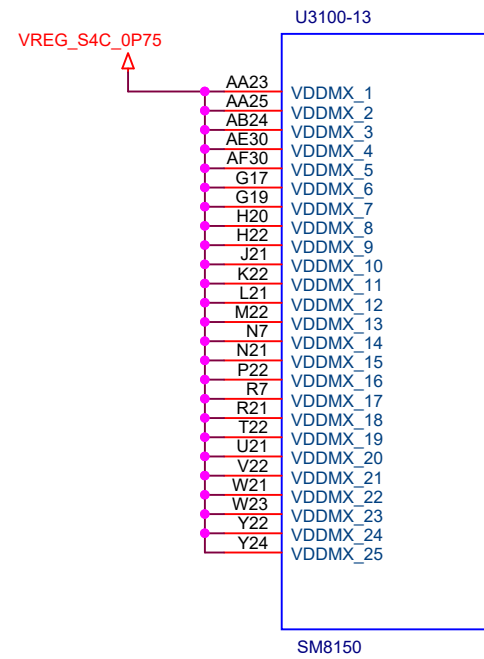


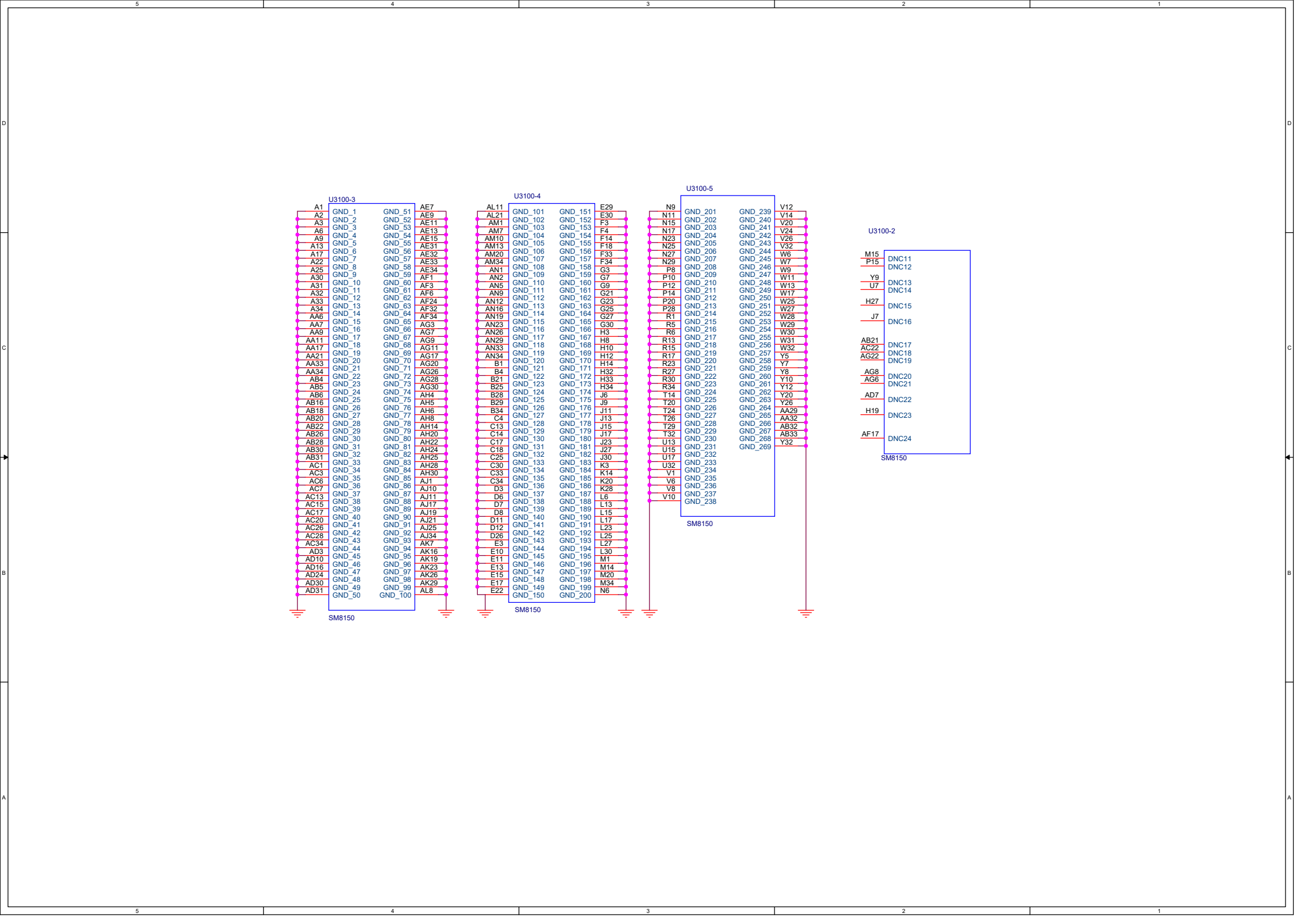












# Critical Layout Guidelines for Clocks

Coupling to any RFCLK or LNBBCLK output from each aggressor should be < 50 fF.

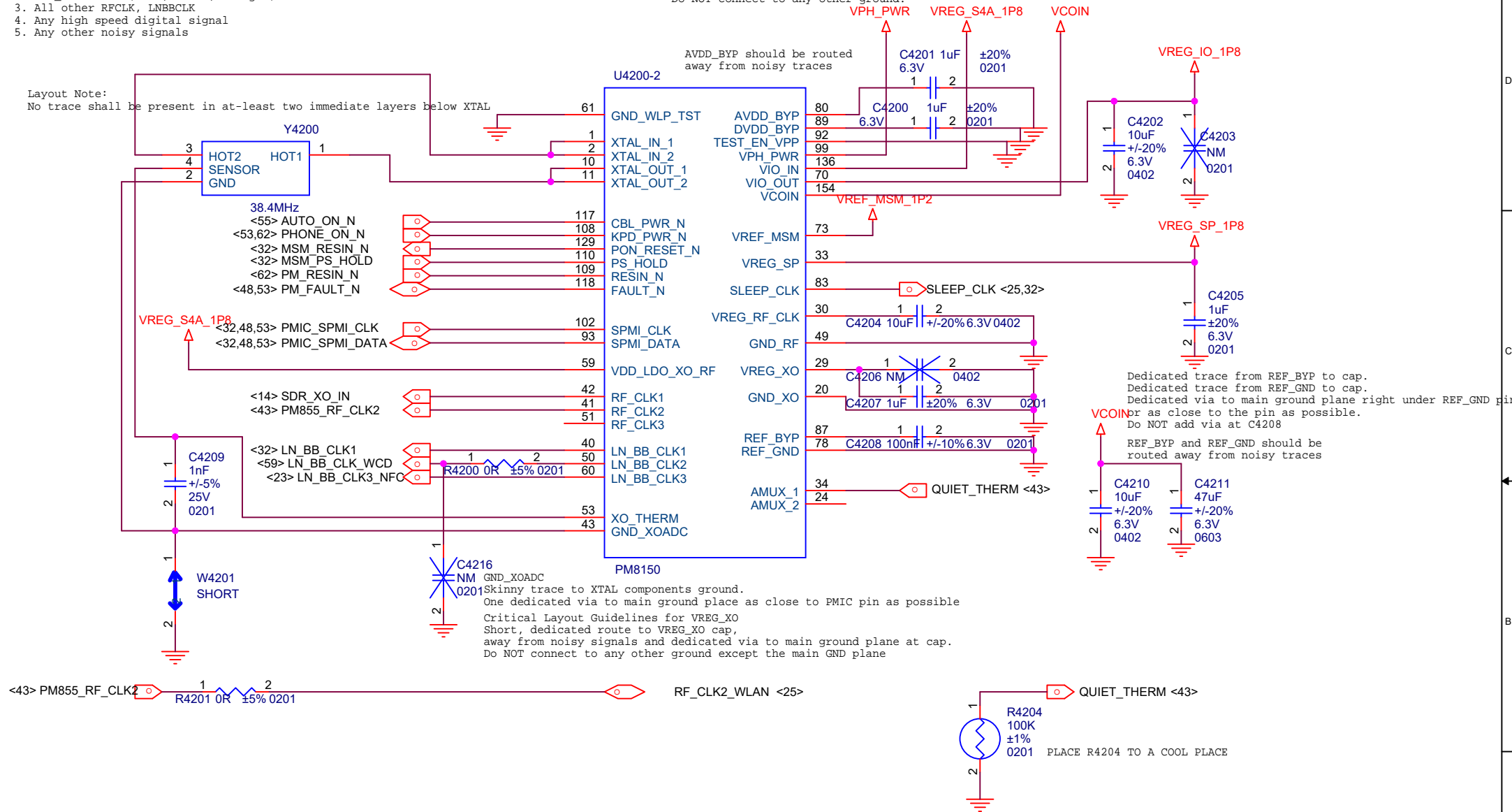
1. SMPS components (Buck, Boost, Charger)
2. VSW\_Sx traces (Buck, Boost, Charger)
3. All other RFCLK, LNBBCLK
4. Any high speed digital signal
5. Any other noisy signals

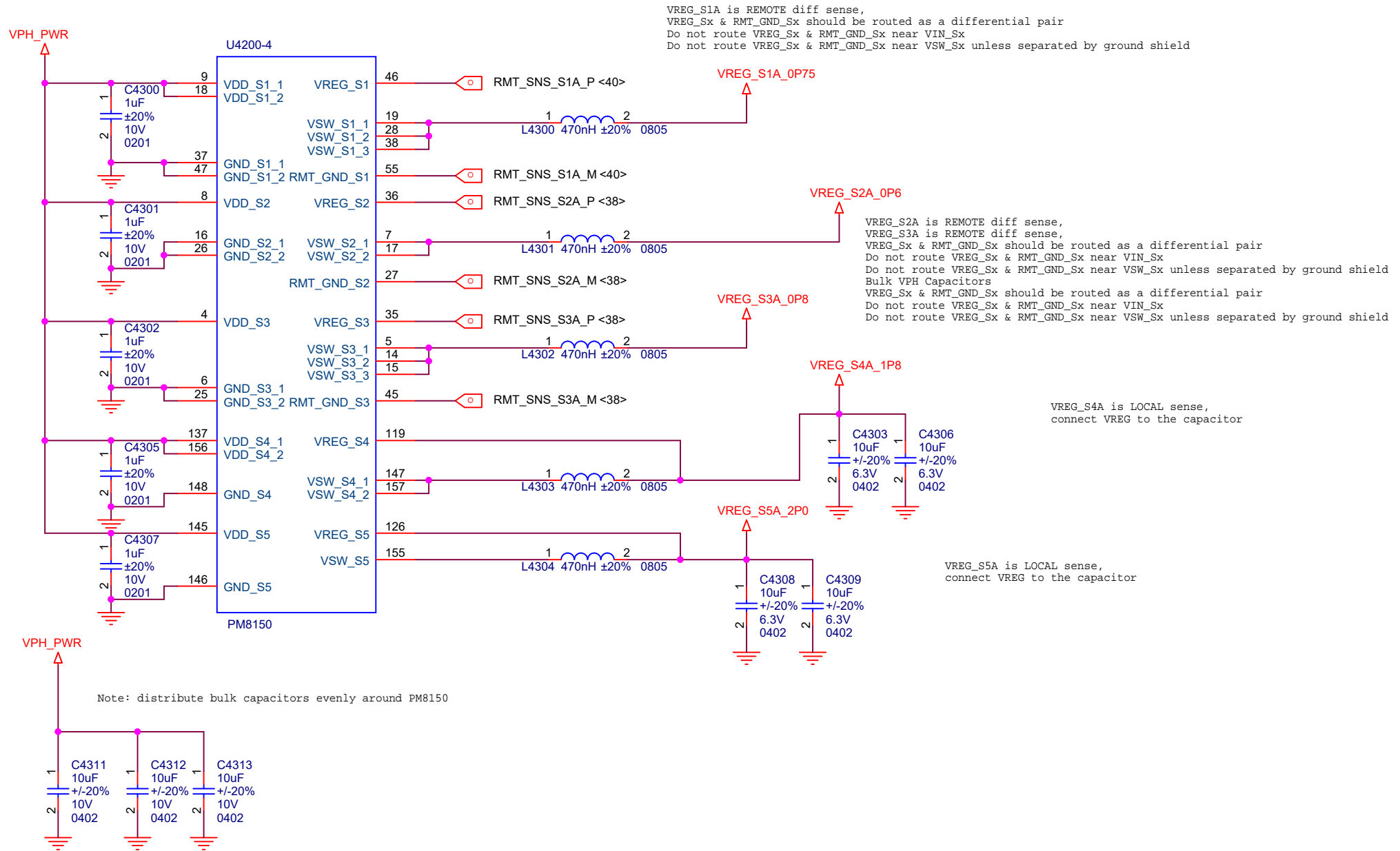
Trace from pin to cap and ONE dedicated via from cap to main ground plane.  
Do NOT connect to any other ground.

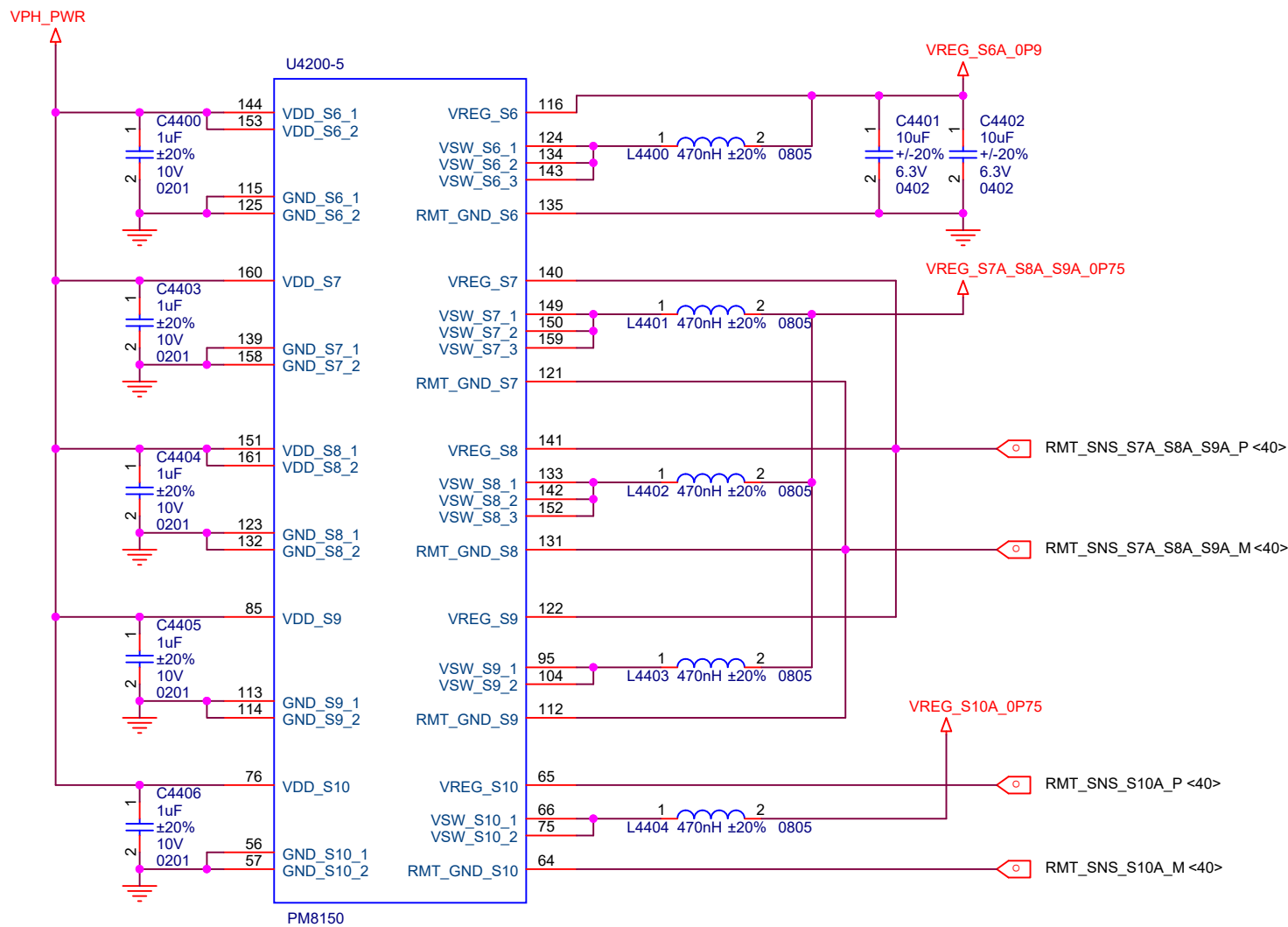
AVDD\_BYP should be routed away from noisy traces

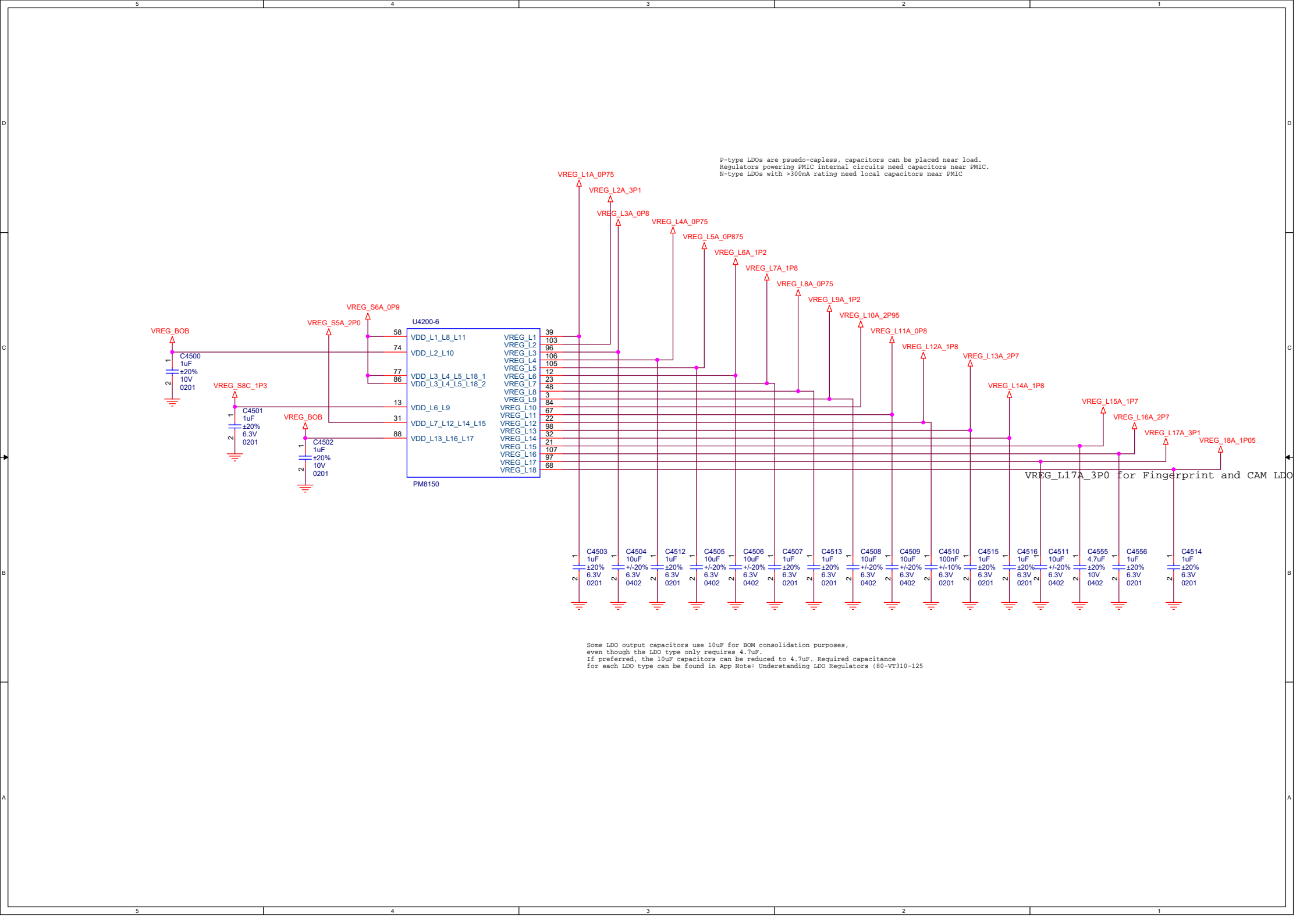
## Layout Note:

No trace shall be present in at-least two immediate layers below XTAL

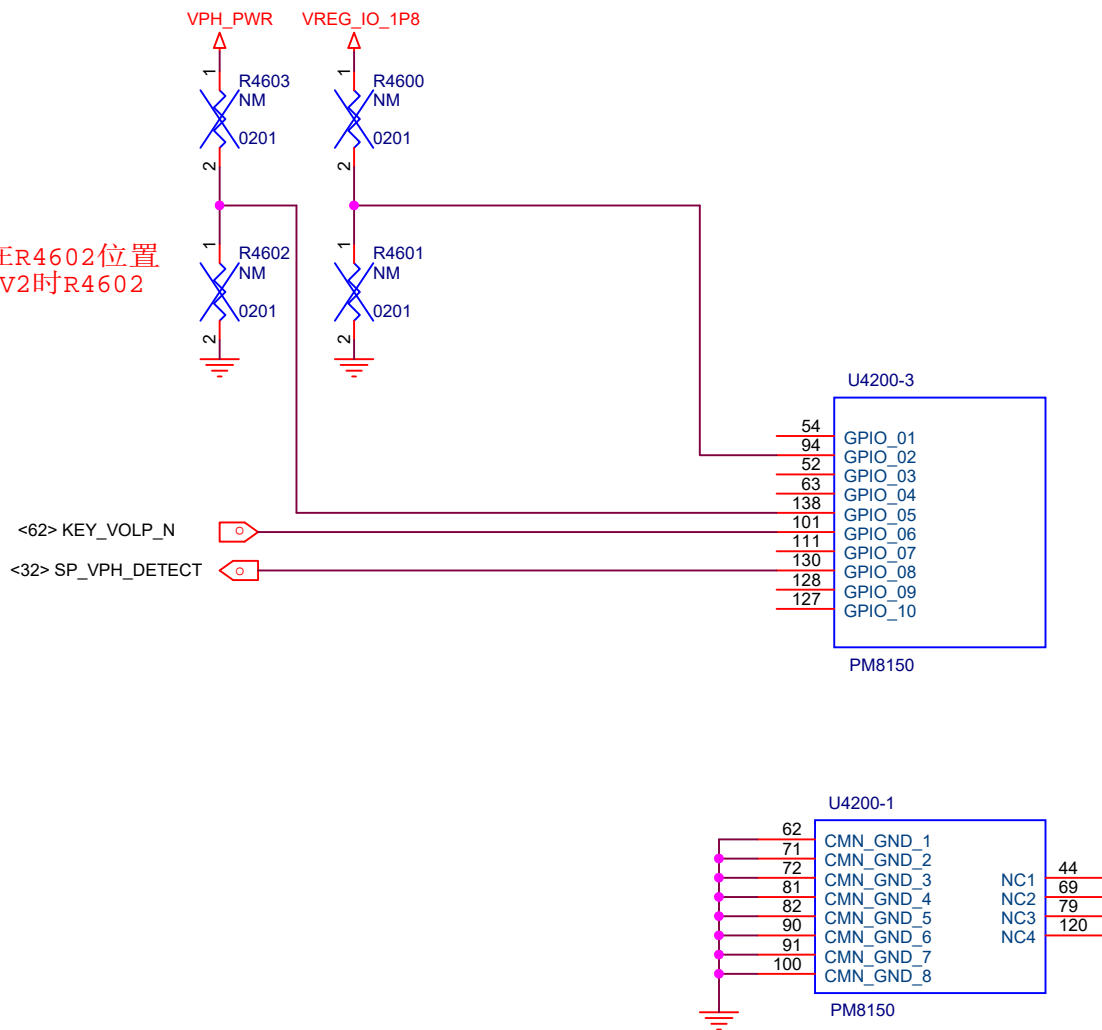


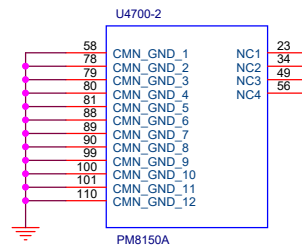
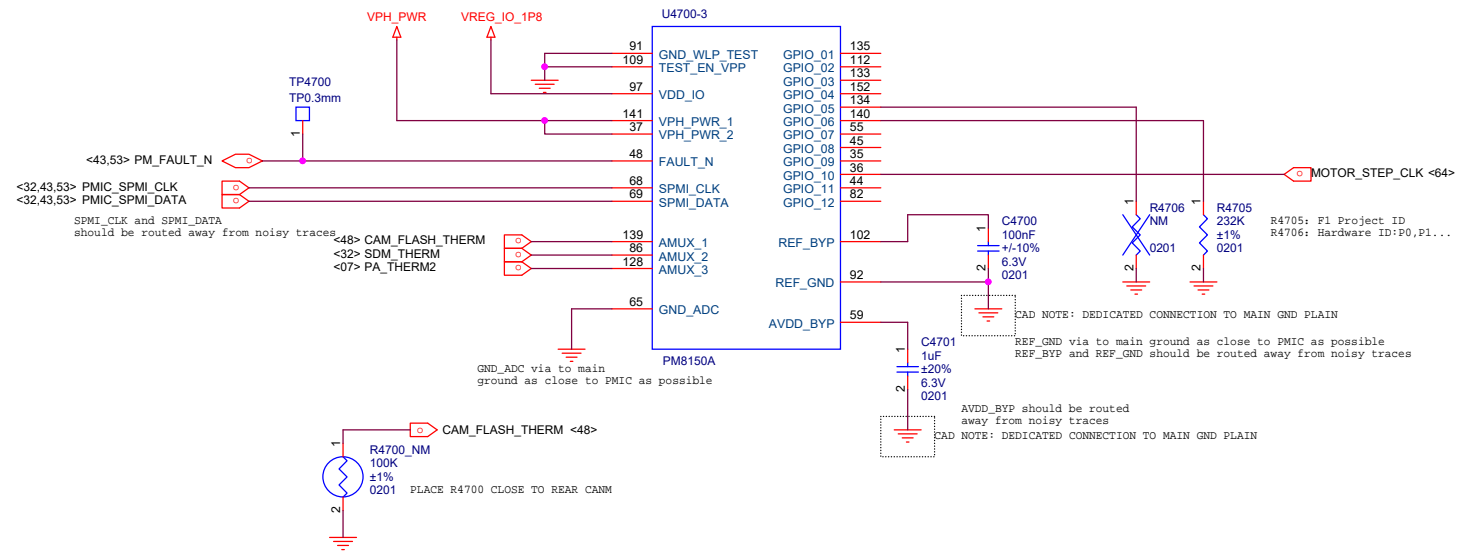






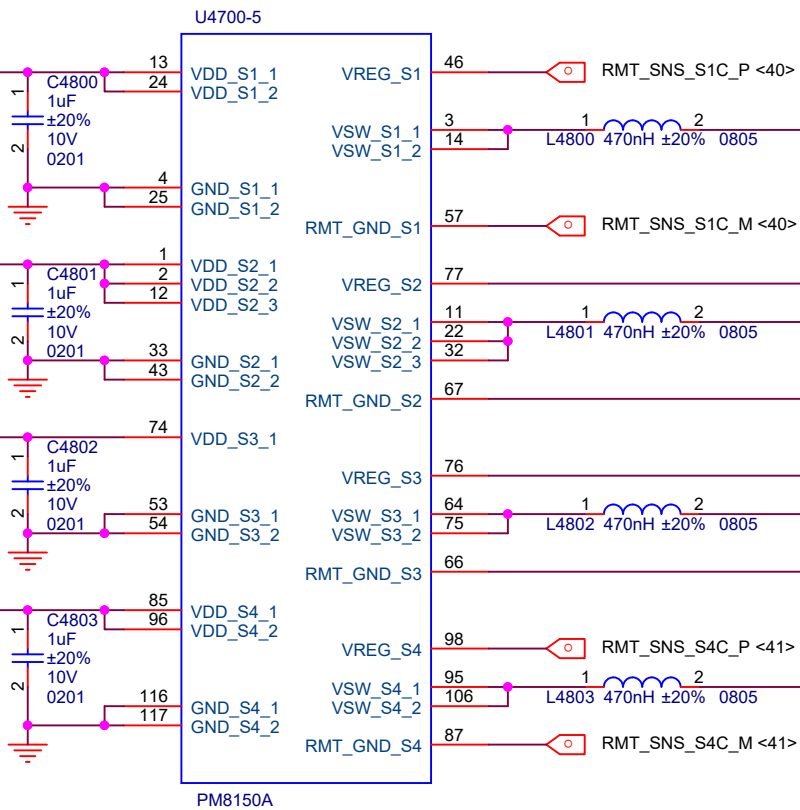
当使用PM8150 V3时需要在R4602位置  
贴0R电阻，目前ES芯片为V2时R4602  
不贴







VPH\_PWR

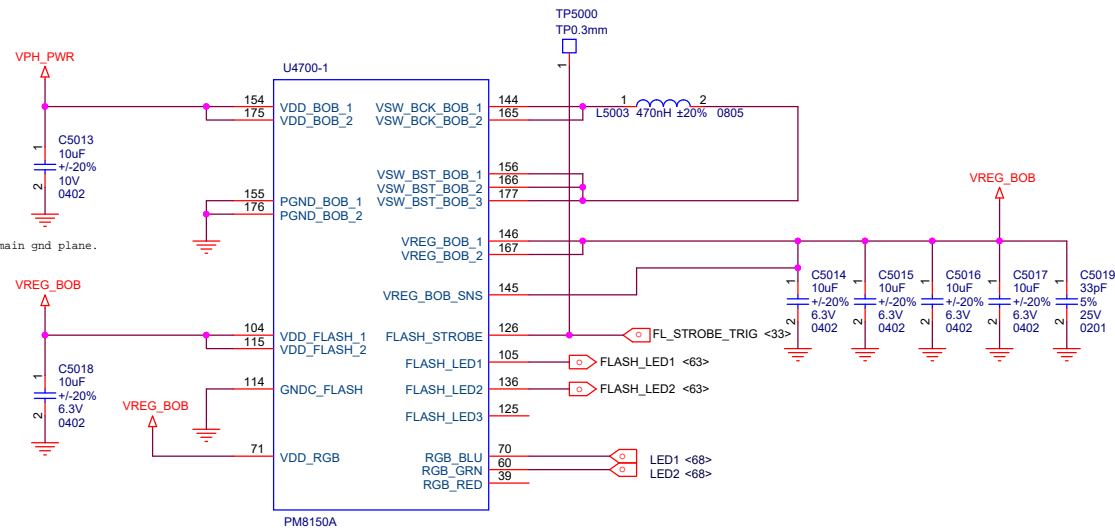
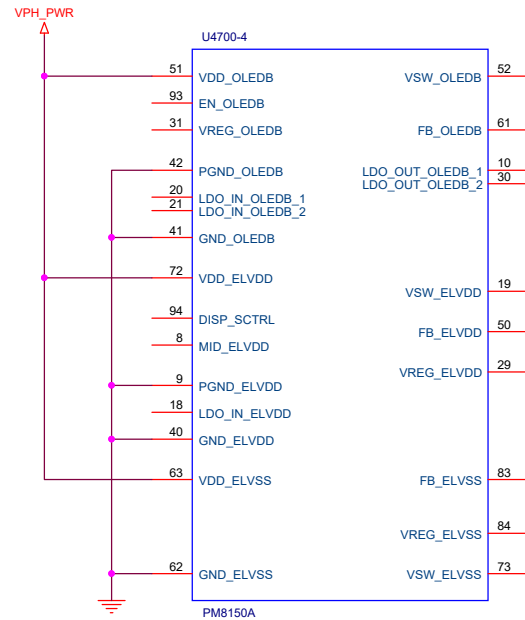


VREG\_S1C is REMOTE diff sense,  
VREG\_Sx & RMT\_GND\_Sx should be routed as a differential pair  
Do not route VREG\_Sx & RMT\_GND\_Sx near VIN\_Sx  
Do not route VREG\_Sx & RMT\_GND\_Sx near VSW\_Sx unless separated by ground shield

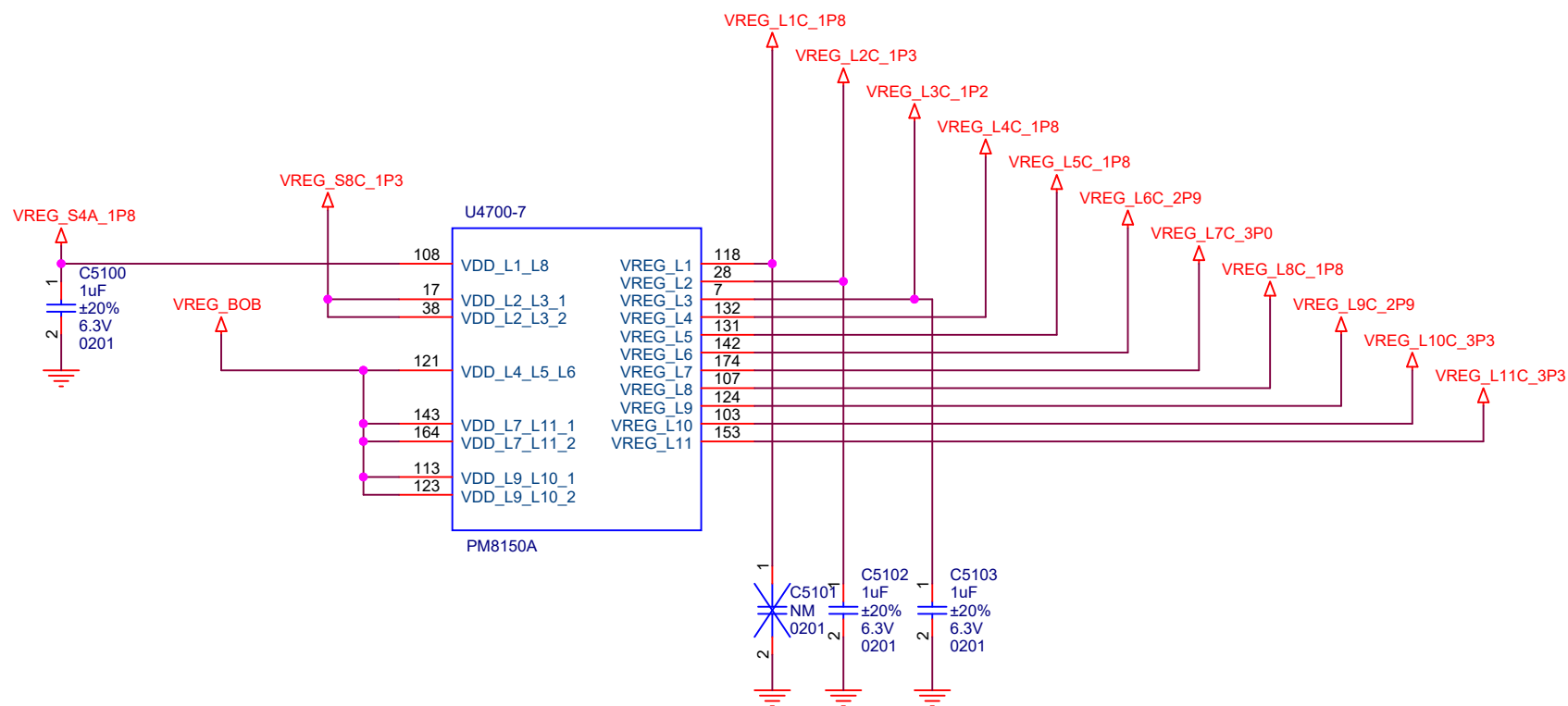
VREG\_S2C\_S3C is REMOTE diff sense,  
VREG\_Sx & RMT\_GND\_Sx should be routed as a differential pair  
Do not route VREG\_Sx & RMT\_GND\_Sx near VIN\_Sx  
Do not route VREG\_Sx & RMT\_GND\_Sx near VSW\_Sx unless separated by ground shield

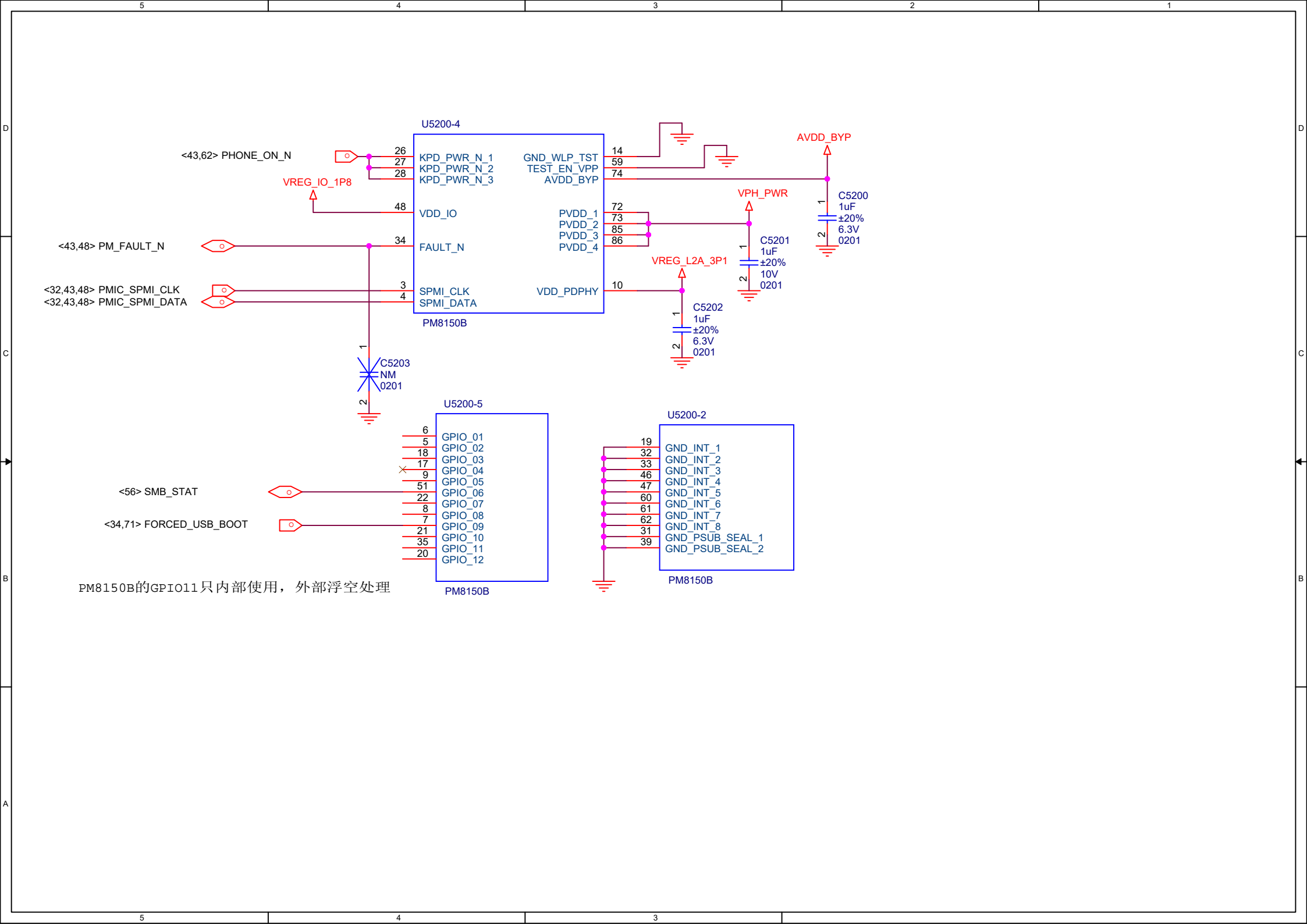
VREG\_S4C is REMOTE diff sense,  
VREG\_Sx & RMT\_GND\_Sx should be routed as a differential pair  
Do not route VREG\_Sx & RMT\_GND\_Sx near VIN\_Sx  
Do not route VREG\_Sx & RMT\_GND\_Sx near VSW\_Sx unless separated by ground shield

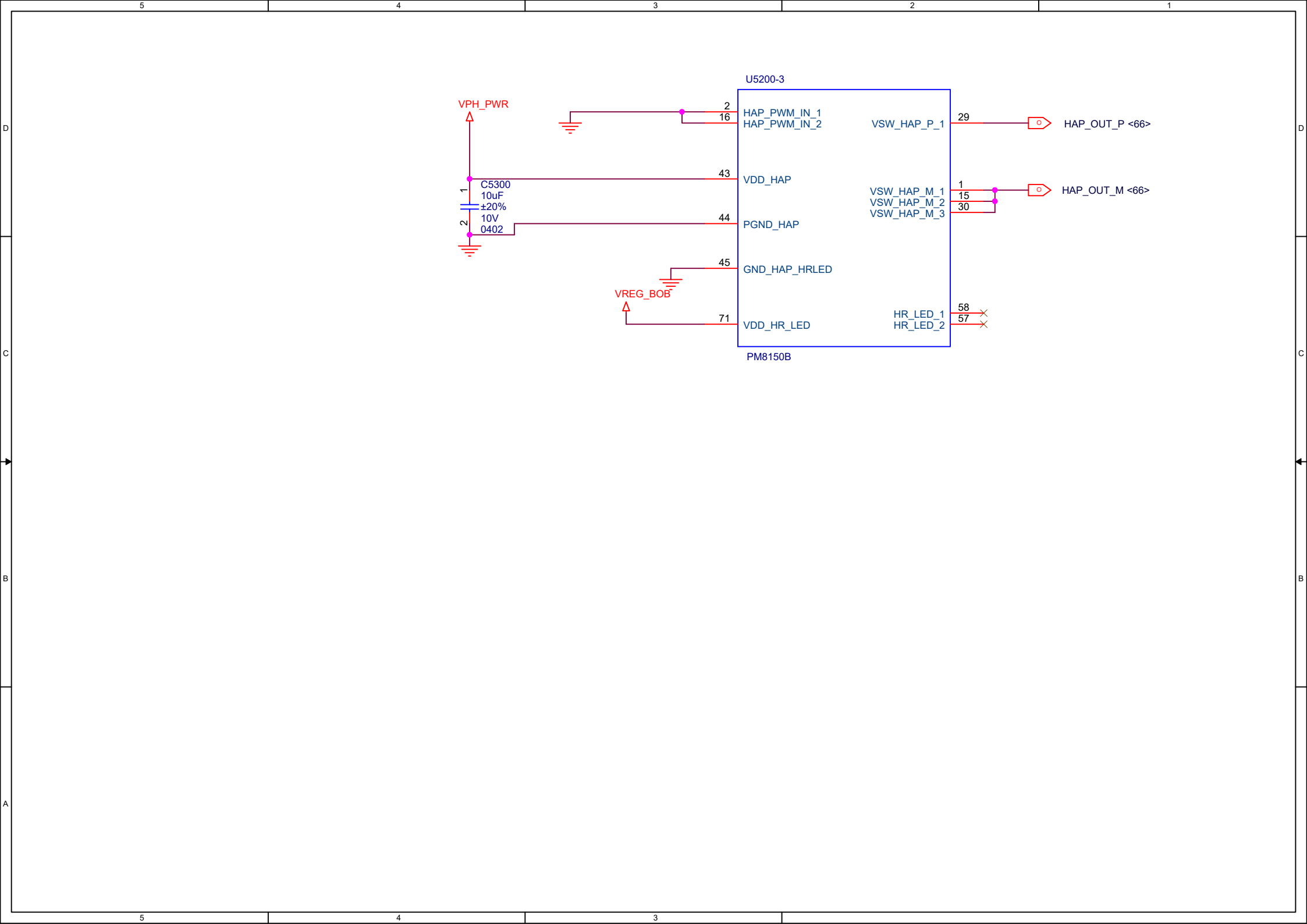


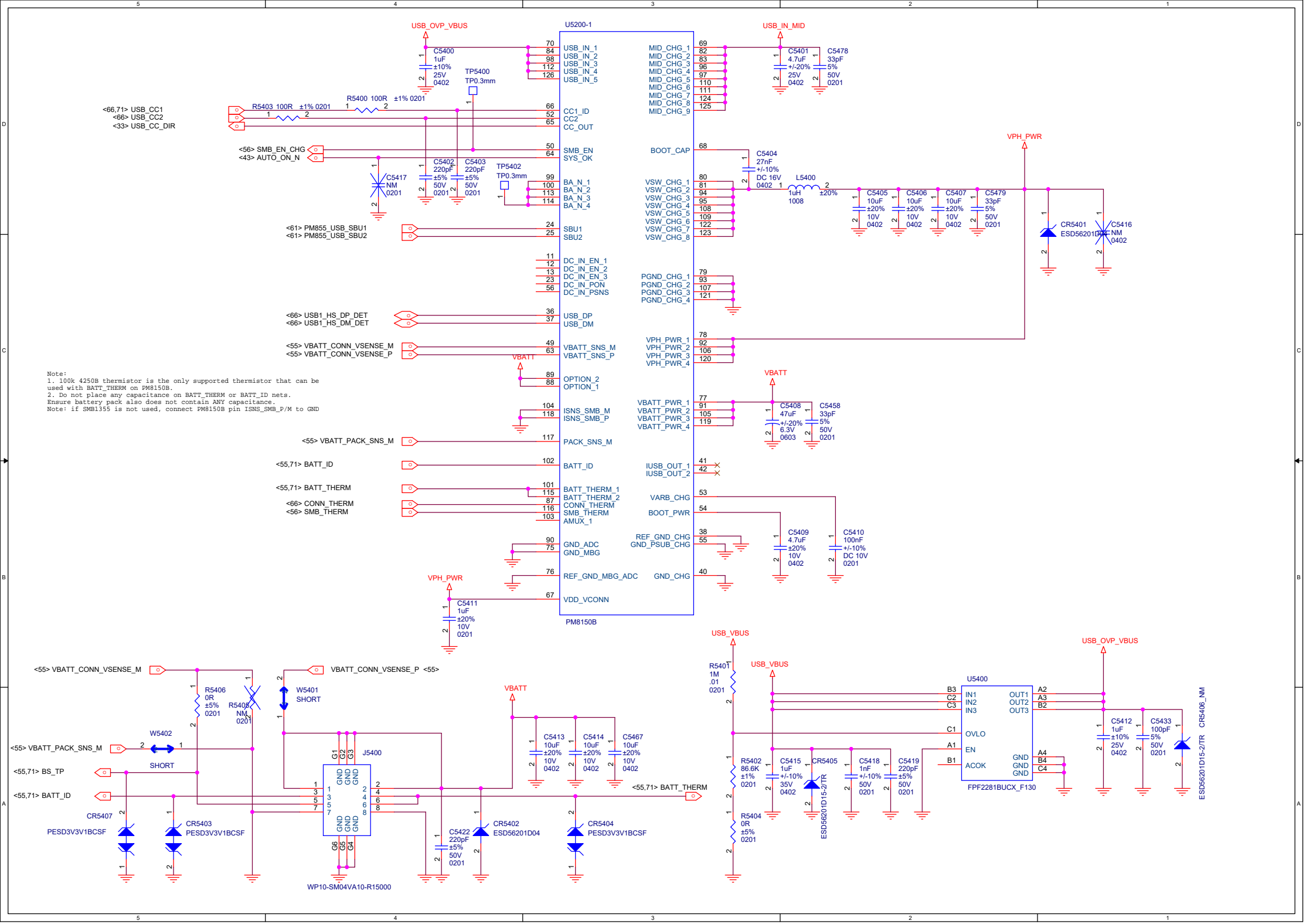


Layout Note:PGND\_BOB  
Dedicated trace from pin to COUT1 and Cin. Dedicated vias from cap directly to main gnd plane.  
Trace and vias should be able to handle 3A of continuous current.  
Do NOT connect to any other grounds.\*

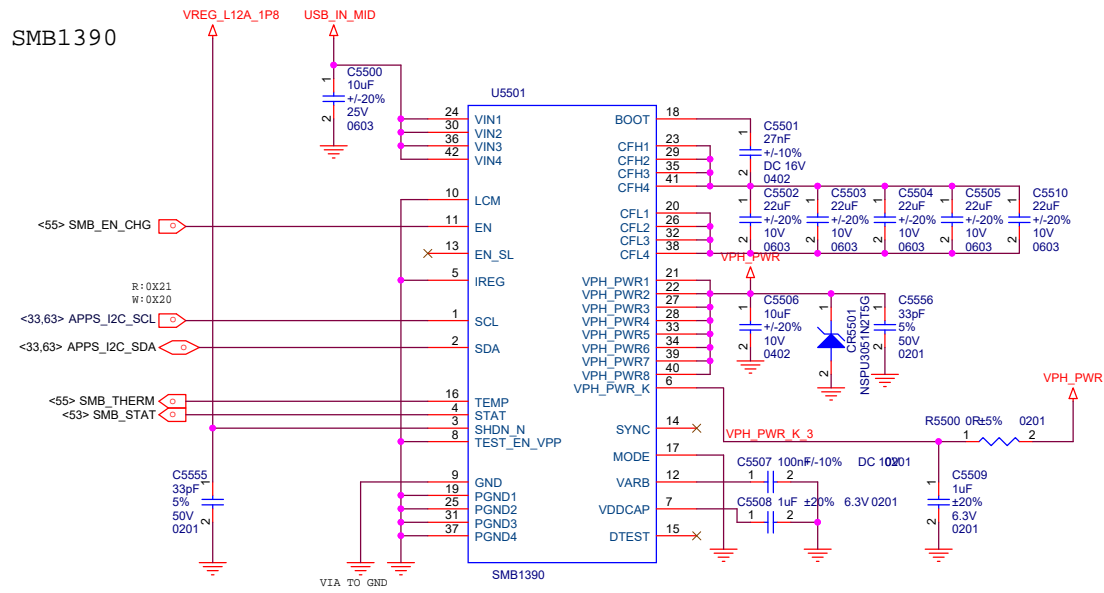




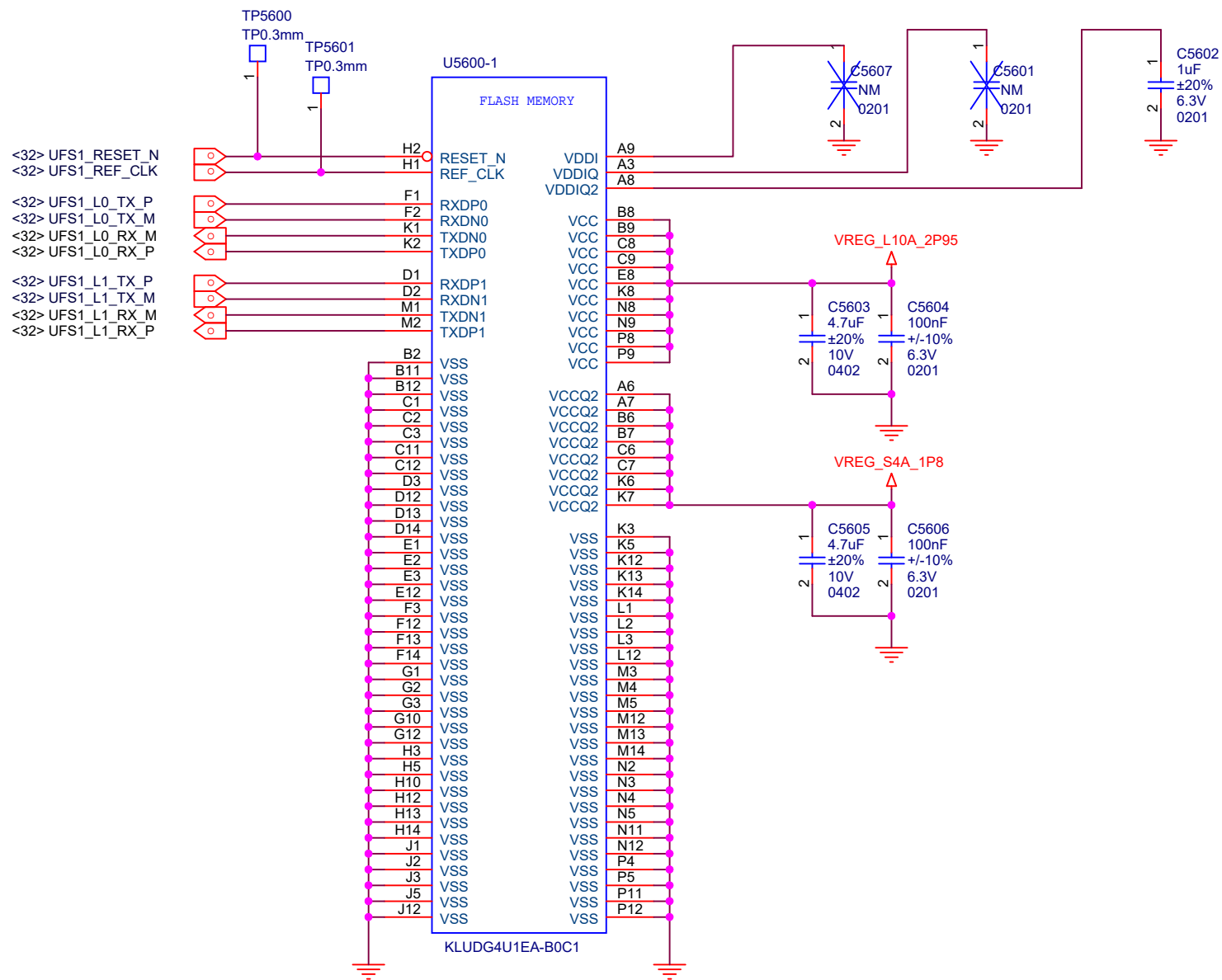


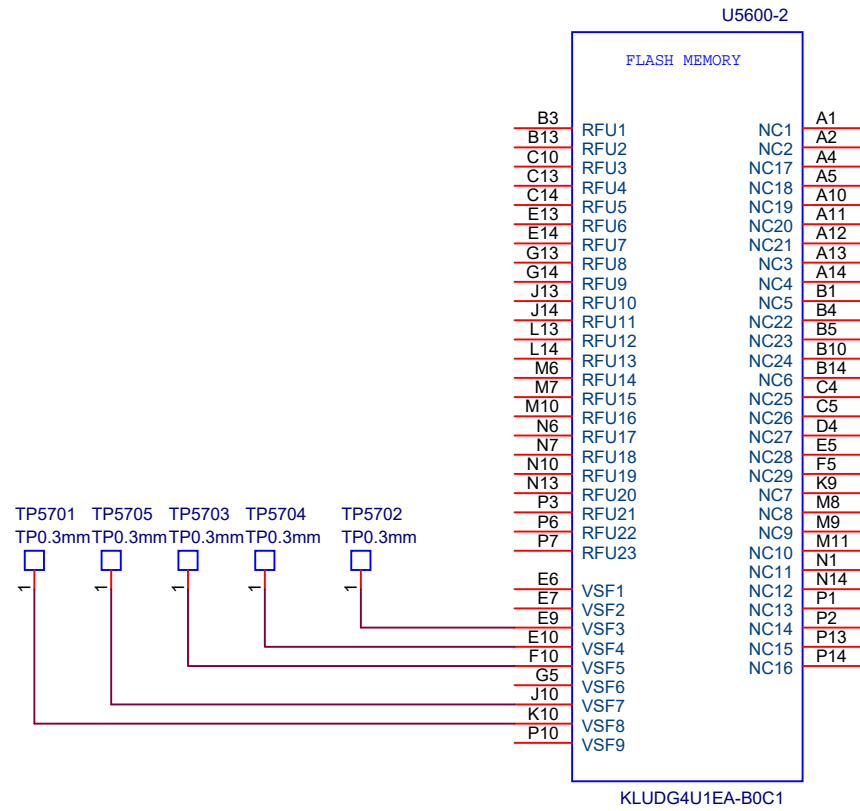


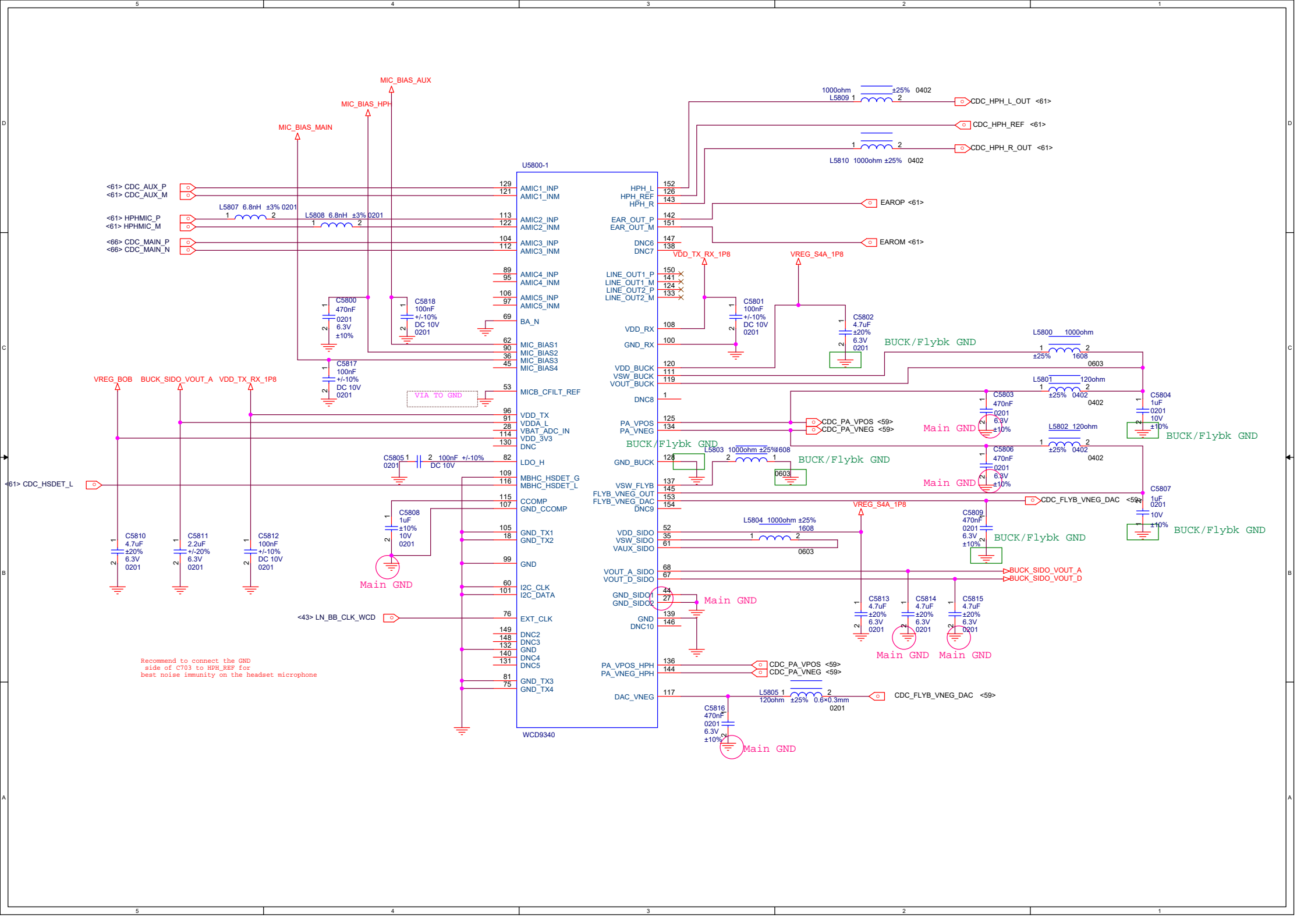
# SMB1390











D

D

C

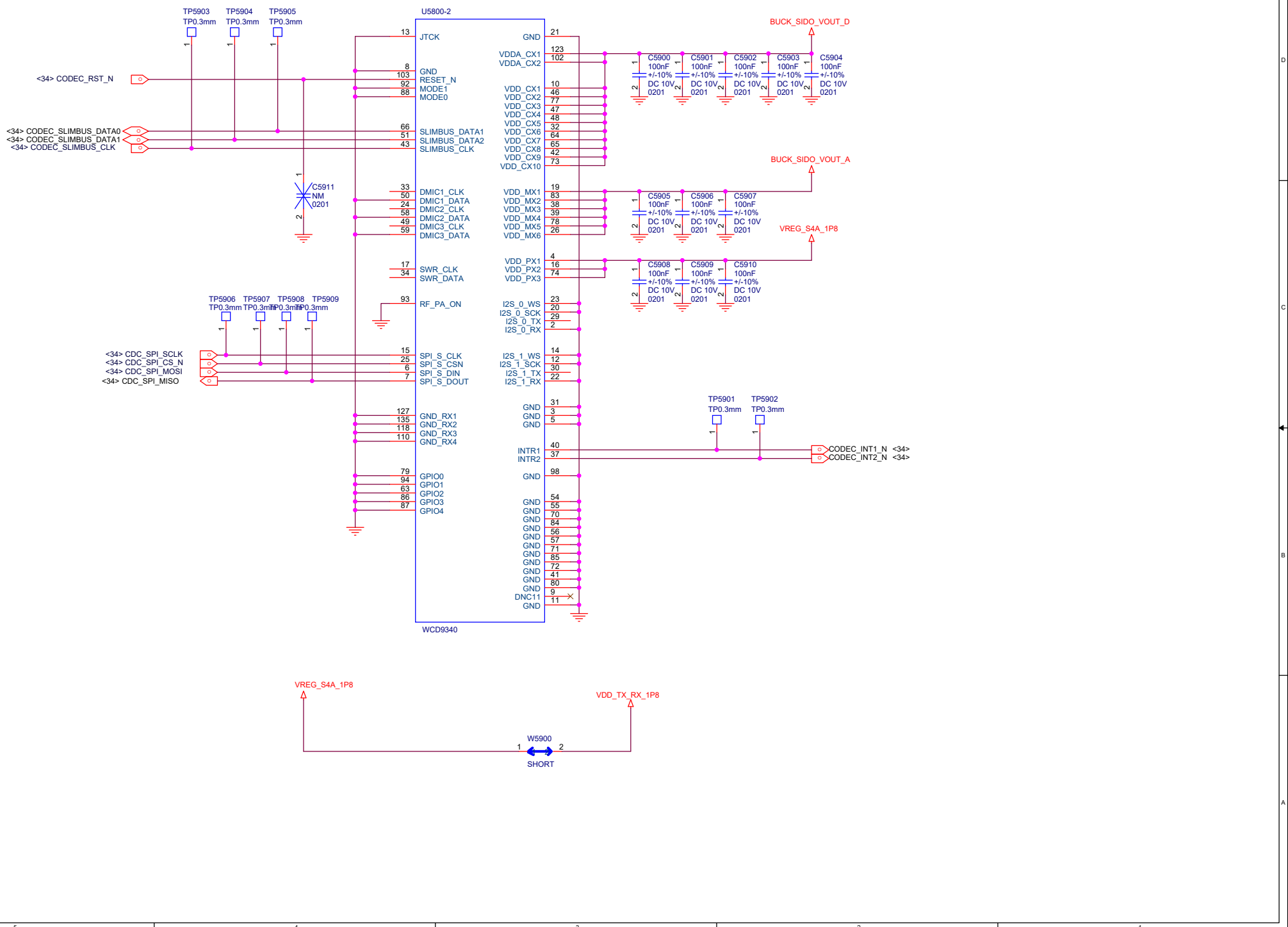
C

B

B

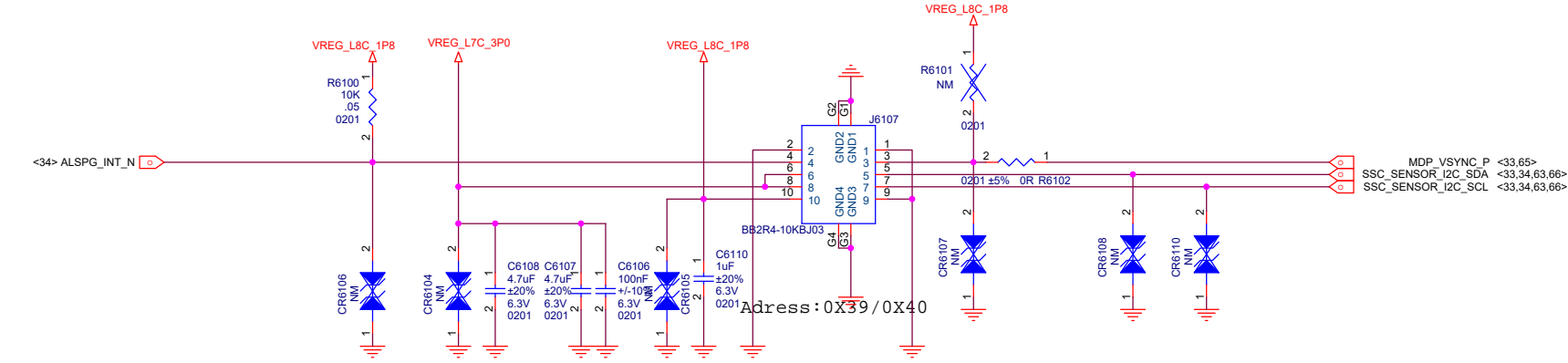
A

A

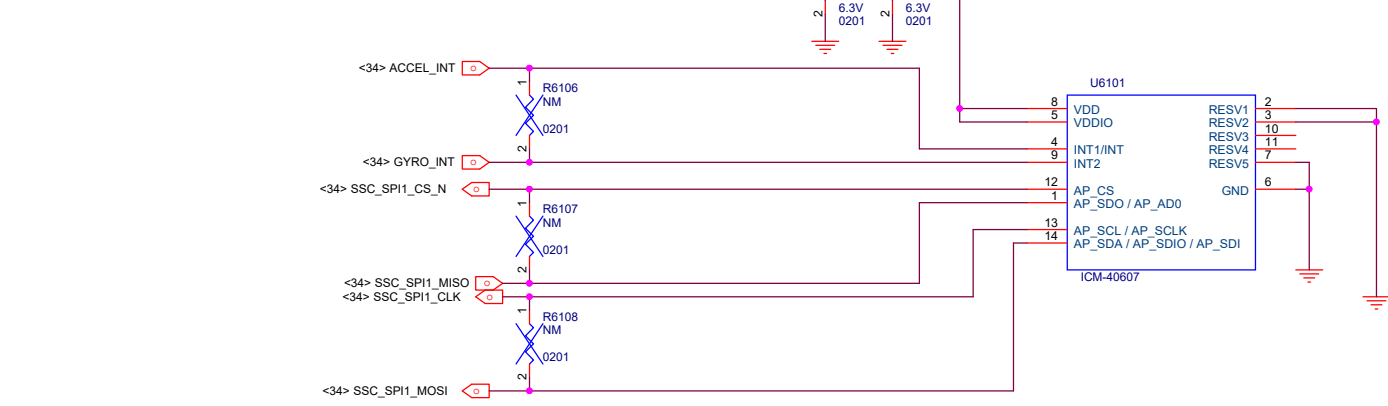




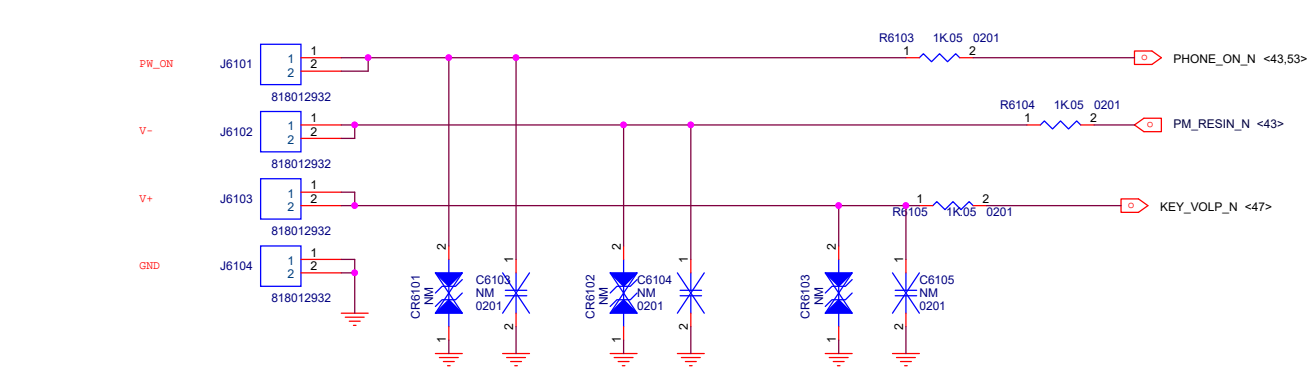
P&L-sensor



A+G

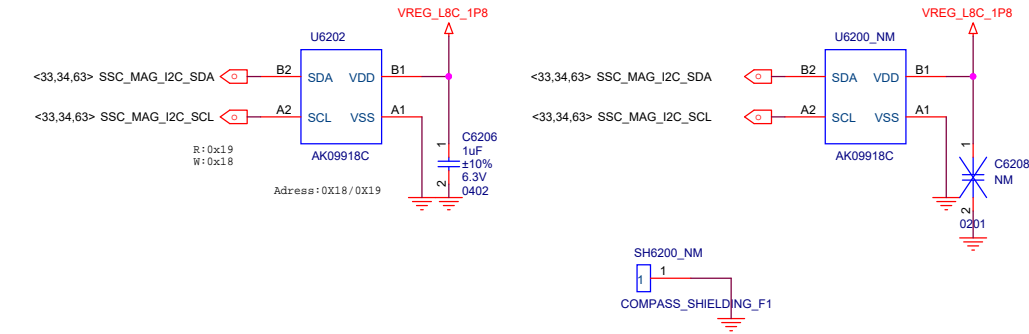


Sidekey

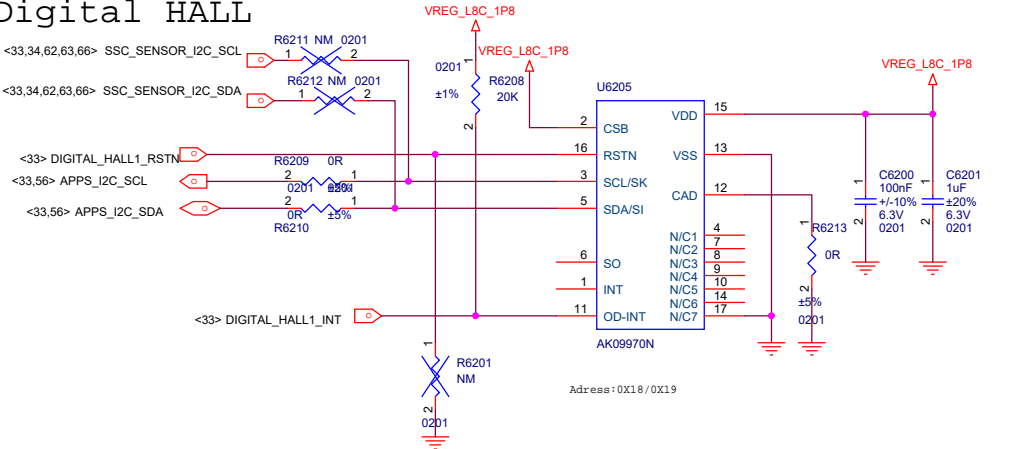


FingerPrint to SUB board

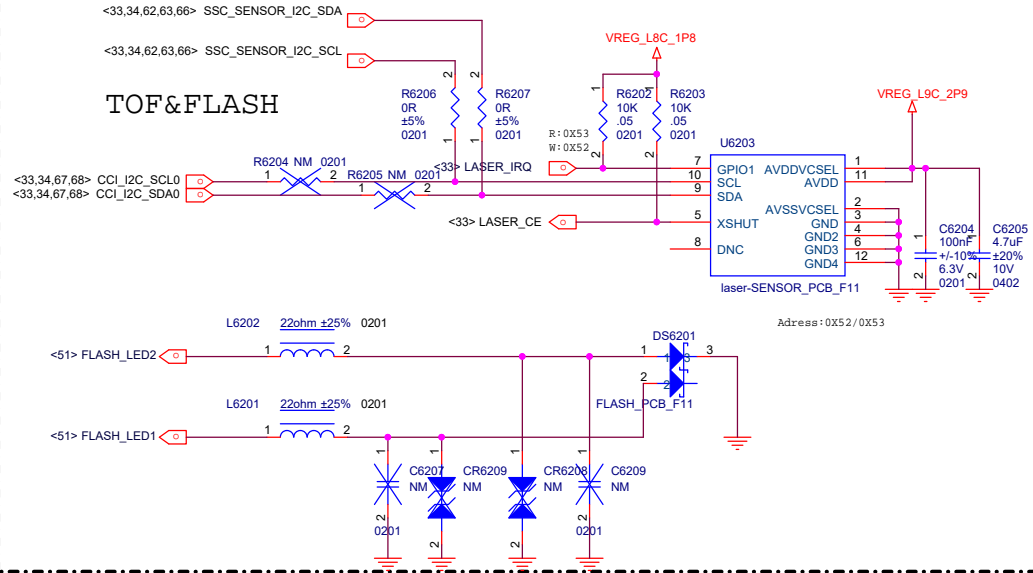
COMPASS



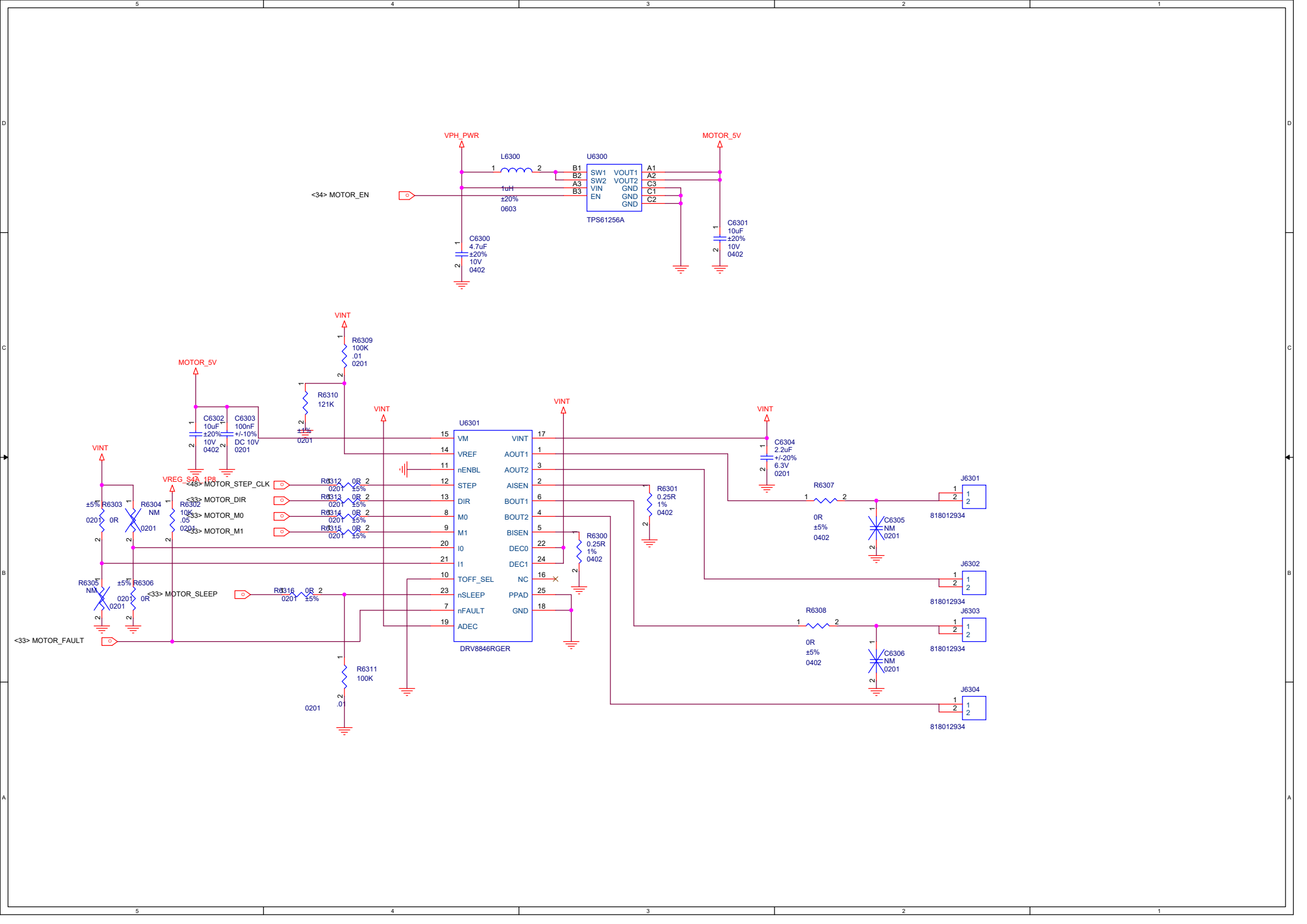
Digital HALL



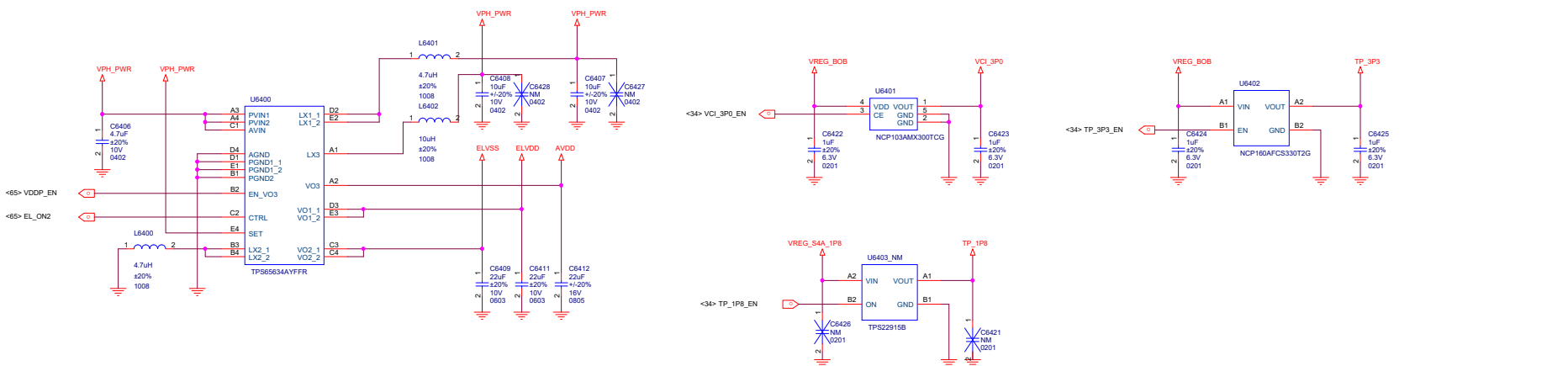
TOF&FLASH



HALL

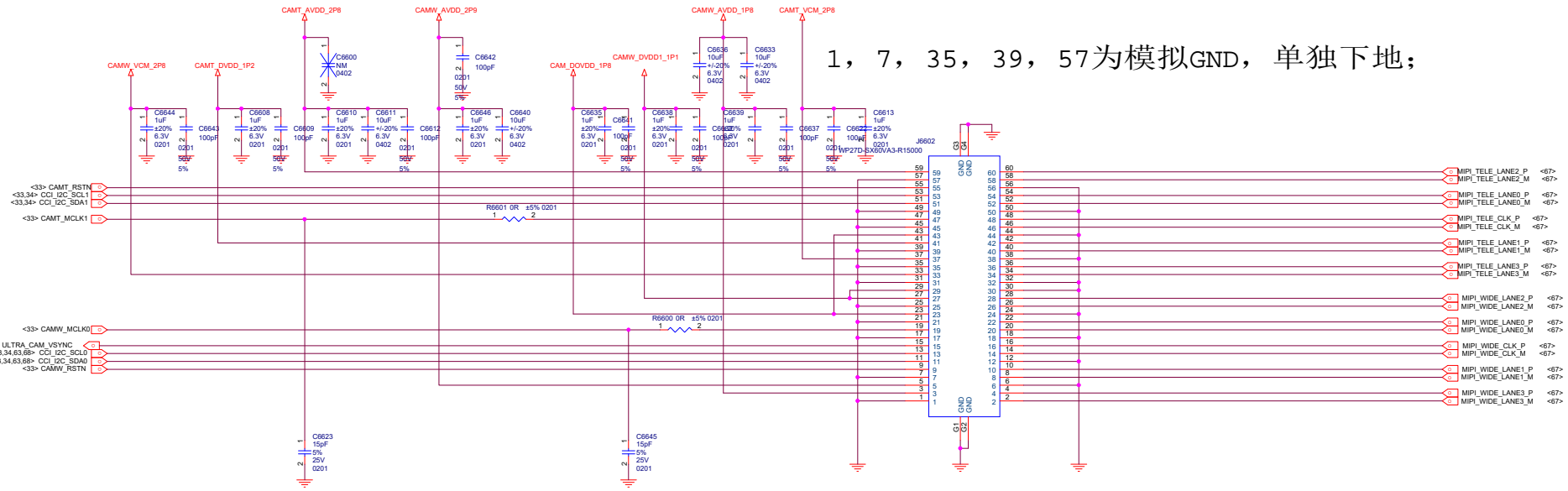


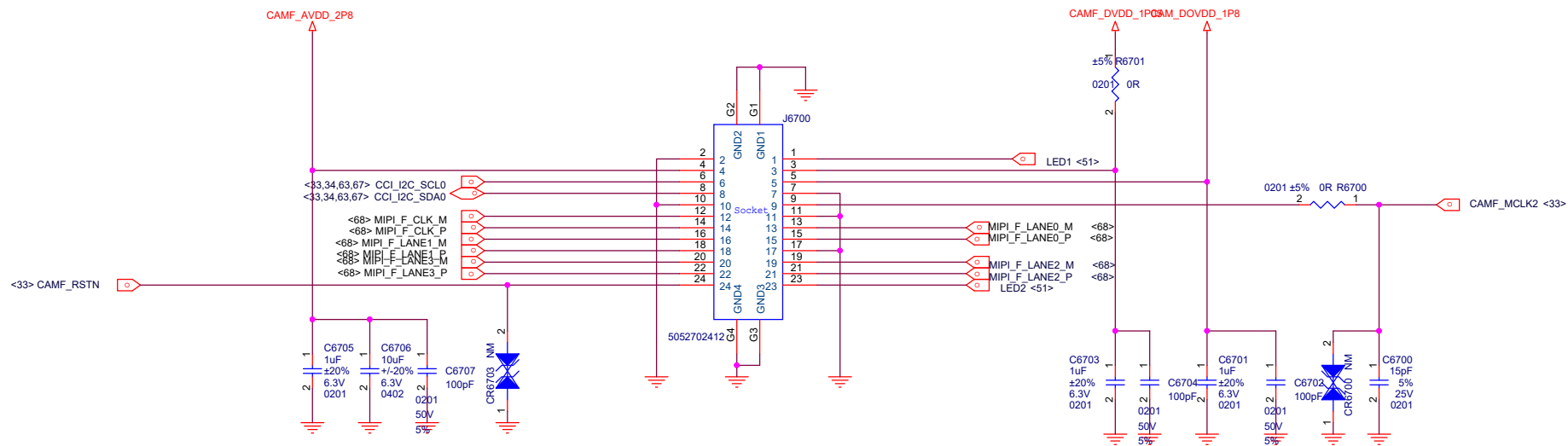


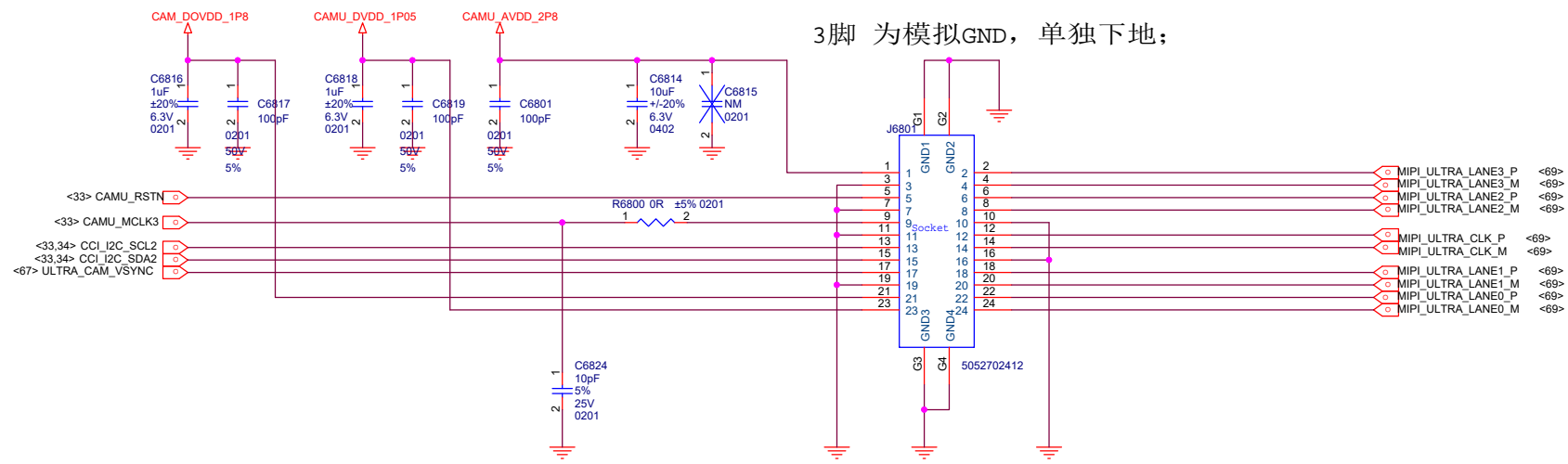




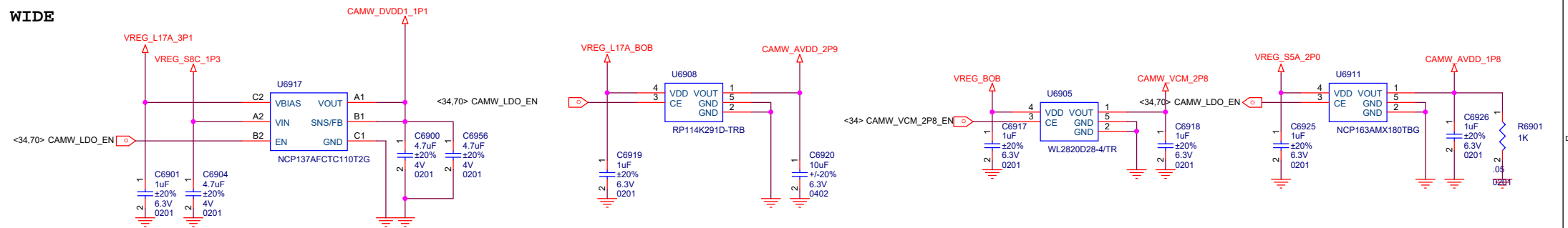
1, 7, 35, 39, 57为模拟GND, 单独下地;



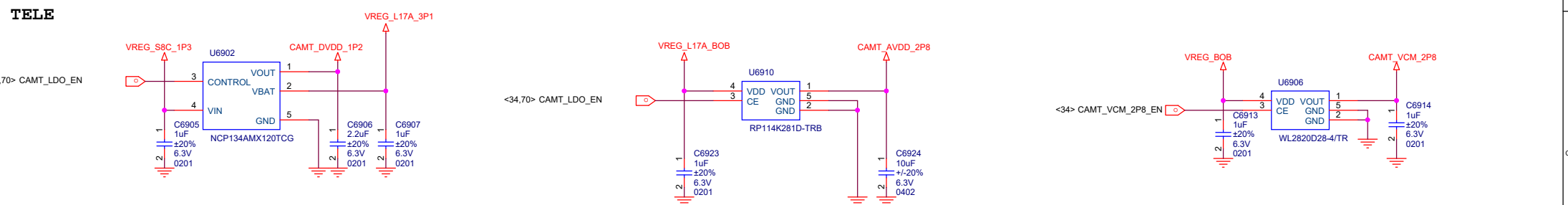




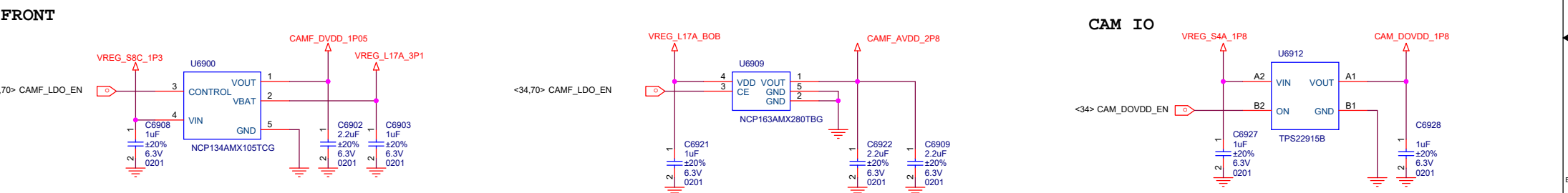
## WIDE



## TELE



## FRONT



## ULTRA

