

[illegible]

Revision History

REV	DESCRIPTION
A	EVT2.0 Initial release

Board Change History

SCHEMATIC MCN	HW VERSION	REVISION	DESCRIPTION OF CHANGE
LD20-P3555	EVT1.1	A	EVT1.1 pre-liminary release
LD20-P4374	EVT2.0	A	EVT2.0 Initial release, the details refer to EVT2.0 change list in "Change list" page

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Revision History

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Title

Draw Name

Date

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Rev

RF Topology

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Block Diagram

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Title		
Drawn	By	Rev
Date: _____ Sheet _____ of _____		

MSM8953 GPIO Configuration For QRD8953

GPIO_0	NFC_SPI_ESR_MOSI	GPIO_41		GPIO_82	FM_DATA
GPIO_1	NFC_SPI_ESR_MISO	GPIO_42	ACCL_INT1	GPIO_83	BT_CTL
GPIO_2	NFC_SPI_ESR_CS_N	GPIO_43	ALSP_INT_N	GPIO_84	BT_DATA
GPIO_3	NFC_SPI_ESR_CLK	GPIO_44	MAG_DRDY_INT	GPIO_85	KEY_VOL_UP_N
GPIO_4	UART_MSM_TX	GPIO_45	GYRO_INT	GPIO_86	
GPIO_5	UART_MSM_RX	GPIO_46	SCAM_D_ELDO_EN	GPIO_87	
GPIO_6		GPIO_47	SENSOR_SPI_CS2_N	GPIO_88	
GPIO_7		GPIO_48	FP_INT_N	GPIO_89	
GPIO_8		GPIO_49	UIM_BATT_ALARM	GPIO_90	
GPIO_9		GPIO_50	WCD_ELDO_EN	GPIO_91	
GPIO_10	TP_I2C_SDA	GPIO_51	UIM1_DATA	GPIO_92	
GPIO_11	TP_I2C_SCL	GPIO_52	UIM1_CLK	GPIO_93	SCAM_ID
GPIO_12		GPIO_53	UIM1_RESET	GPIO_94	
GPIO_13		GPIO_54		GPIO_95	
GPIO_14	SENSOR_I2C_SDA	GPIO_55	UIM2_DATA	GPIO_96	WSA_EN
GPIO_15	SENSOR_I2C_SCL	GPIO_56	UIM2_CLK	GPIO_97	
GPIO_16	NFC_DISABLE	GPIO_57	UIM2_RESET	GPIO_98	
GPIO_17	NFC_IRQ	GPIO_58		GPIO_99	
GPIO_18	NFC_I2C_SDA	GPIO_59		GPIO_100	GRFC0_SEL
GPIO_19	NFC_I2C_SCL	GPIO_60	GP_PDM_A0	GPIO_101	GRFC1_SEL
GPIO_20	SENSOR_SPI_MOSI	GPIO_61	LCD_RST_N	GPIO_102	GRFC2_SEL
GPIO_21	SENSOR_SPI_MISO	GPIO_62	NFC_DWL_REQ	GPIO_103	GRFC3_SEL
GPIO_22	SENSOR_SPI_CS0_N	GPIO_63		GPIO_104	GRFC4_SEL
GPIO_23	SENSOR_SPI_CLK	GPIO_64	TP_RST_N	GPIO_105	GRFC5_SEL
GPIO_24	LCD_TE0	GPIO_65	TP_INT_N	GPIO_106	WDOG_DISABLE
GPIO_25		GPIO_66		GPIO_107	GRFC7_SEL
GPIO_26	CAM_MCLK0	GPIO_67	WCD_RST_N	GPIO_108	GRFC8_SEL
GPIO_27	CAM_MCLK1	GPIO_68		GPIO_109	GRFC9_SEL
GPIO_28		GPIO_69	WCD_MSM_MCLK	GPIO_110	
GPIO_29	CAM_I2C_SDA0	GPIO_70	SLIMBUS_CLK	GPIO_111	
GPIO_30	CAM_I2C_SCL0	GPIO_71	SLIMBUS_DATA0	GPIO_112	
GPIO_31	CAM_I2C_SDA1	GPIO_72		GPIO_113	
GPIO_32	CAM_I2C_SDA1	GPIO_73	WCD_INTR1	GPIO_114	
GPIO_33		GPIO_74	WCD_INTR2	GPIO_115	
GPIO_34	FLASH_STROBE_NOW	GPIO_75	BT_SSB1	GPIO_116	EXT_GPS_LINA_EN
GPIO_35		GPIO_76	WL_CMD_DATA_2	GPIO_117	CH0_GSM_TX_PHASE_D0
GPIO_36		GPIO_77	WL_CMD_DATA_1	GPIO_118	RFFE1_CLK
GPIO_37	FORCE_USB_BOOT	GPIO_78	WL_CMD_DATA_0	GPIO_119	RFFE1_DATA
GPIO_38		GPIO_79	WL_CMD_SET	GPIO_120	RFFE2_CLK
GPIO_39	MCAM_PWD_N	GPIO_80	WL_CMD_CLK	GPIO_121	RFFE2_DATA
GPIO_40	MCAM_RST_N	GPIO_81	FM_SSB1	GPIO_122	RFFE4_CLK

GPIO_123	RFFE4_DATA	GPIO_134	
GPIO_124		GPIO_135	FP_SPI_CLK
GPIO_125		GPIO_136	FP_SPI_CS
GPIO_126	RFFE3_CLK	GPIO_137	FP_SPI_MOSI
GPIO_127	RFFE3_DATA	GPIO_138	FP_SPI_MISO
GPIO_128		GPIO_139	USB_SS_SEL
GPIO_129	SCAM_RST_N	GPIO_140	FP_RST_N
GPIO_130	SCAM_PWD_N	GPIO_141	NFC_ESR_PWR_REQ
GPIO_131			
GPIO_132			
GPIO_133	SDCARD_DET_N		

PMI8952 GPIO/MPP Configuration For QRD8953

GPIO_1		MPP_1	
GPIO_2		MPP_2	GREEN_LED
		MPP_3	
		MPP_4	FLASH_STROBE_NOW

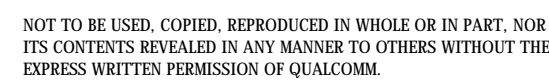
PM8953 GPIO/MPP Configuration For QRD8953

GPIO_1	CODEC_DIV_CLK	MPP_1	VDD_PX_BIAS_MPP_1
GPIO_2	NFC_CLK_REQ (SDCARD_DET_N)	MPP_2	PA_THERM1
GPIO_3	UIM_BATT_ALARM	MPP_3	VREF_DAC_MPP_3
GPIO_4		MPP_4	QUIET_THERM
GPIO_5			
GPIO_6			
GPIO_7	VBUS_USB_IN		
GPIO_8	USB_ID		

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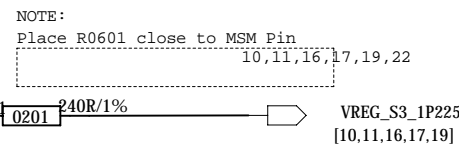
GPIO TABLE

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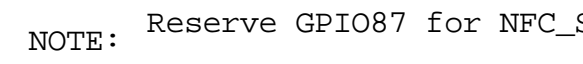


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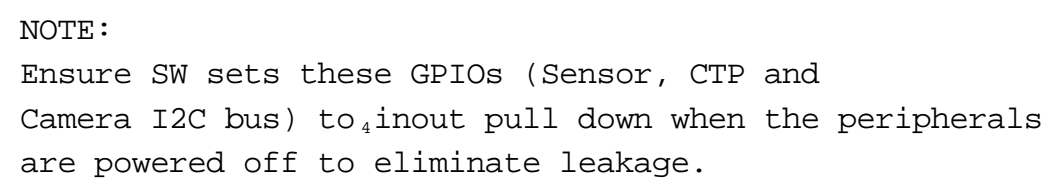


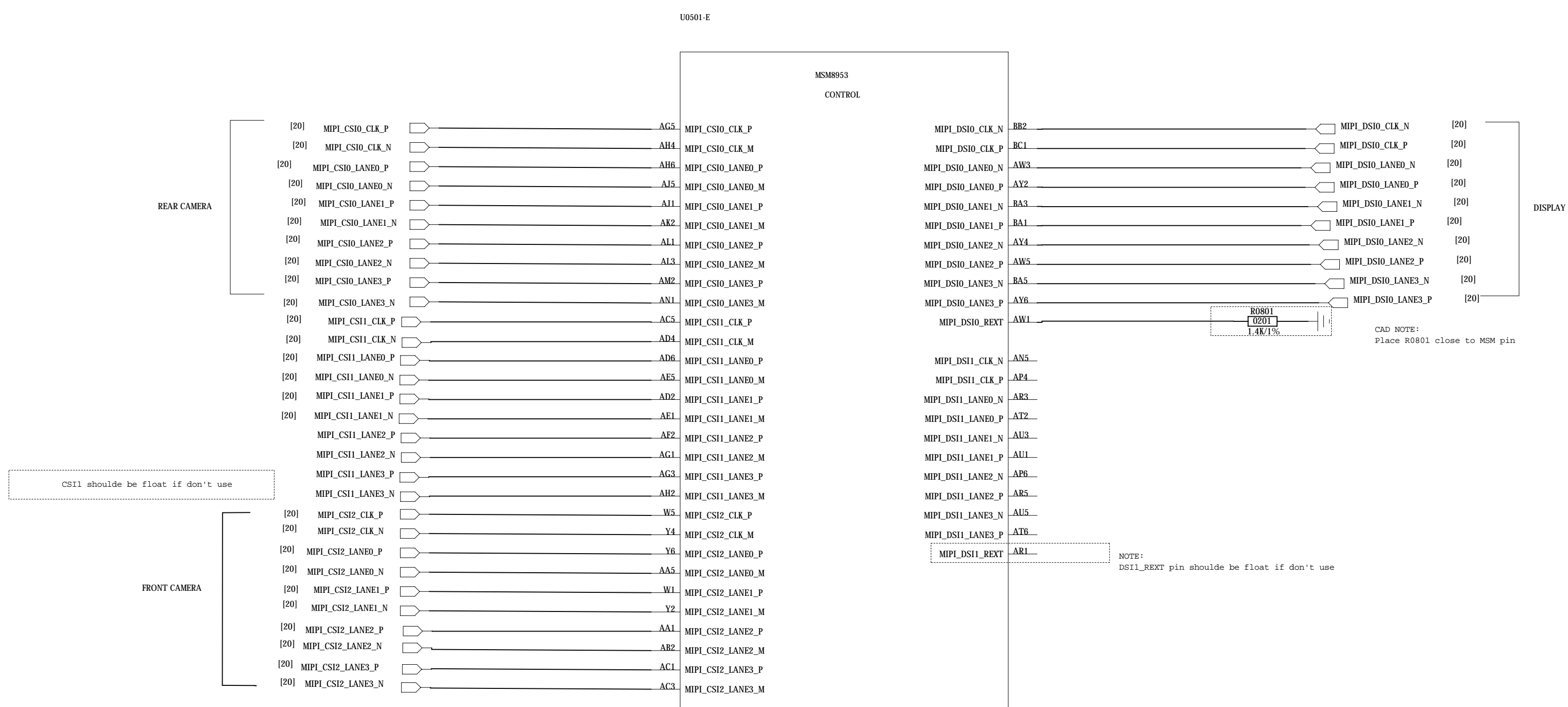
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BOOT_CONFIG[3+1]	BOOT_CONFIG
0x00	SDC1 -> SDC2 -> USB2.0
0x01	SDC2 -> SDC1 -> USB2.0
0x10	SDC1 -> USB2.0
0x11	USB2.0

MSM8953 GPIO



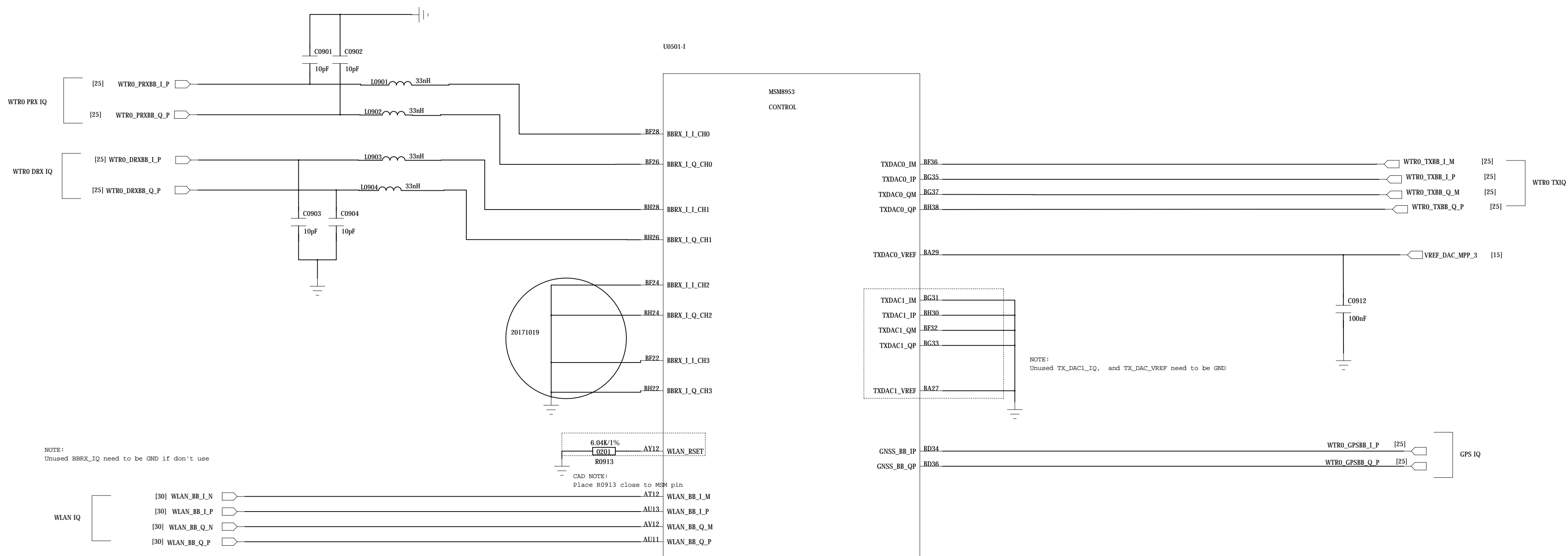


CSI Pin Name	CSI DPHY 4-lane	CSI DPHY 2+1 Mode	CSI CPHY 3Phase Mode
CSI0_3PHASE_PIN0	CSI0_CLKP	CSI0_2LANE_CLKP	NC
CSI0_3PHASE_PIN1	CSI0_CLKN	CSI0_2LANE_CLKN	CSI0_TRI0_A
CSI0_3PHASE_PIN2	CSI0_DP0	CSI0_2LANE_DP0	CSI0_TRI0_B
CSI0_3PHASE_PIN3	CSI0_DN0	CSI0_2LANE_DN0	CSI0_TRI0_C
CSI0_3PHASE_PIN4	CSI0_DP1	CSI0_2LANE_DP1	CSI0_TRI1_A
CSI0_3PHASE_PIN5	CSI0_DN1	CSI0_2LANE_DN1	CSI0_TRI1_B
CSI0_3PHASE_PIN6	CSI0_DP2	CSI0_1LANE_DP0	CSI0_TRI1_C
CSI0_3PHASE_PIN7	CSI0_DN2	CSI0_1LANE_DN0	CSI0_TRI2_A
CSI0_3PHASE_PIN8	CSI0_DP3	CSI0_1LANE_CLKP	CSI0_TRI2_B
CSI0_3PHASE_PIN9	CSI0_DN3	CSI0_1LANE_CLKN	CSI0_TRI2_C
CSI1_3PHASE_PIN1	CSI1_CLKN	CSI1_2LANE_CLKN	CSI1_TRI0_A
CSI1_3PHASE_PIN2	CSI1_DP0	CSI1_2LANE_DP0	CSI1_TRI0_B
CSI1_3PHASE_PIN3	CSI1_DN0	CSI1_2LANE_DN0	CSI1_TRI0_C
CSI1_3PHASE_PIN4	CSI1_DP1	CSI1_2LANE_DP1	CSI1_TRI1_A
CSI1_3PHASE_PIN5	CSI1_DN1	CSI1_2LANE_DN1	CSI1_TRI1_B
CSI1_3PHASE_PIN6	CSI1_DP2	CSI1_1LANE_DP0	CSI1_TRI1_C
CSI1_3PHASE_PIN7	CSI1_DN2	CSI1_1LANE_DN0	CSI1_TRI2_A
CSI1_3PHASE_PIN8	CSI1_DP3	CSI1_1LANE_CLKP	CSI1_TRI2_B
CSI1_3PHASE_PIN9	CSI1_DN3	CSI1_1LANE_CLKN	CSI1_TRI2_C
CSI2_3PHASE_PIN1	CSI2_CLKN	CSI2_2LANE_CLKN	CSI2_TRI0_A
CSI2_3PHASE_PIN2	CSI2_DP0	CSI2_2LANE_DP0	CSI2_TRI0_B
CSI2_3PHASE_PIN3	CSI2_DN0	CSI2_2LANE_DN0	CSI2_TRI0_C
CSI2_3PHASE_PIN4	CSI2_DP1	CSI2_2LANE_DP1	CSI2_TRI1_A
CSI2_3PHASE_PIN5	CSI2_DN1	CSI2_2LANE_DN1	CSI2_TRI1_B
CSI2_3PHASE_PIN6	CSI2_DP2	CSI2_1LANE_DP0	CSI2_TRI1_C
CSI2_3PHASE_PIN7	CSI2_DN2	CSI2_1LANE_DN0	CSI2_TRI2_A
CSI2_3PHASE_PIN8	CSI2_DP3	CSI2_1LANE_CLKP	CSI2_TRI2_B
CSI2_3PHASE_PIN9	CSI2_DN3	CSI2_1LANE_CLKN	CSI2_TRI2_C

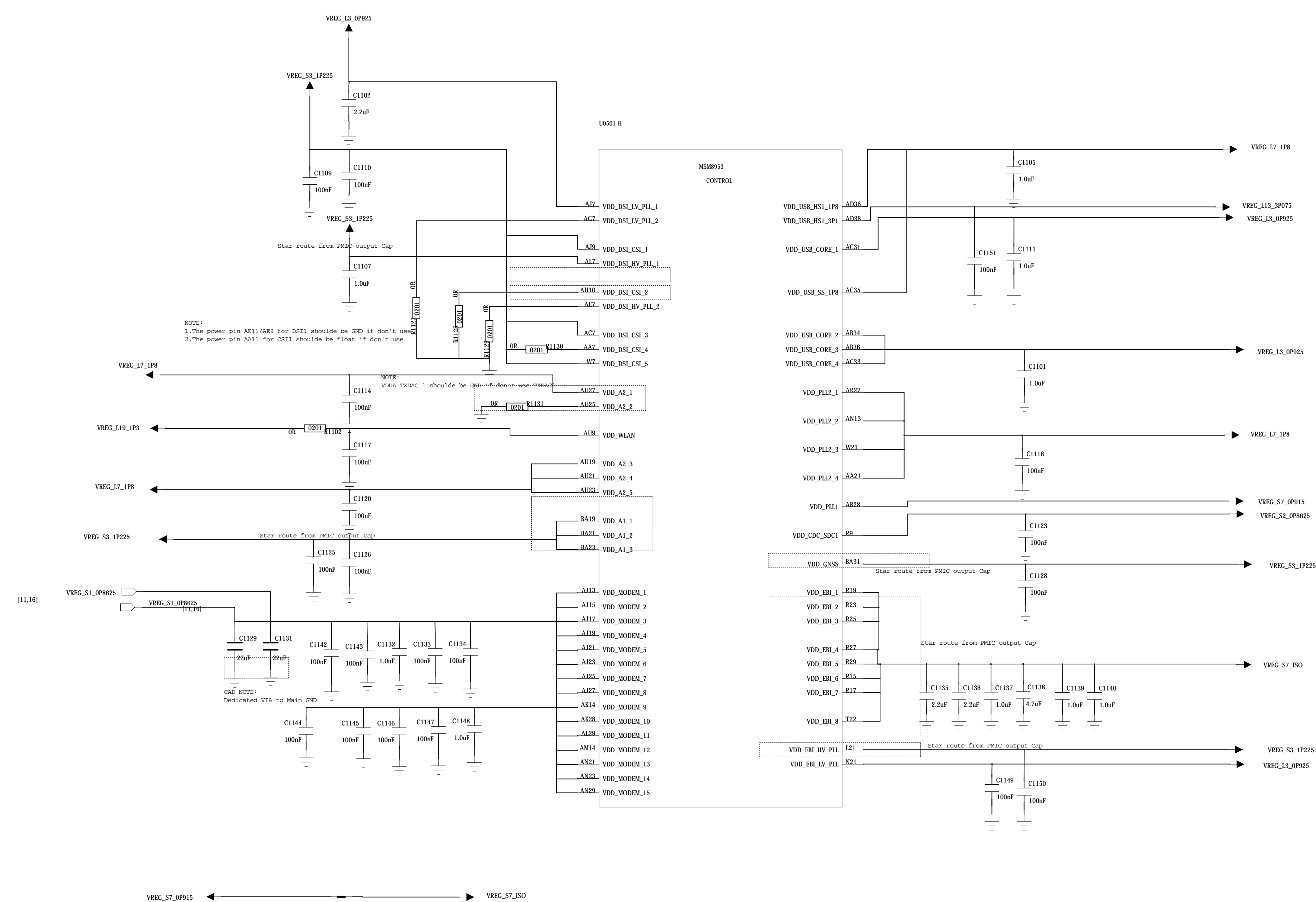
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MSM8953 MIPI

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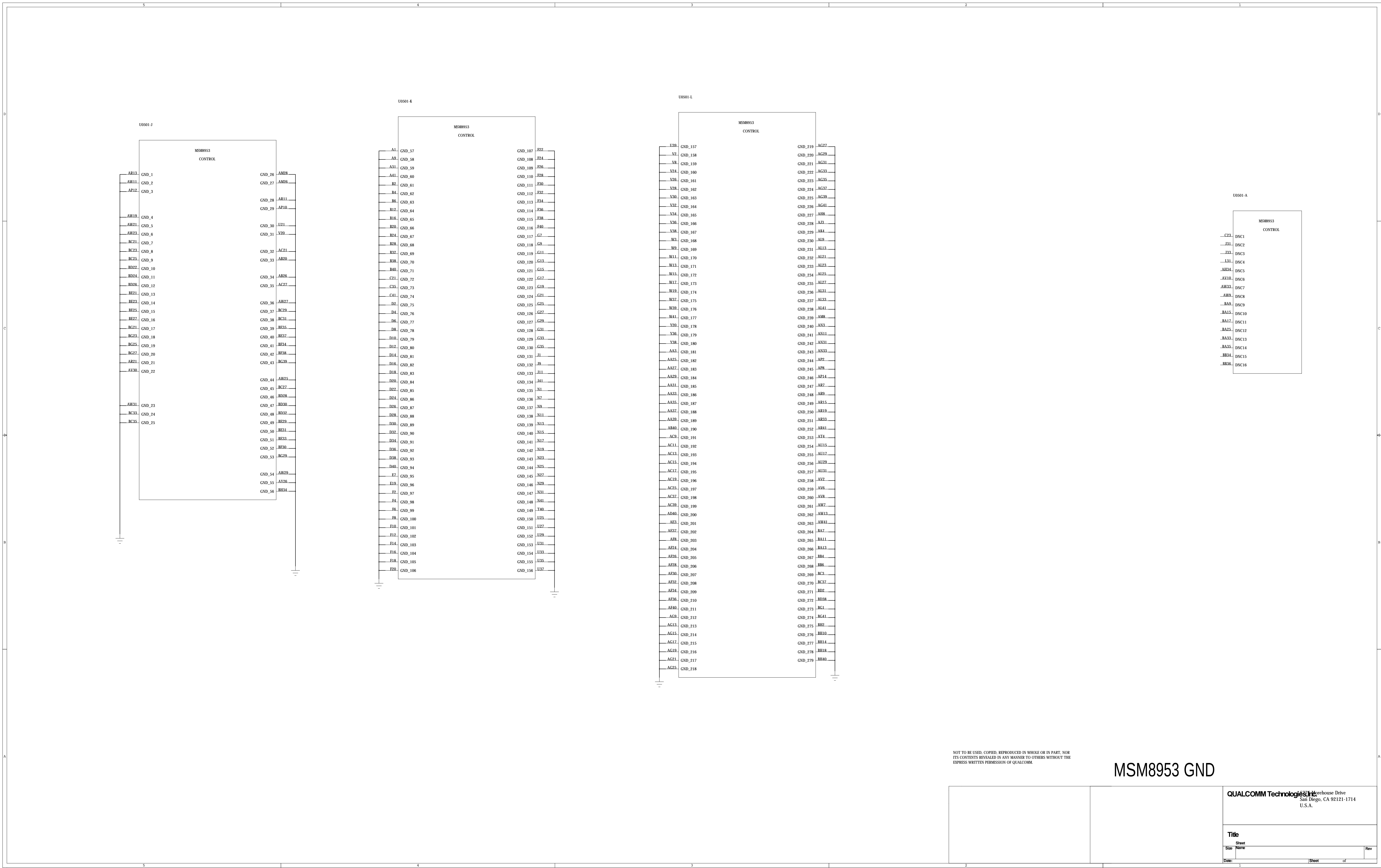
CAD NOTE:
About star route from PMIC output Cap:



MSM8953 POWER2

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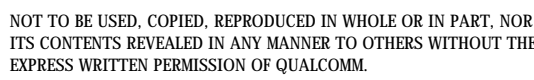
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MSM8953 GND

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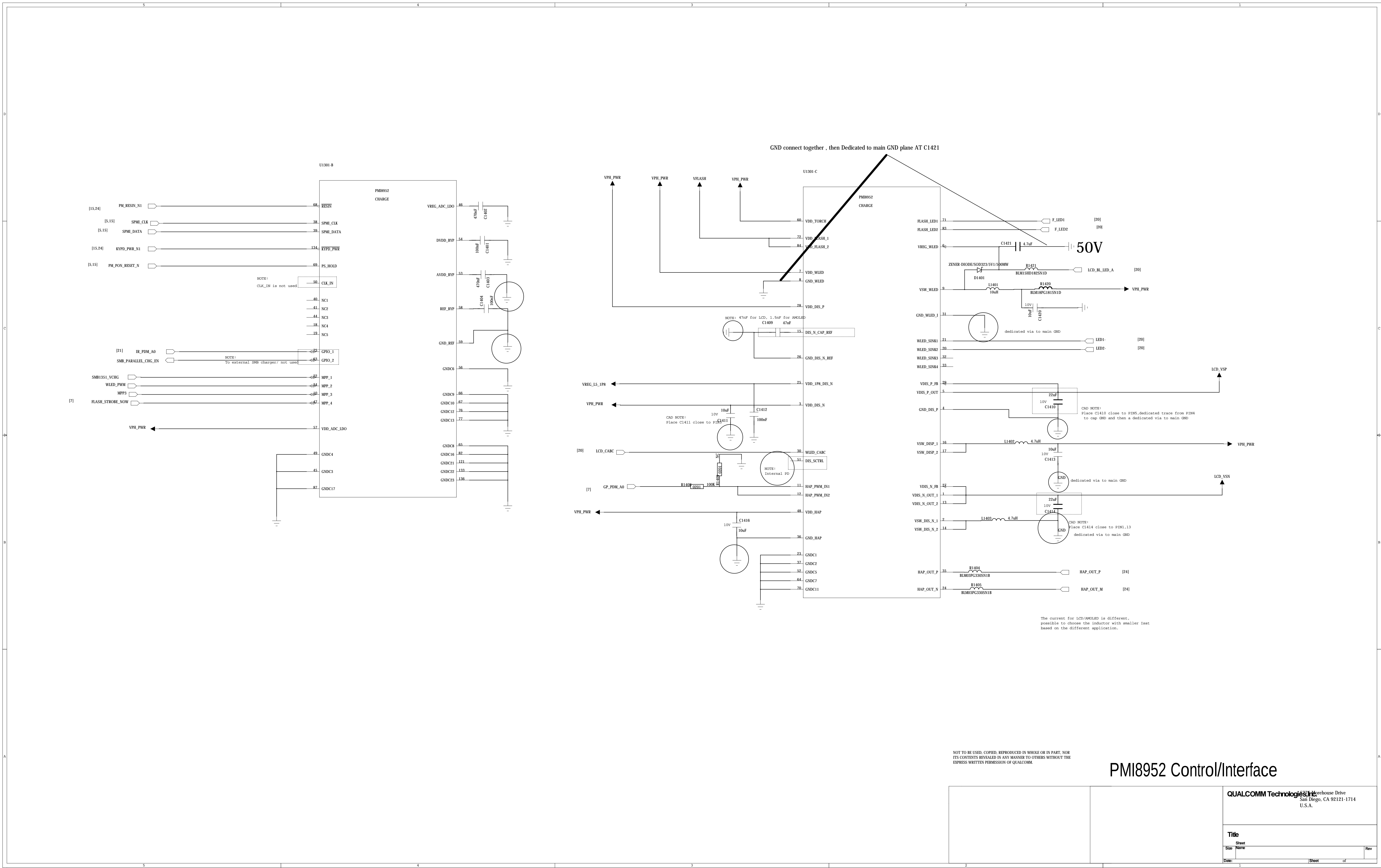
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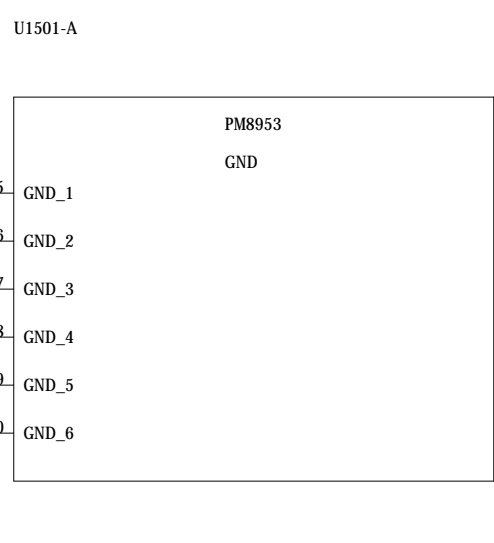
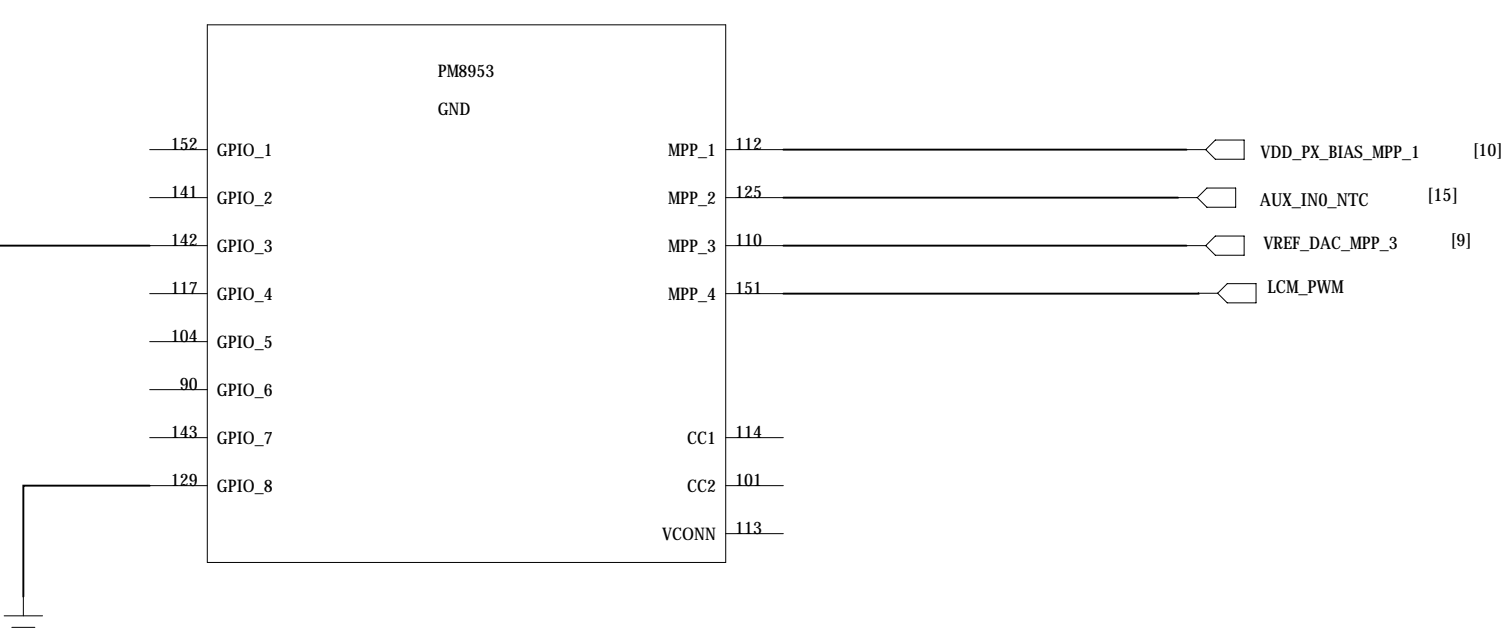
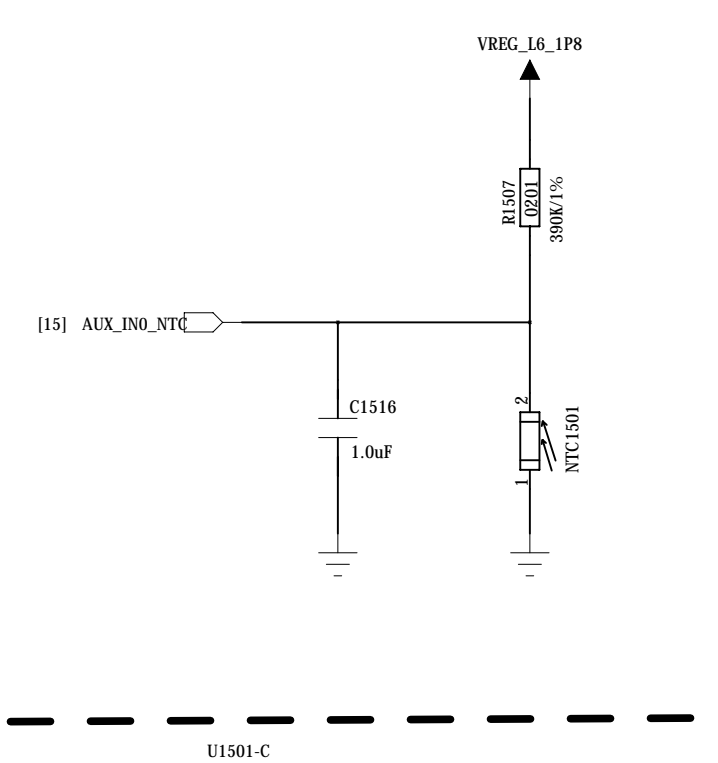
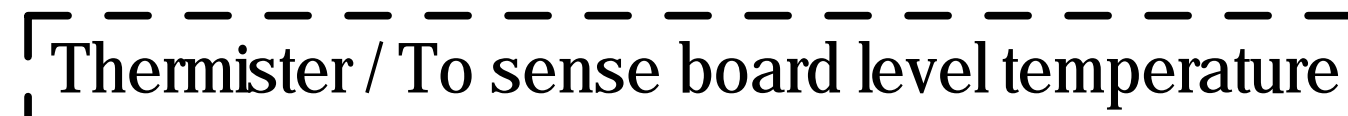
Use C1302= 4.7uF for Single Charging Config
Use C1302 = 2.2uF for Parallel Charging Config



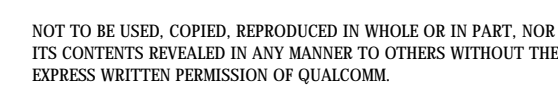
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PM8953 Control/Interface



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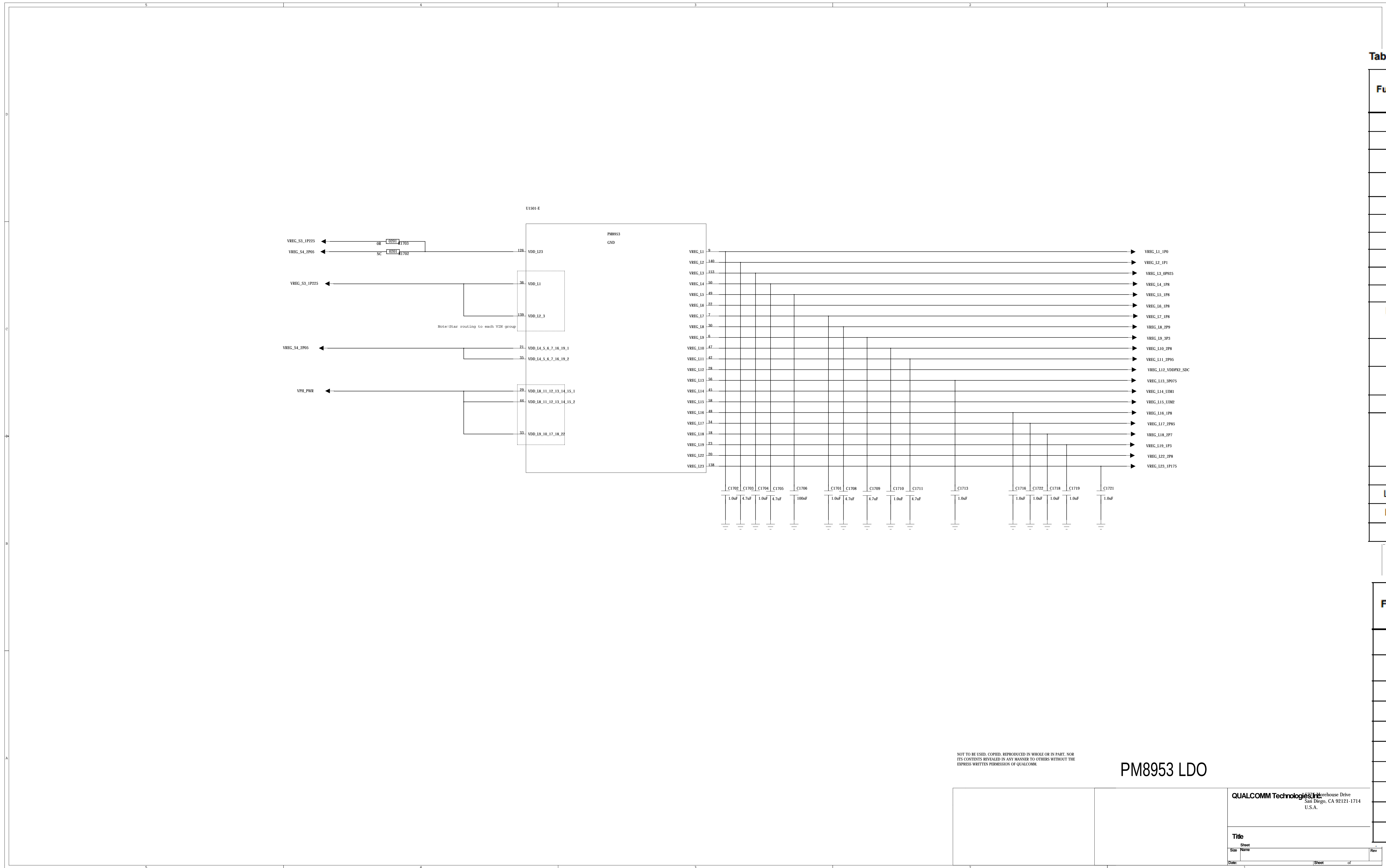
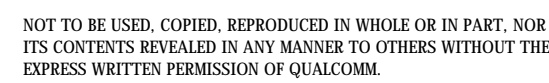


Table 3-6 PM8937/PM8940 regulators and their intended uses

Function	Circuit type	Default V (V) ¹	Specified range (V) ² (MSM8937)	Programmable range (V)	Rated current (mA)	Default on	Expected use
S1	ULT-SMPS	1.225	0.900–1.350	0.375–1.5625	2000 ³	N	MSM modem
S2	ULT-SMPS	1.225	0.550–1.350	0.375–1.5625	3000	Y	MSM core and graphics
S3	HF-SMPS	1.288	1.200–1.4125	0.375–1.5625	2700	Y	Low-voltage LDOs (1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100)
S4	ULT-SMPS	2.050	1.800–2.050	1.550–3.126	2500	Y	High-voltage LDOs (4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100)
S5	FT-SMPS	1.225	1.050–1.350	0.350–1.355	3000	Y	MSM applications processor
S6	FT-SMPS	1.225	1.050–1.350	0.350–1.355	3000	N	MSM applications processor
L1	NMOS LDO	1.000	1.000	0.375–1.5375	1200	N	RFICs
L2	NMOS LDO	1.200	1.200	0.375–1.5375	1200	Y	LPDDR2/LPDDR3, M
L3	NMOS LDO	1.225	0.750–1.350	0.375–1.5375	1200	Y	VDDMX
L4	PMOS LDO	1.800	1.800	1.750–3.3375	450	N	RFICs and GPS eLNA
L5 ⁴	PMOS LDO	1.800	1.800	1.750–3.3375	500	Y	Most digital I/Os, MSM and eMMC
L6	PMOS LDO	1.800	1.800	1.750–3.3375	300	N	MSM DSI PLL and OT display, and sensors
L7	PMOS LDO	1.800	1.800	1.750–3.3375	150	Y	MSM analog and PLL clock driver
L8	PMOS LDO	2.900	2.900	1.750–3.3375	600	Y	eMMC
L9	PMOS LDO	V _{out} = 3.3 V for VBAT > 3.575 V; V _{out} = 3 V for VBAT < 3.575 V	3.000–3.300	1.750–3.3375	600	N	WCN
L10	PMOS LDO	2.8	2.800	1.750–3.3375	150	N	Sensors
L11 ⁵	PMOS LDO	2.950	2.950	1.750–3.3375	800	Y	Micro SD
L12 ⁴	PMOS LDO	2.950	1.800/2.950	1.750–3.3375	150	Y	MSM pad group 2 and
L13	PMOS LDO	3.075	3.075	1.750–3.3375	50	Y	MSM USB and audio

Function	Circuit type	Default V (V) ¹	Specified range (V) ² (MSM8937)	Programmable range (V)	Rated current (mA)	Default on	Expected use
L14 ⁵	PMOS LDO	1.800	1.800/2.925/3.050	1.750–3.3375	50	N	MSM pad group 1 and
L15 ⁵	PMOS LDO	1.800	1.800/2.925/3.050	1.750–3.3375	50	N	MSM pad group 1 and
L16	PMOS LDO	1.800	1.800	1.750–3.3375	5	N	PMIC HK
L17	PMOS LDO	2.850	2.850	1.750–3.3375	600	N	Camera, RF
L18	PMOS LDO	2.700	2.700	1.750–3.3375	150	N	QTI RF fr
L19	NMOS LDO	1.350	1.350	0.375–1.5375	1200	N	MSM ana
L20	Low-noise LDO	1.74	1.74	1.74–3.3375	5	Y	PMIC XO
L21	Low-noise LDO	1.74	1.74	1.74–3.3375	5	Y	PMIC RF
L22	PMOS LDO	2.800	2.800	1.750–3.3375	300	N	Camera -
L23	NMOS LDO	1.3	1.2	0.375–1.5375	300	N	Camera -

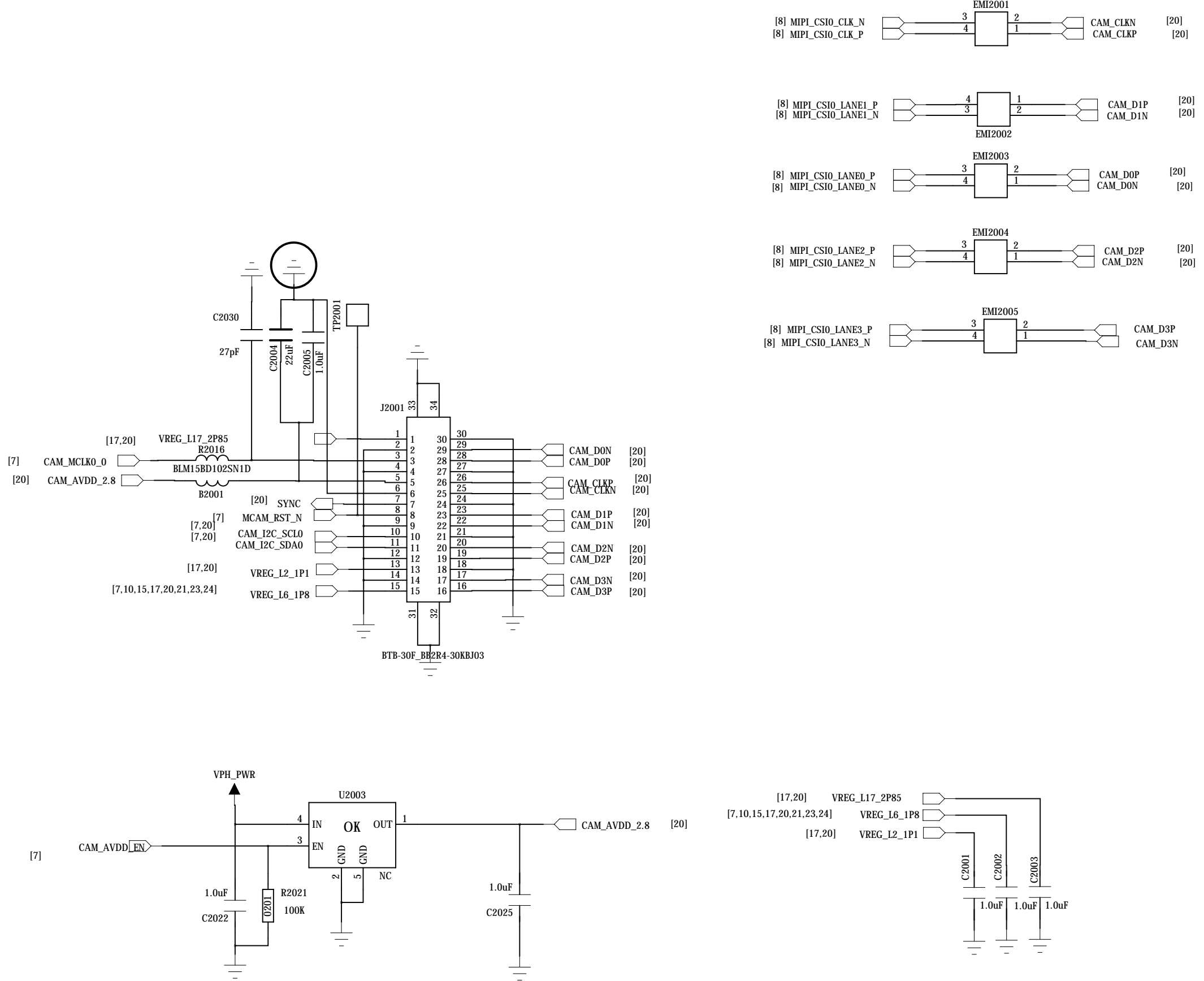


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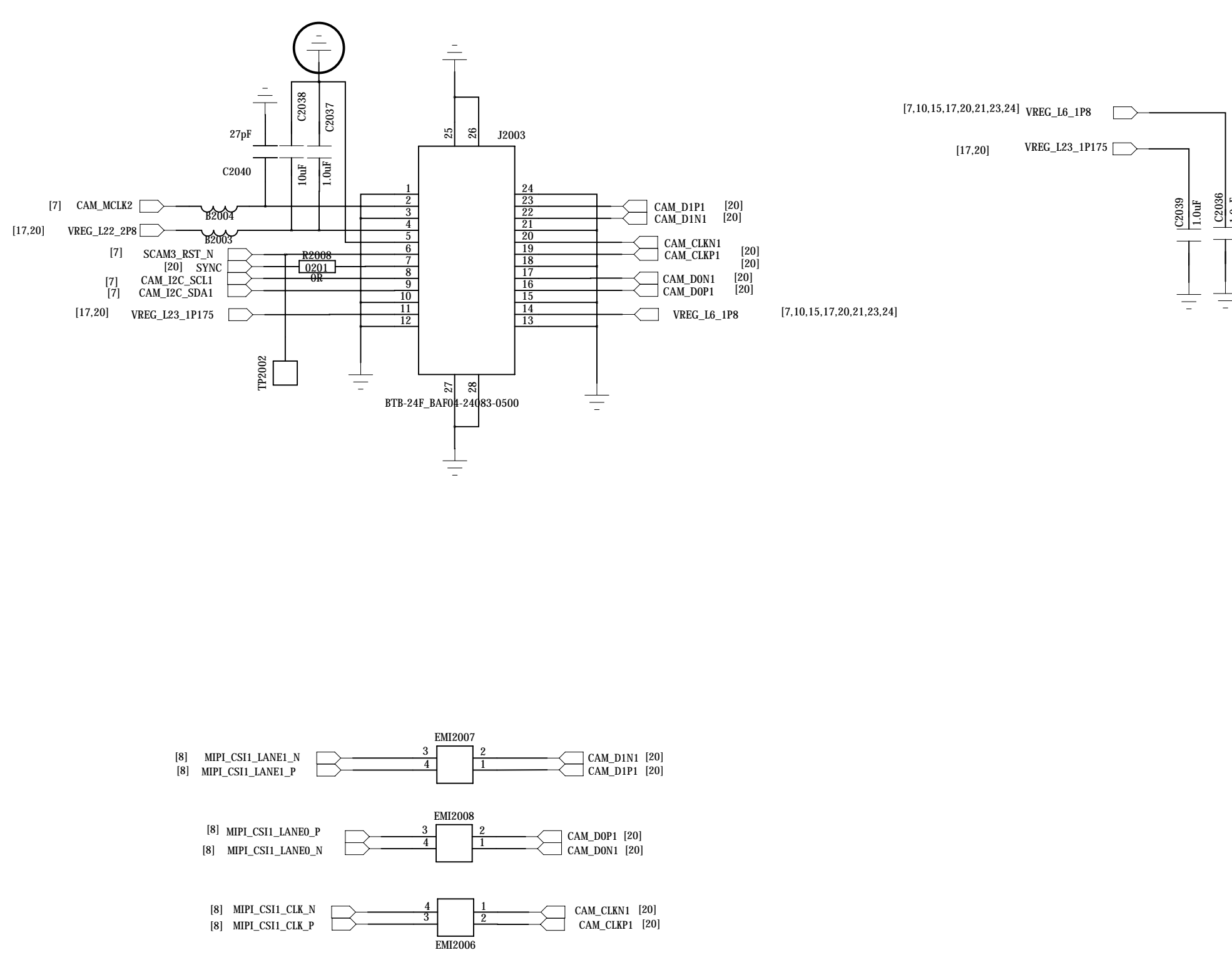
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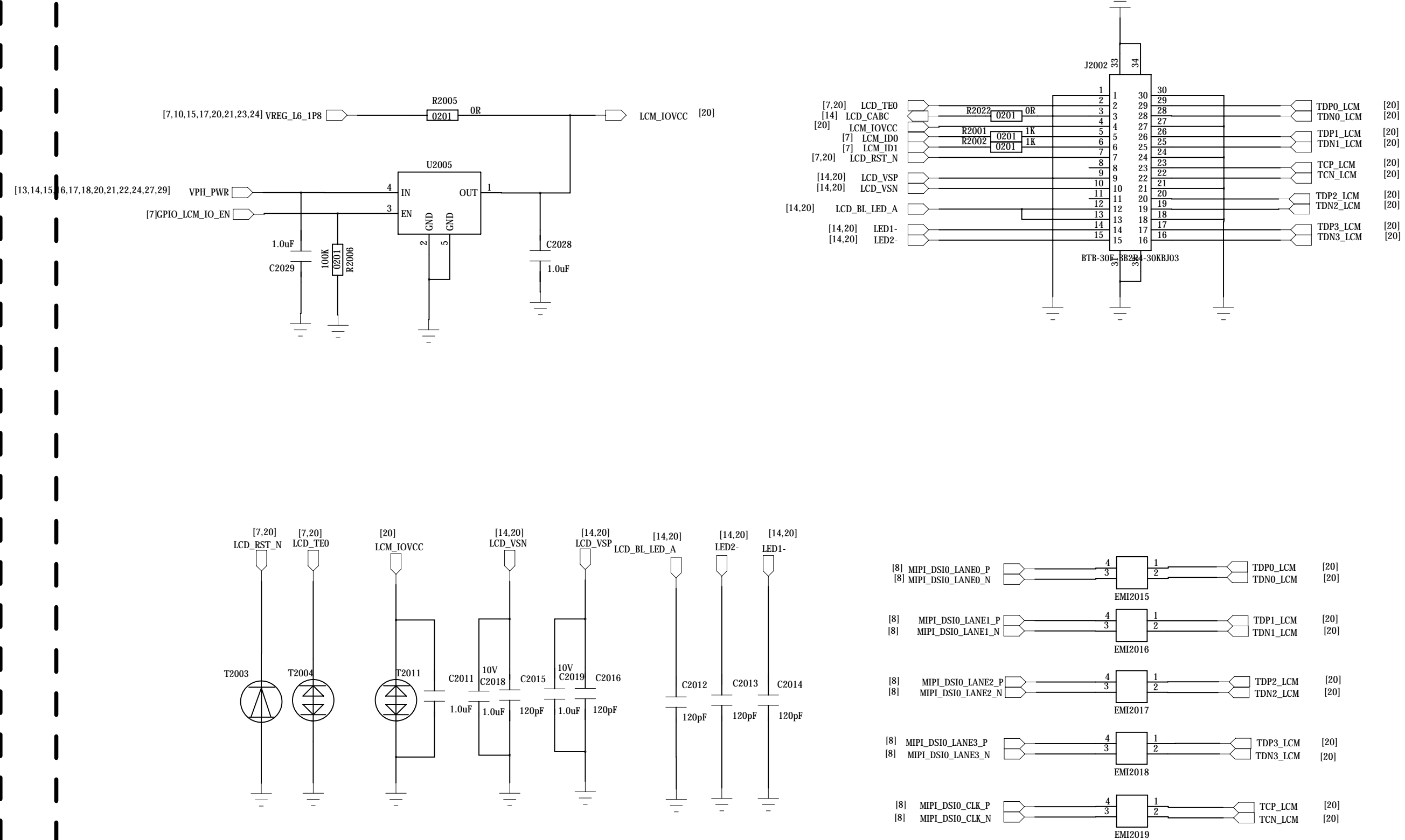
Main Camera A



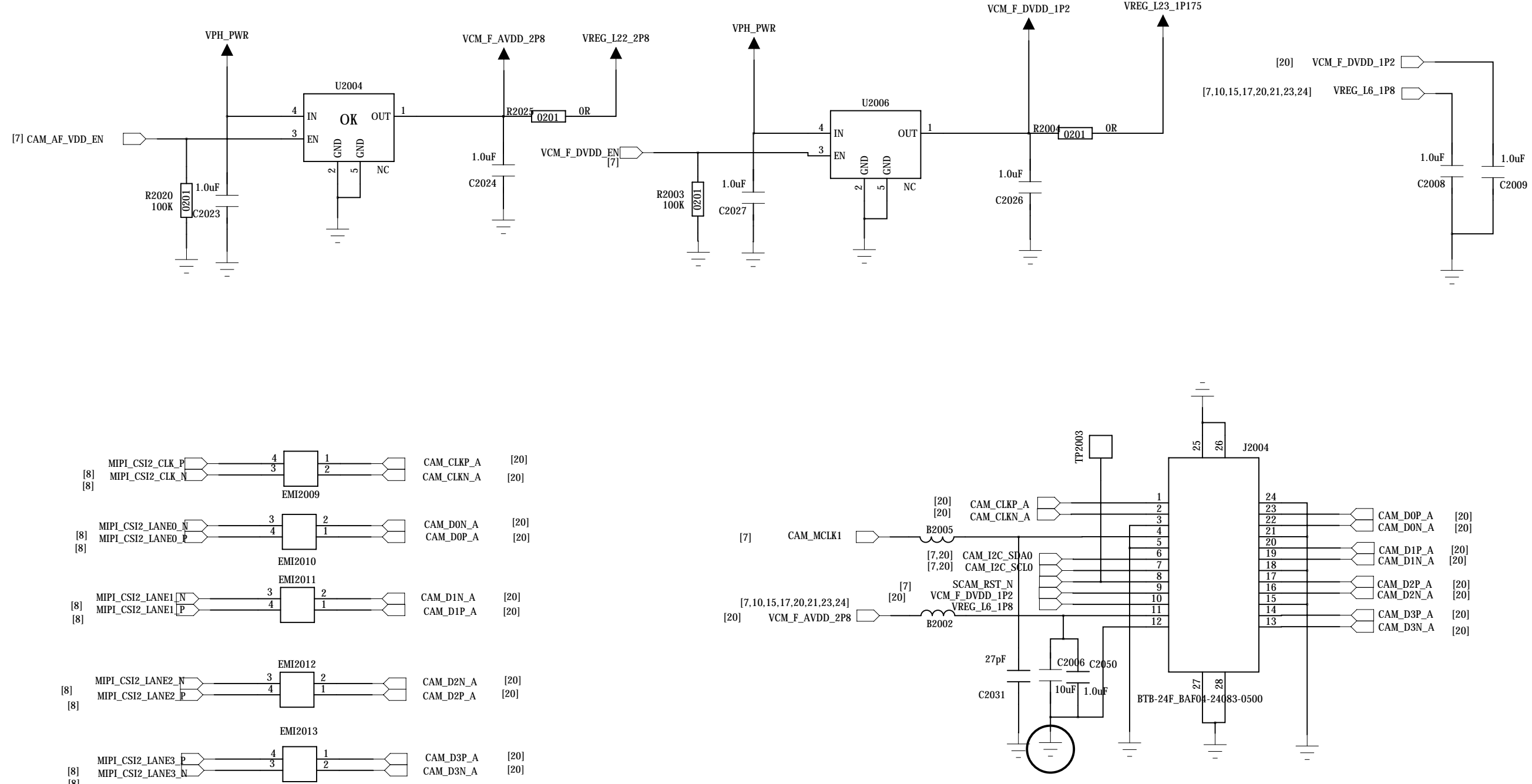
Main Camera B



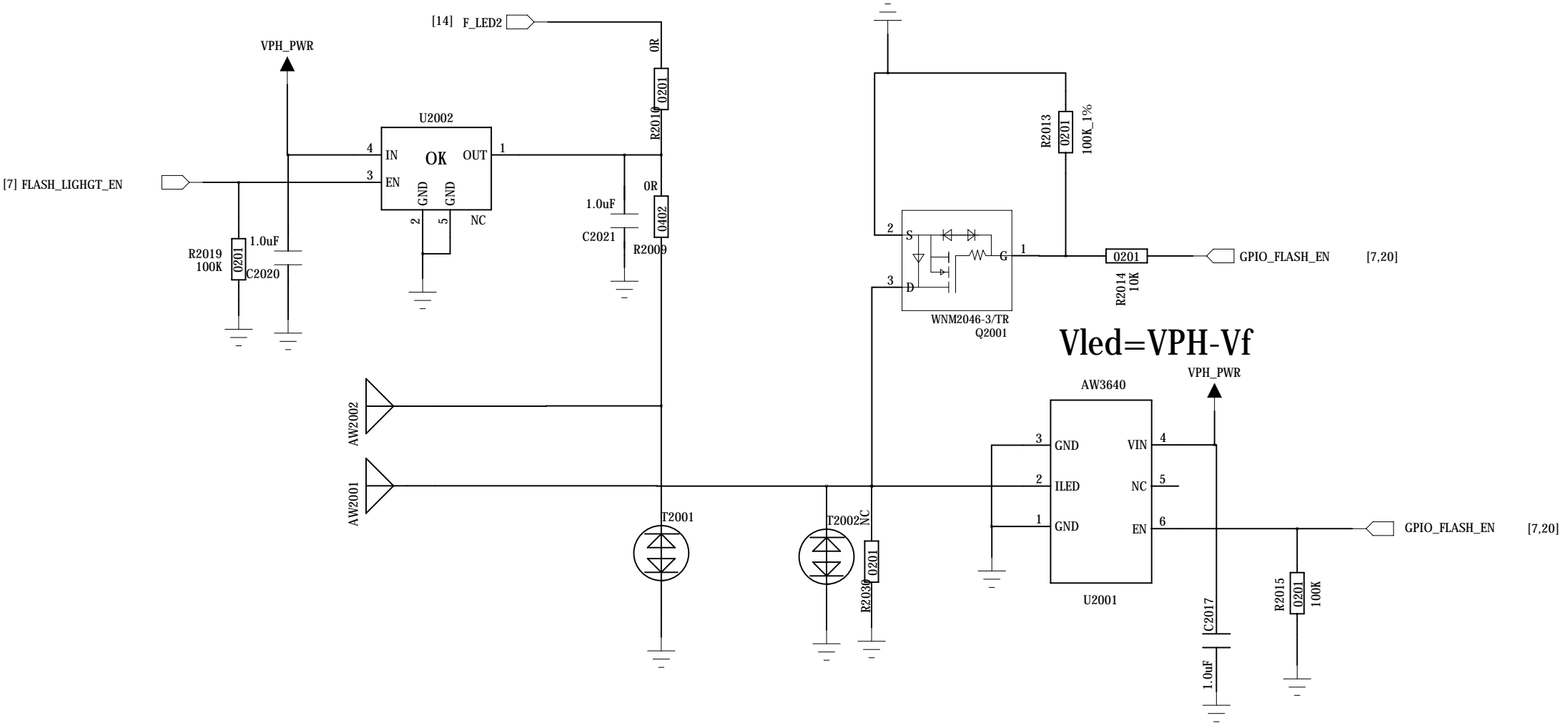
LCM



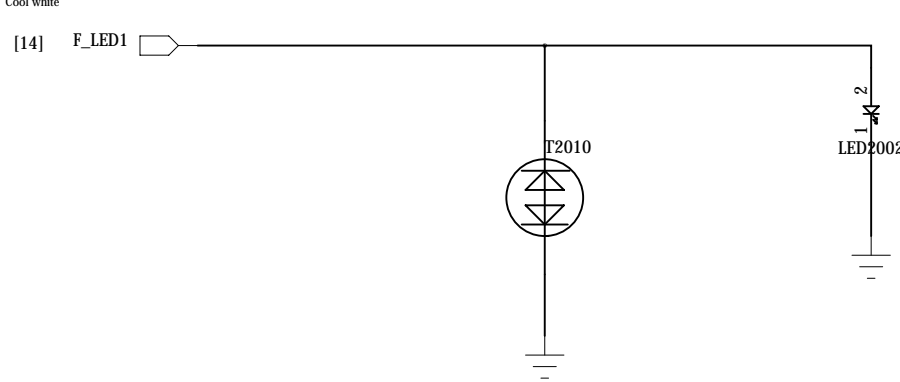
Front Camera



Front FLASHLIGHT



Main FLASHLIGHT



Schematic design notice of "63_PERI_CAMERA_KEYPAD" page.

Note 62-1: The VCC of I2C_0 is pulled to "VCAM_IO_PMU".

Note 62-2: I2C control interface of front camera (with AF) must be assigned to I2C-2 bus when PIP/ATV feature be supported.

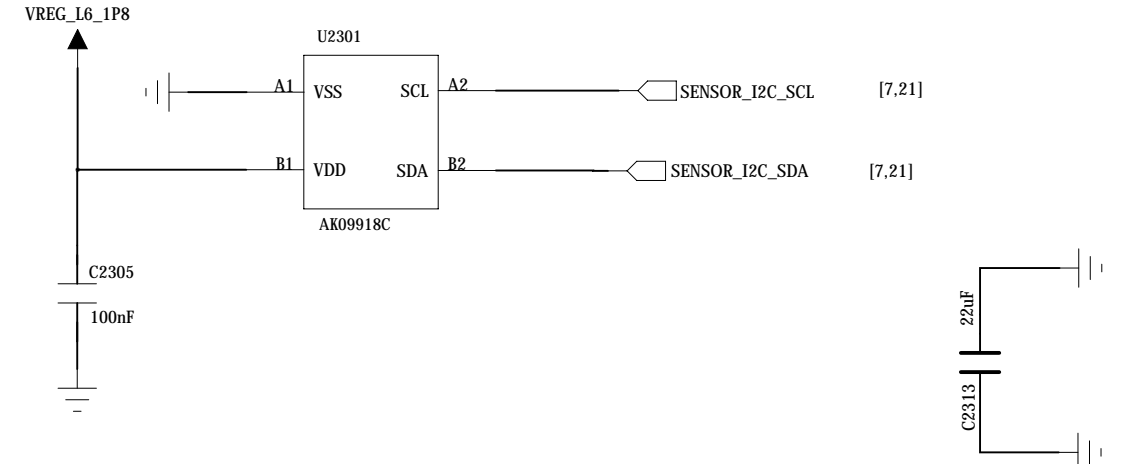
Note 62-3: Reserve a capacitor (27pF) on camera's MCLK and shunt it to GND to prevent GPS de-sense.

COMPANY: <Company Name>			
TITLE: <Title>			
DRAWN: <Drawn By>	DATE: <Drawn Date>		
CHECKED: <Checked By>	DATE: <Checked Date>		
QUALITY CONTROL: <QC By>	DATE: <QC Date>		
RELEASED: <Released By>	DATE: <Release Date>		
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SCALE: <Scale>		SHEET: 00	31

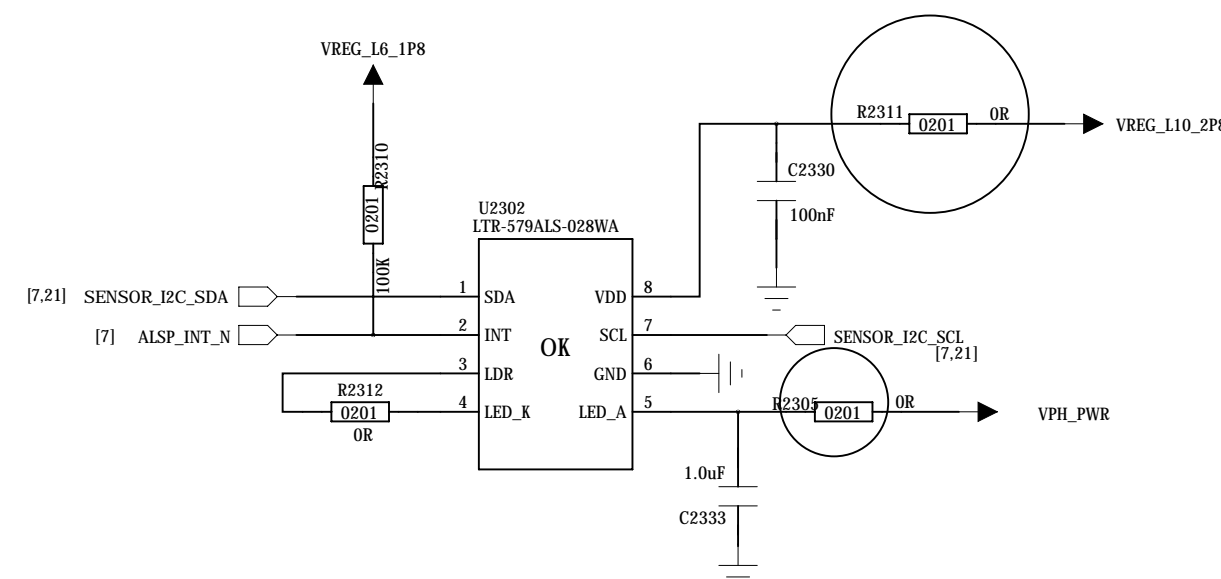
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M-Sensor

M-Sensor I2C Address: 0x0C

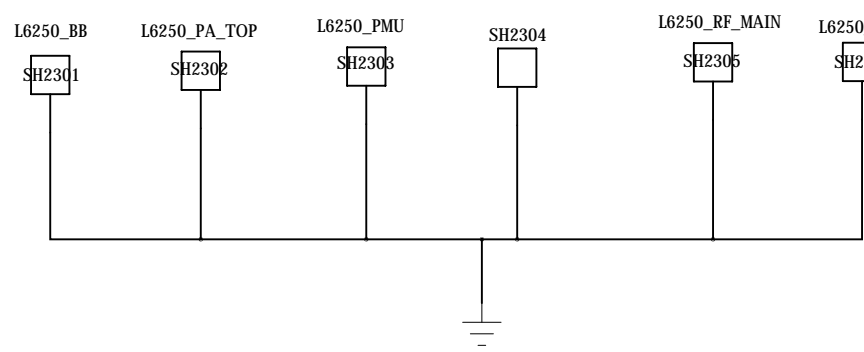
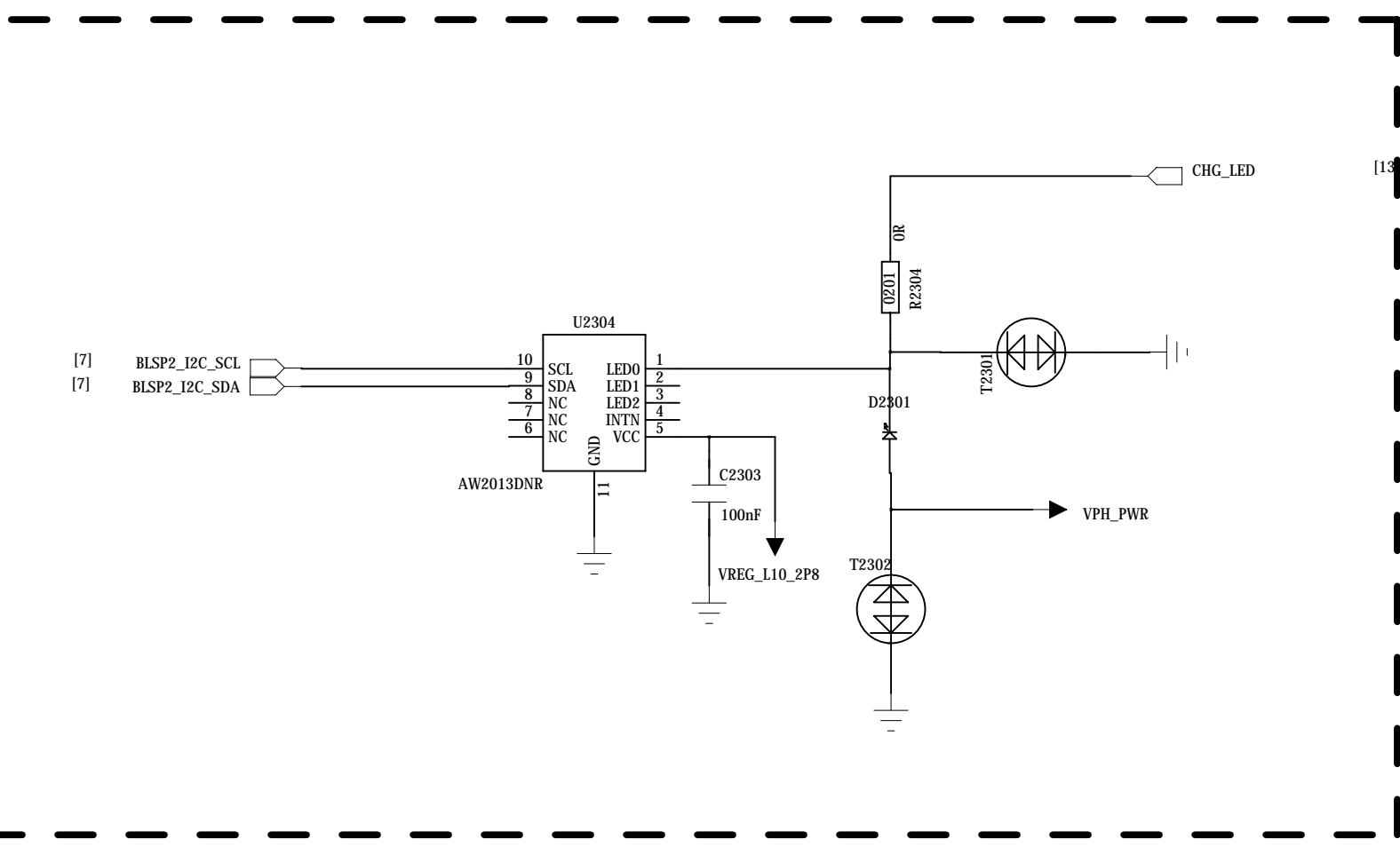
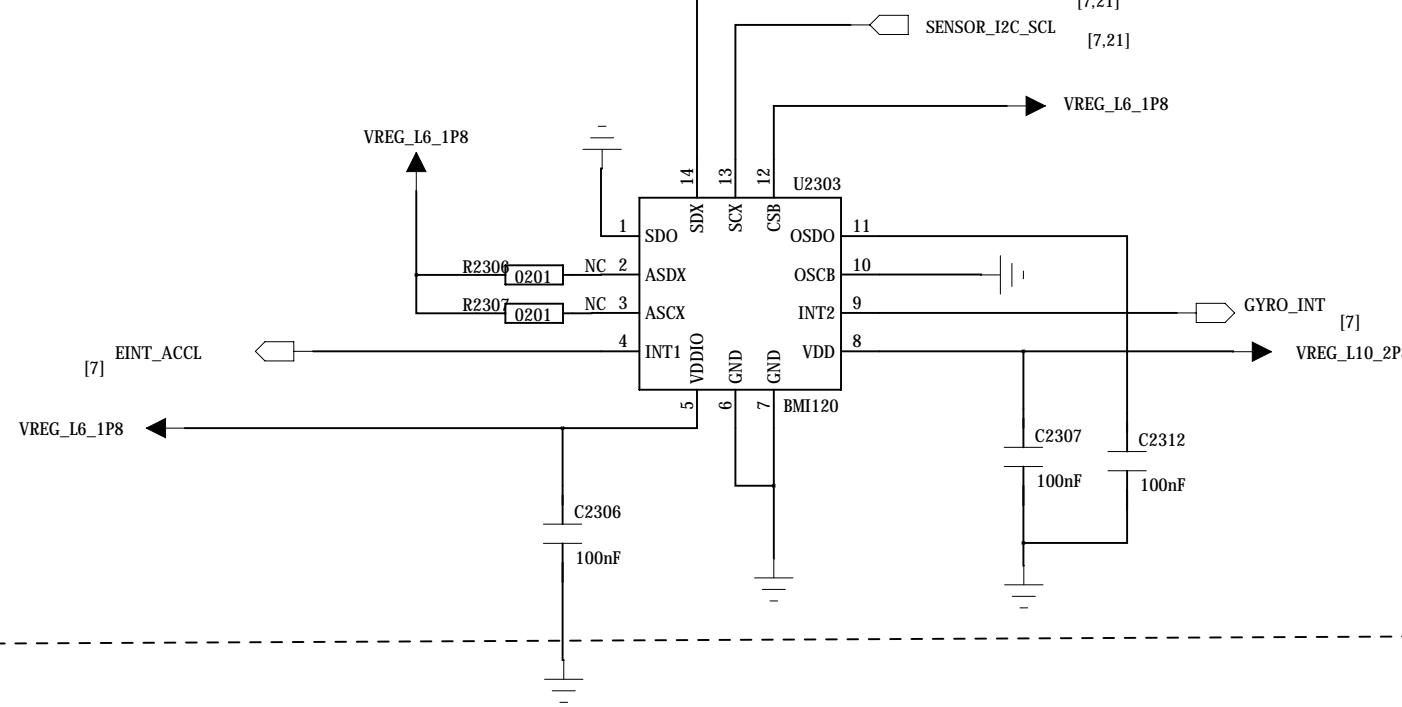


P_SENSOR

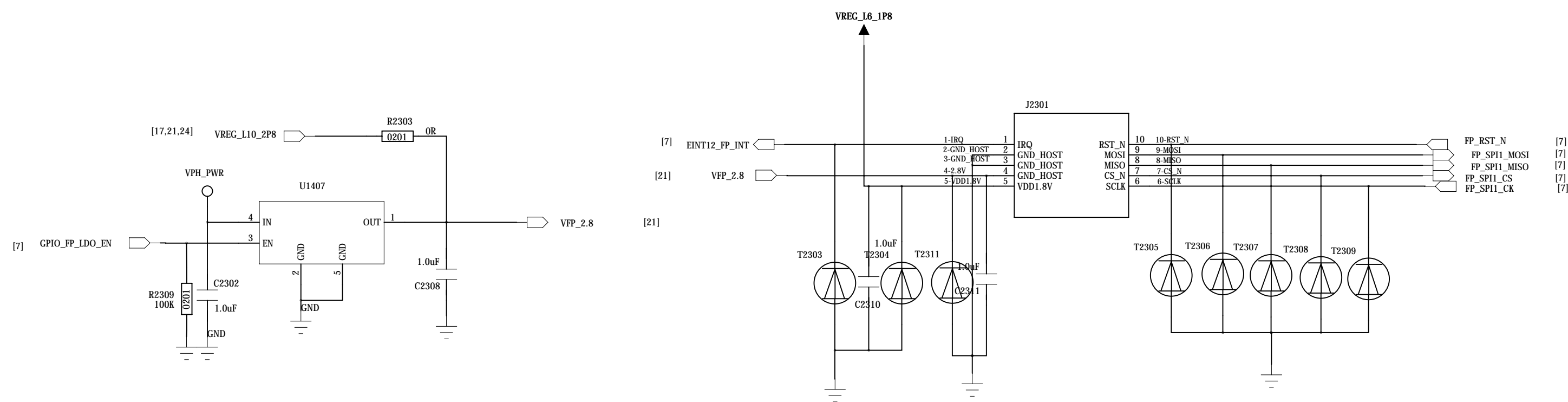


G+Gyro-Sensor

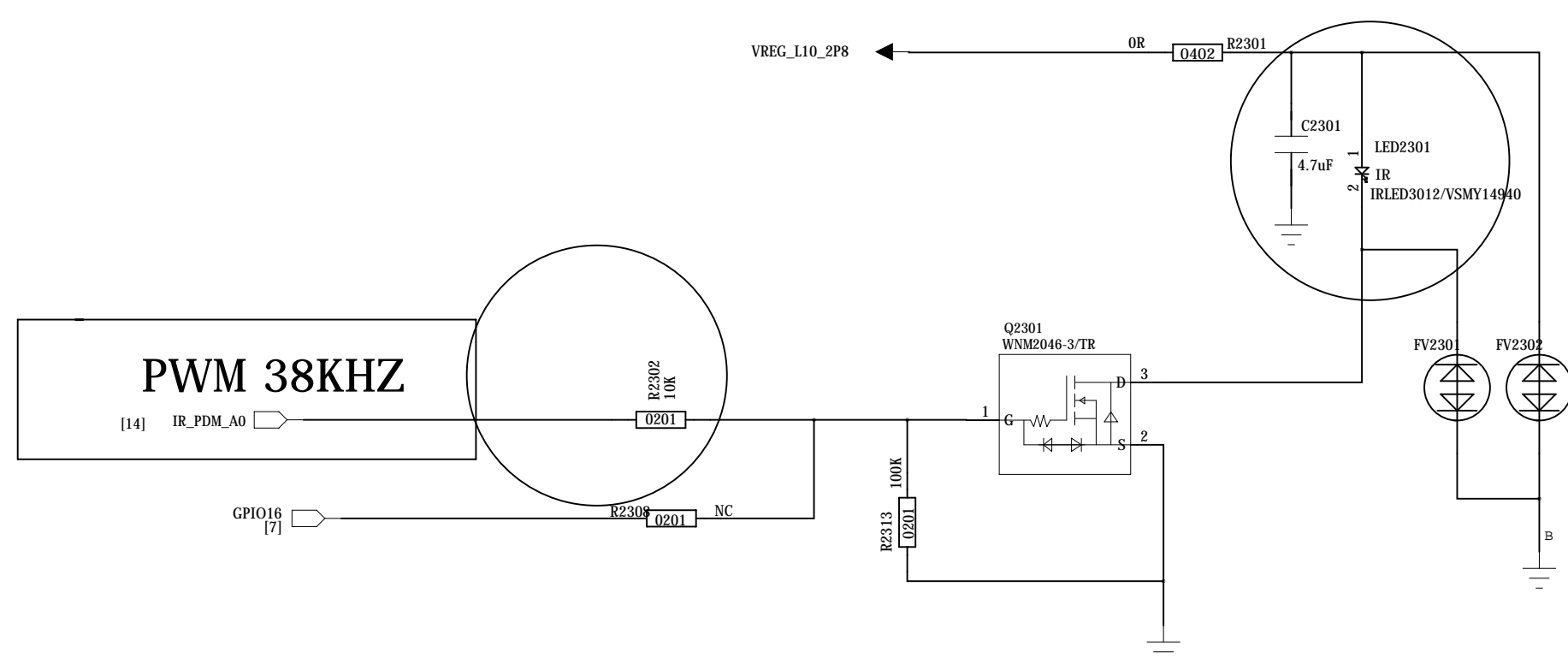
BMI160 and BMI120 is Pin To Pin I2C address : 0x68



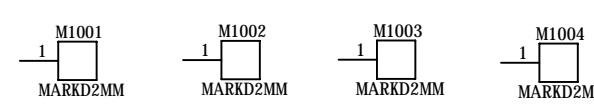
FingerPrint-Sensor



IR



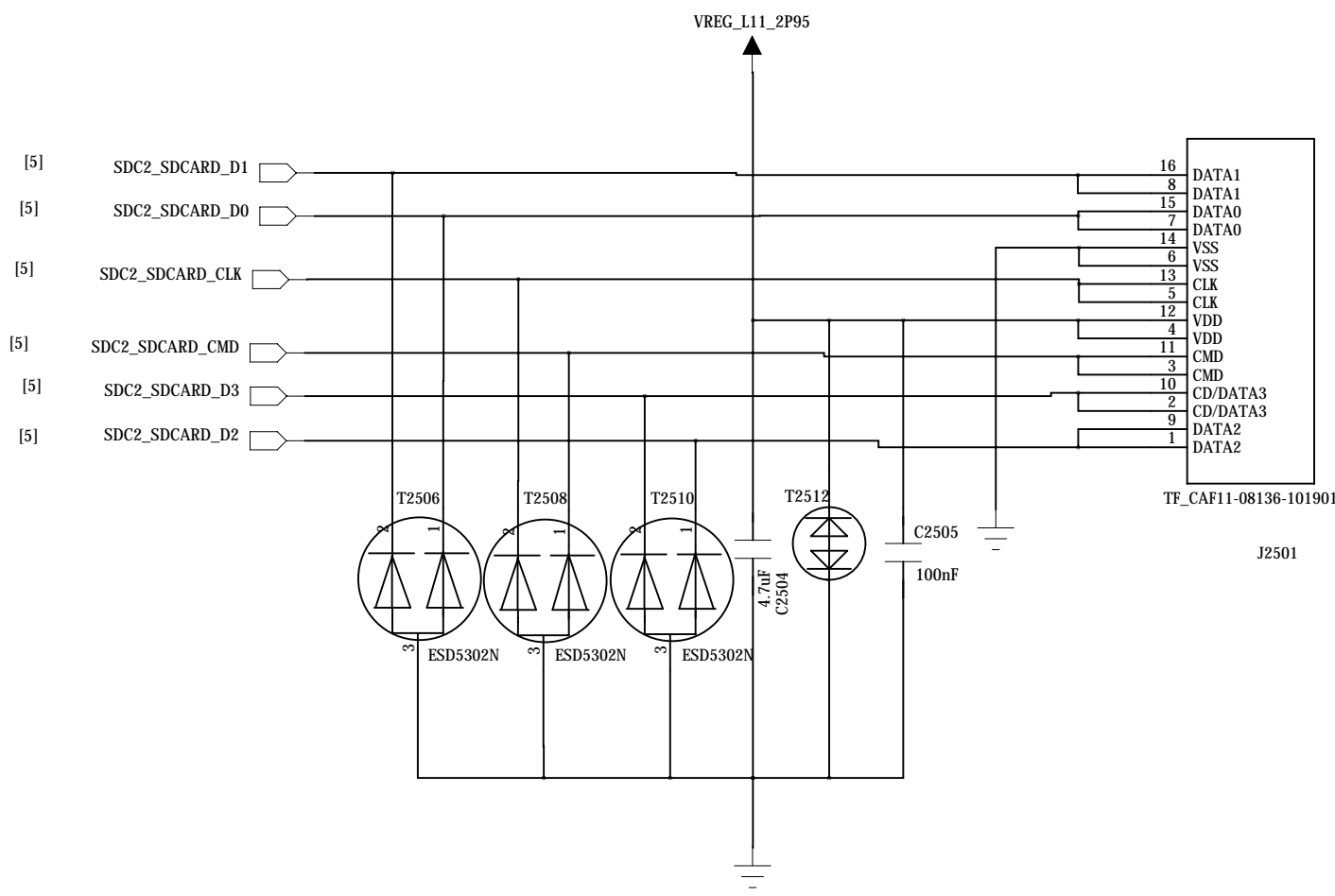
MARK POINT



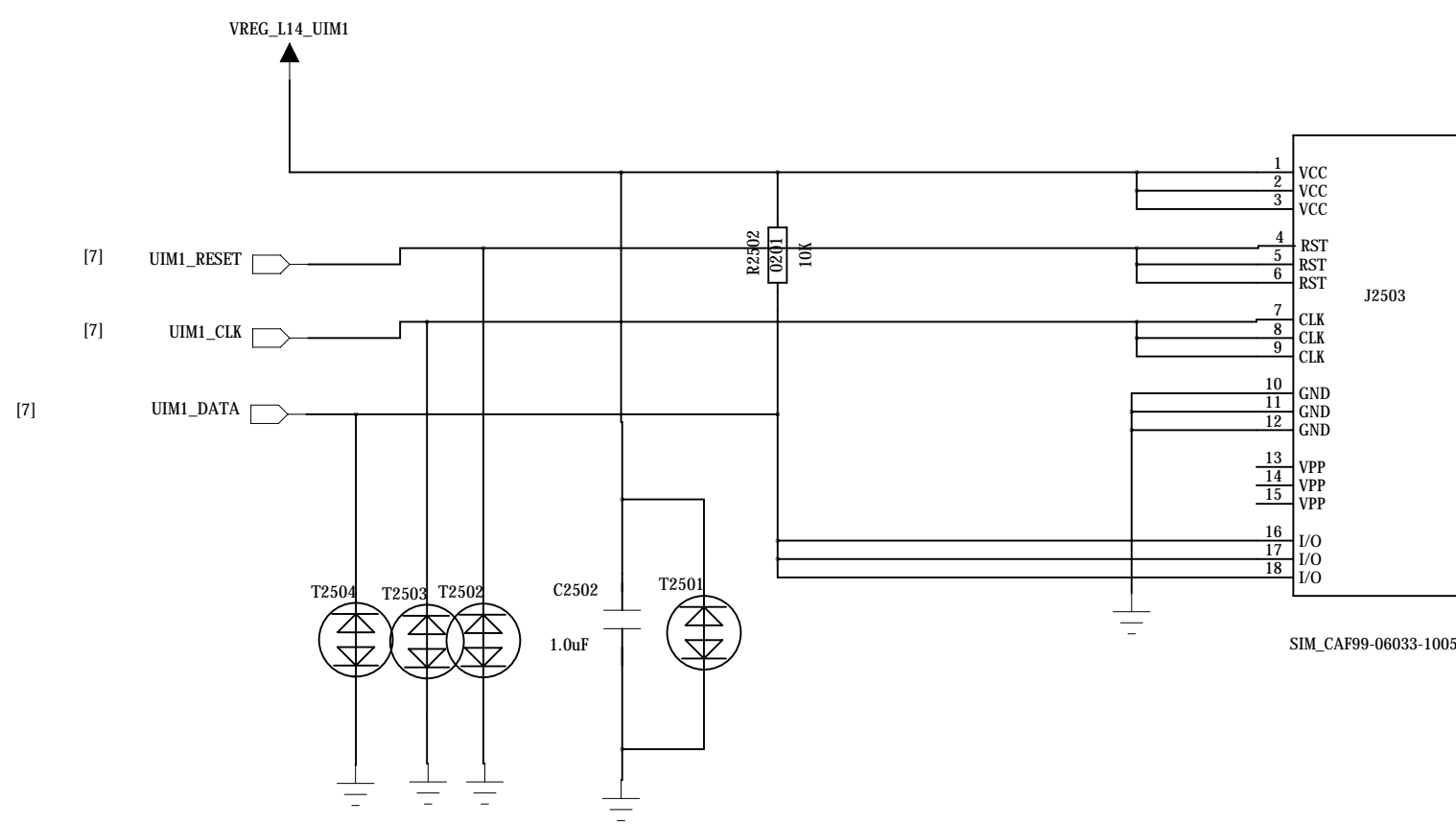
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<Company Name>			
TITLE:			
<Title>			
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<Drawn By>	<Checked By>	<QC Date>	<Scale>
CODE:	SIZE:	DRAWING NO:	REV:
<Code>	A0	<Drawing Number>	<Revision>
SHEET: 84 31			

CTR	ECO NO.	APPROVED	DATE

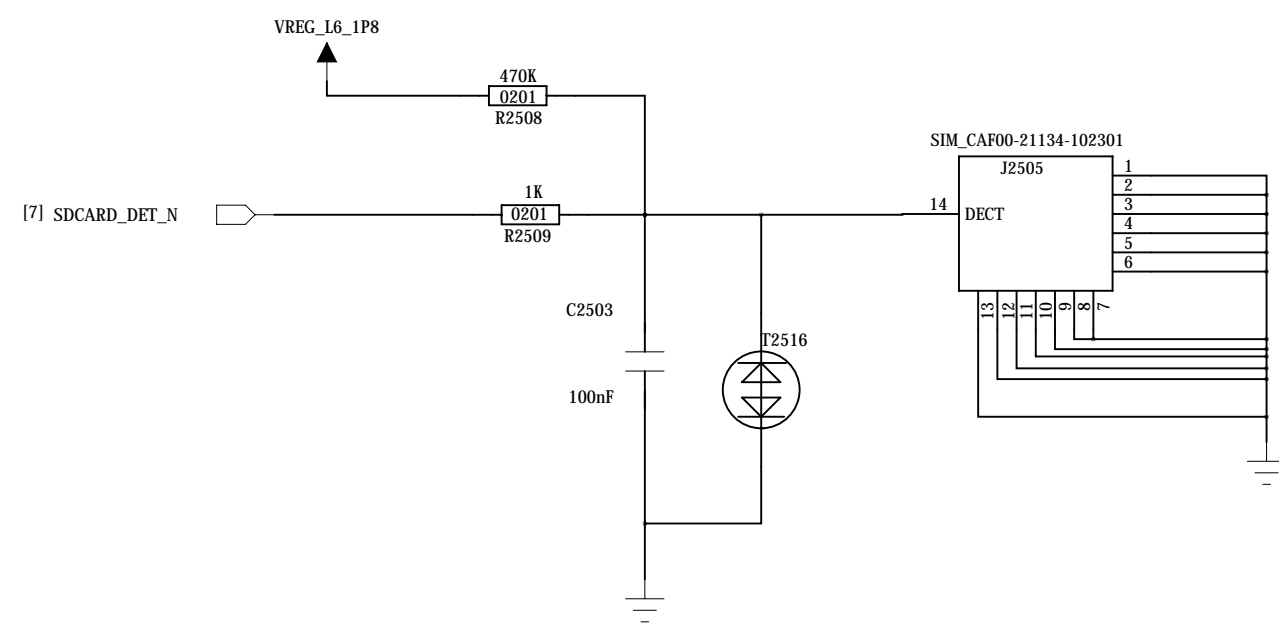
T- Card



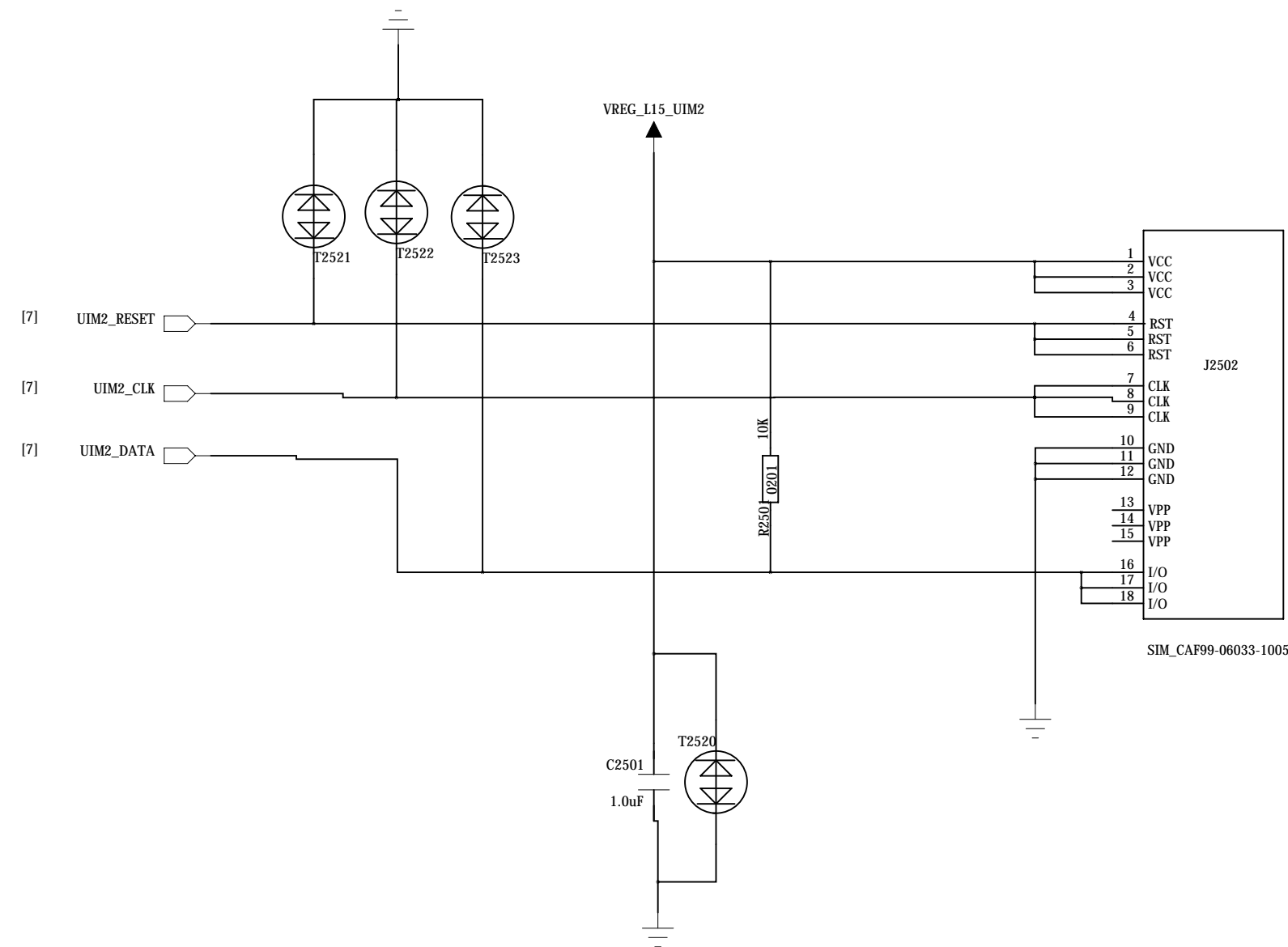
SIM1



INT

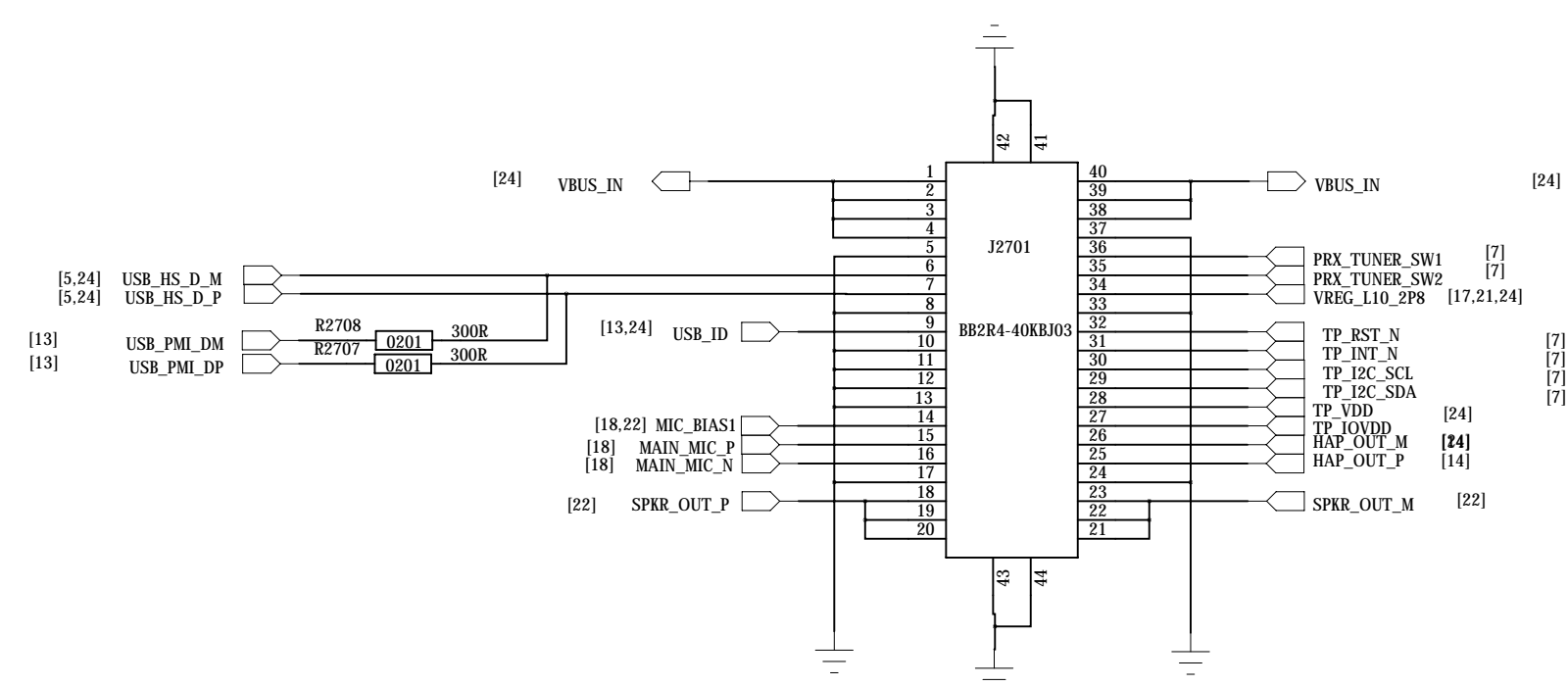


SIM2

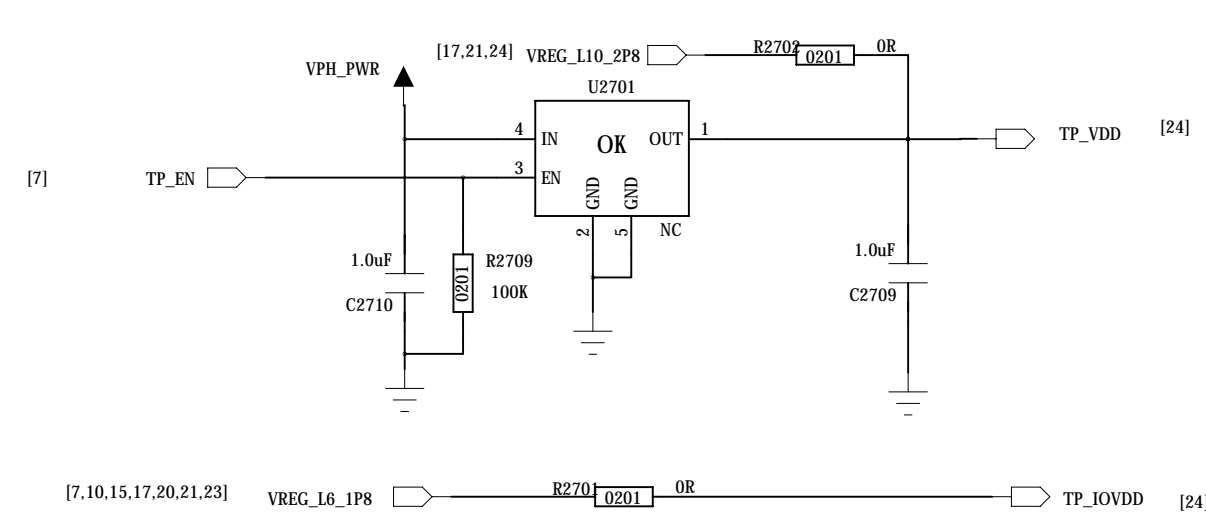


COMPANY				<Company Name>			
TITLE				<Title>			
DESIGN	<Drawn By>	DATE	<Drawn Date>	CORE	SIDE	DRAWING NO.	REV.
CHECKED	<Checked By>	DATE	<Checked Date>	<Code>	A0	<Drawing Number>	<Revision>
QUALITY CONTROL	<QC By>	DATE	<QC Date>	SCALE	<Scale>	SHEET	31
RELEASED	<Released By>	DATE	<Release Date>				

SUB_FPC

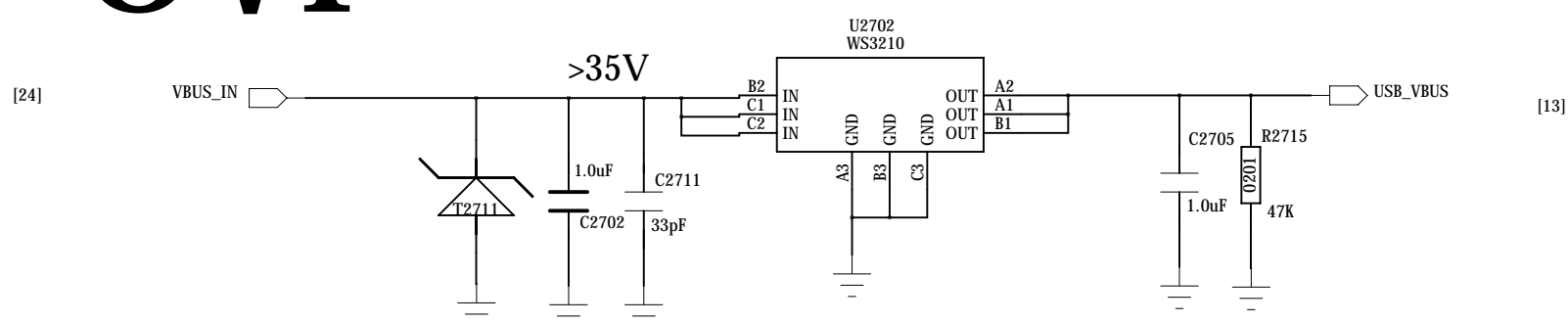


LDO

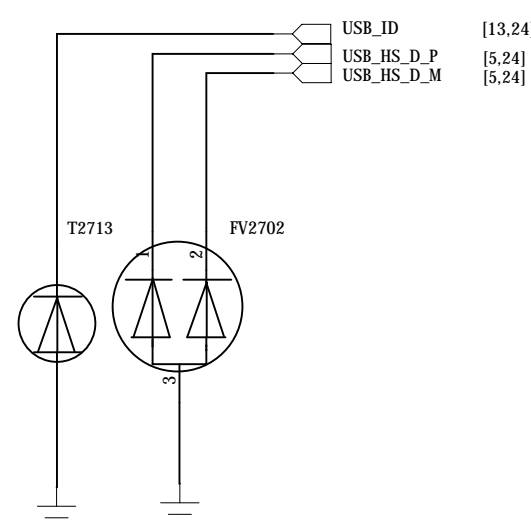
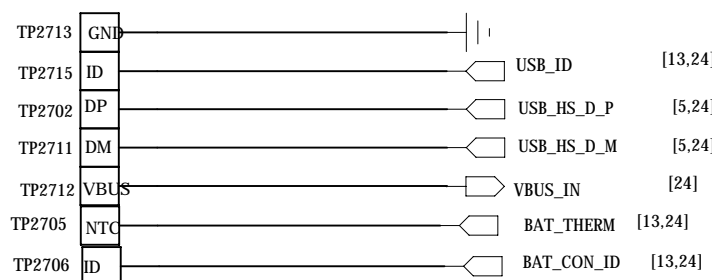


OVP

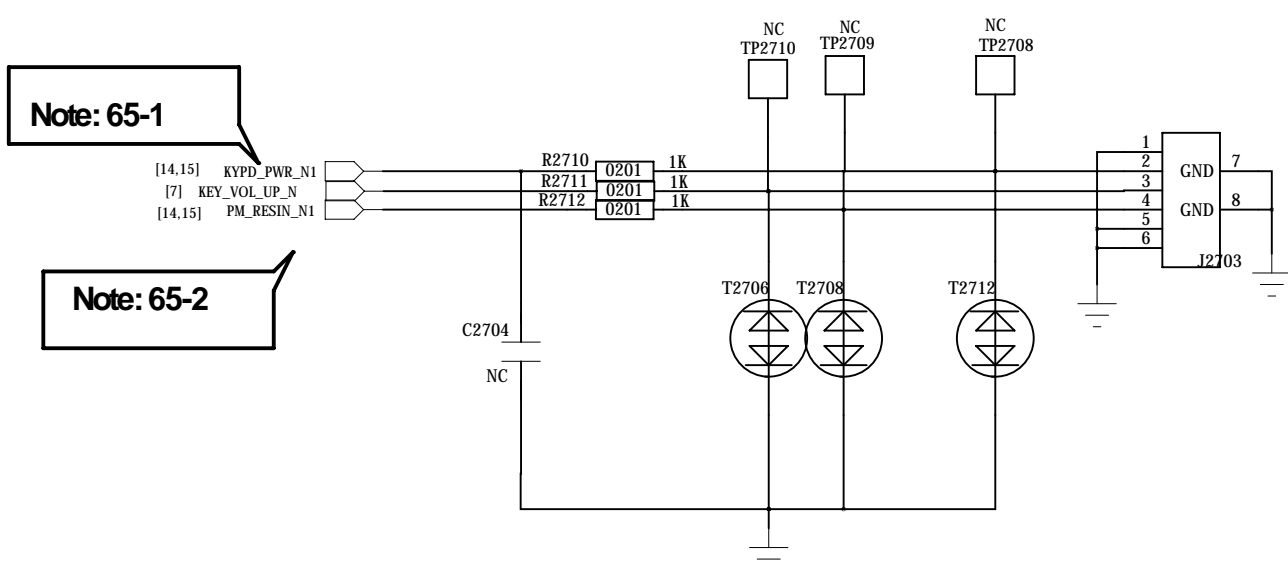
OUT cap share with C704 , can be del



Test point



Power Key

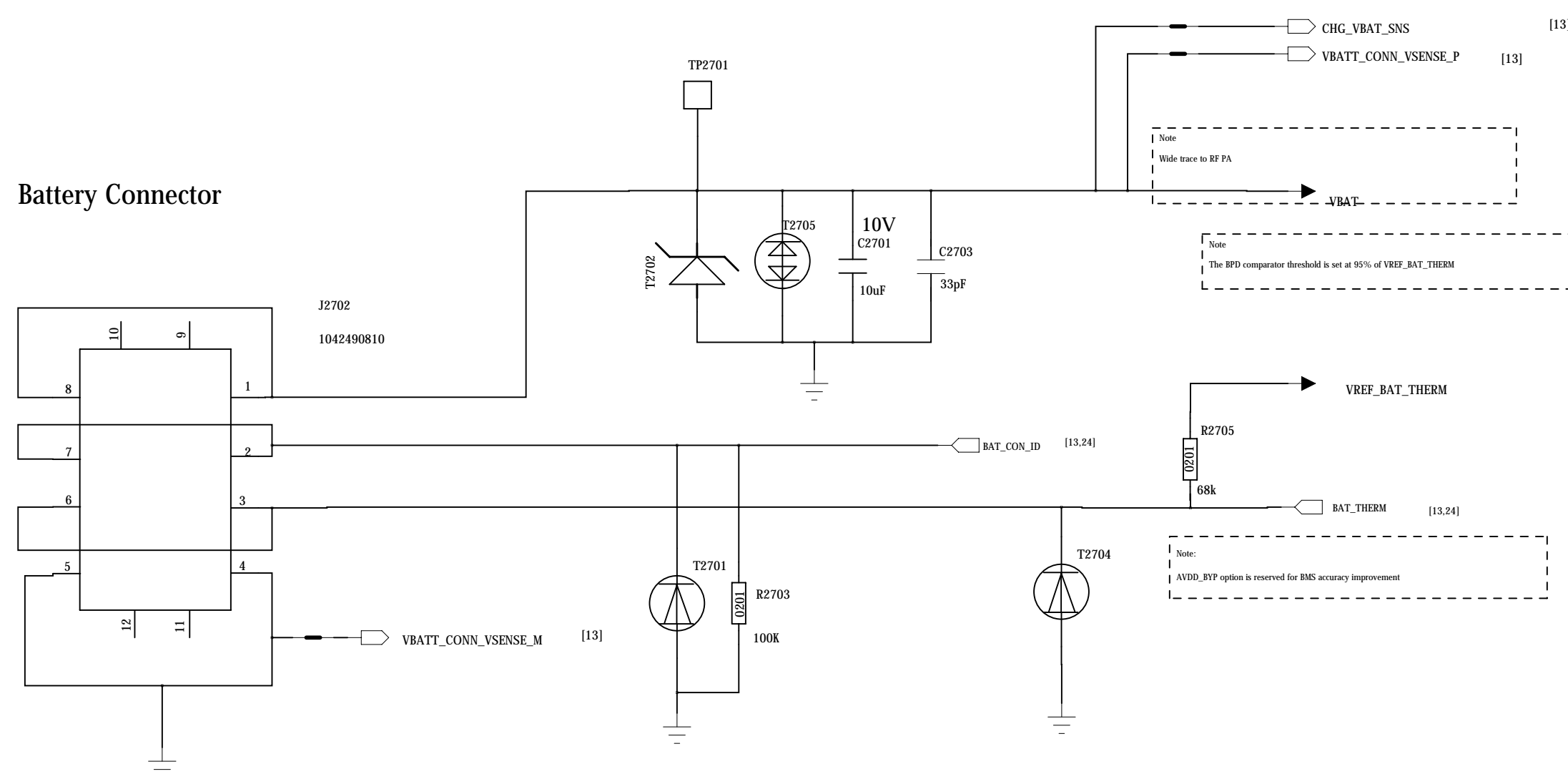


Schematic design notice of "65_PERI_Dual_SIM_ICUSB_KEYPAD" page.

Note 65-1: DO NOT put pull-up resistor on PWRKEY

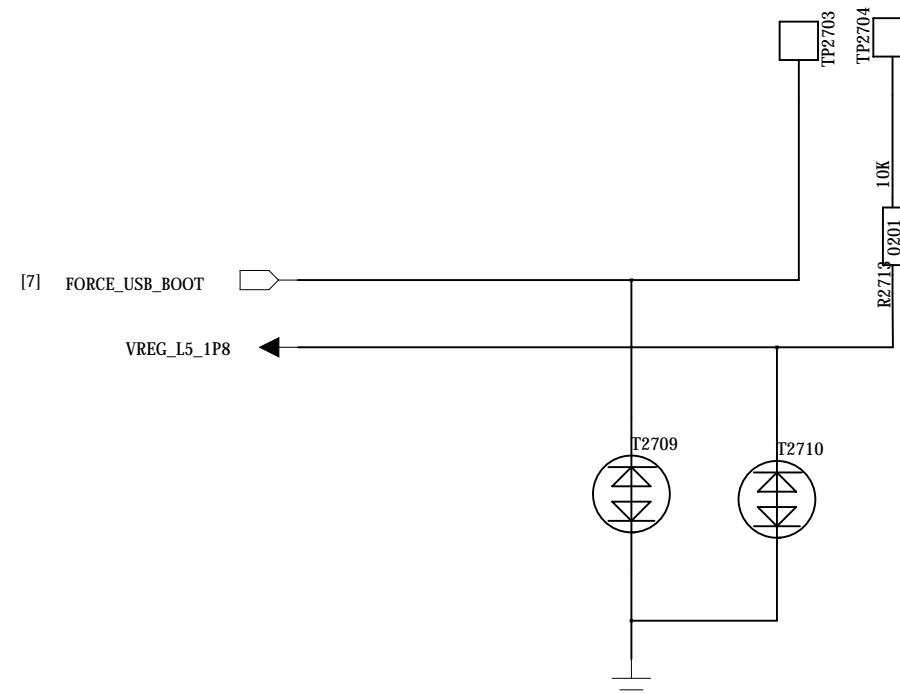
Note 65-2: Volume Up : HOME Key / GND
Volume Down : (KPROW/KPCOL) or KPCOL / GND

BAT

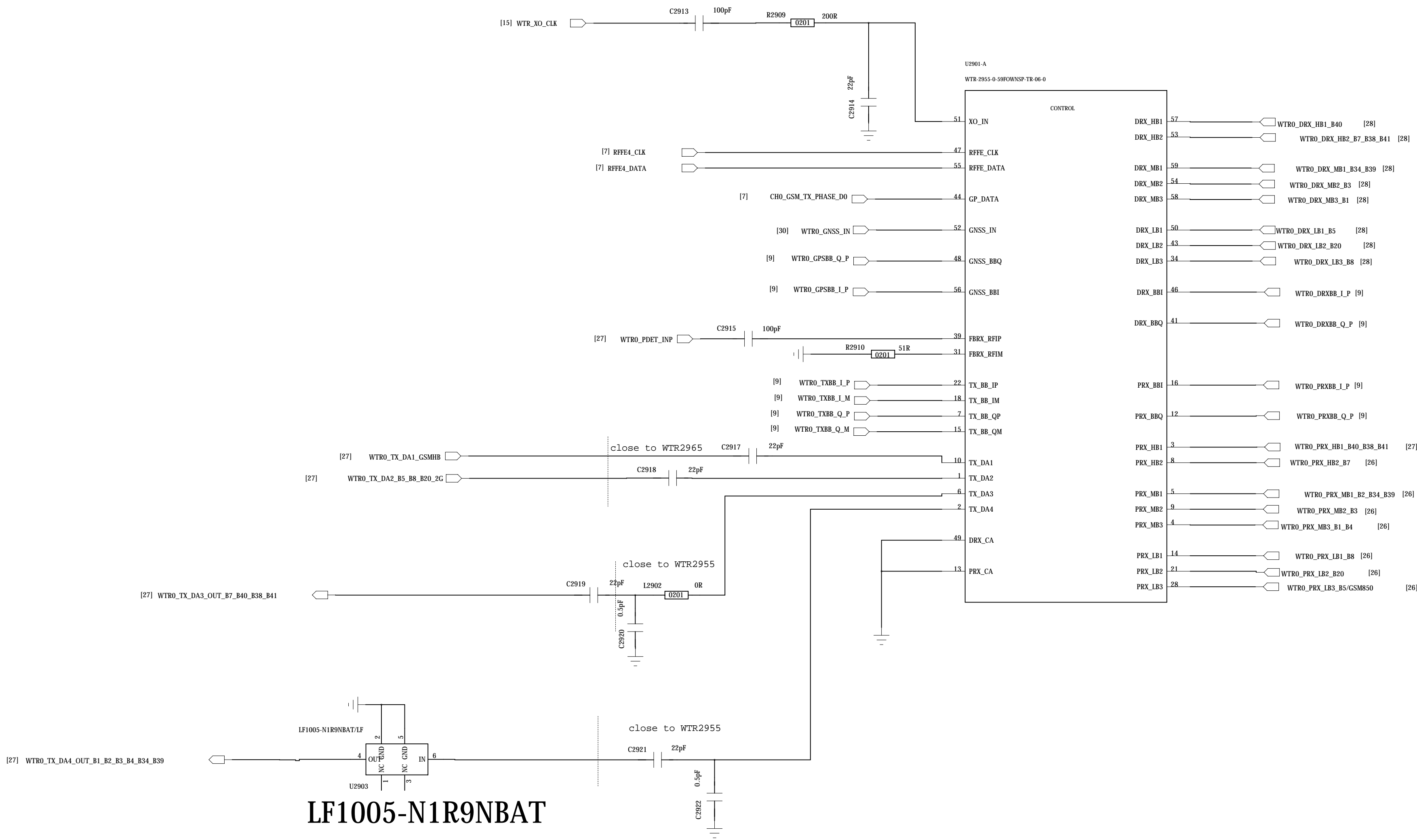
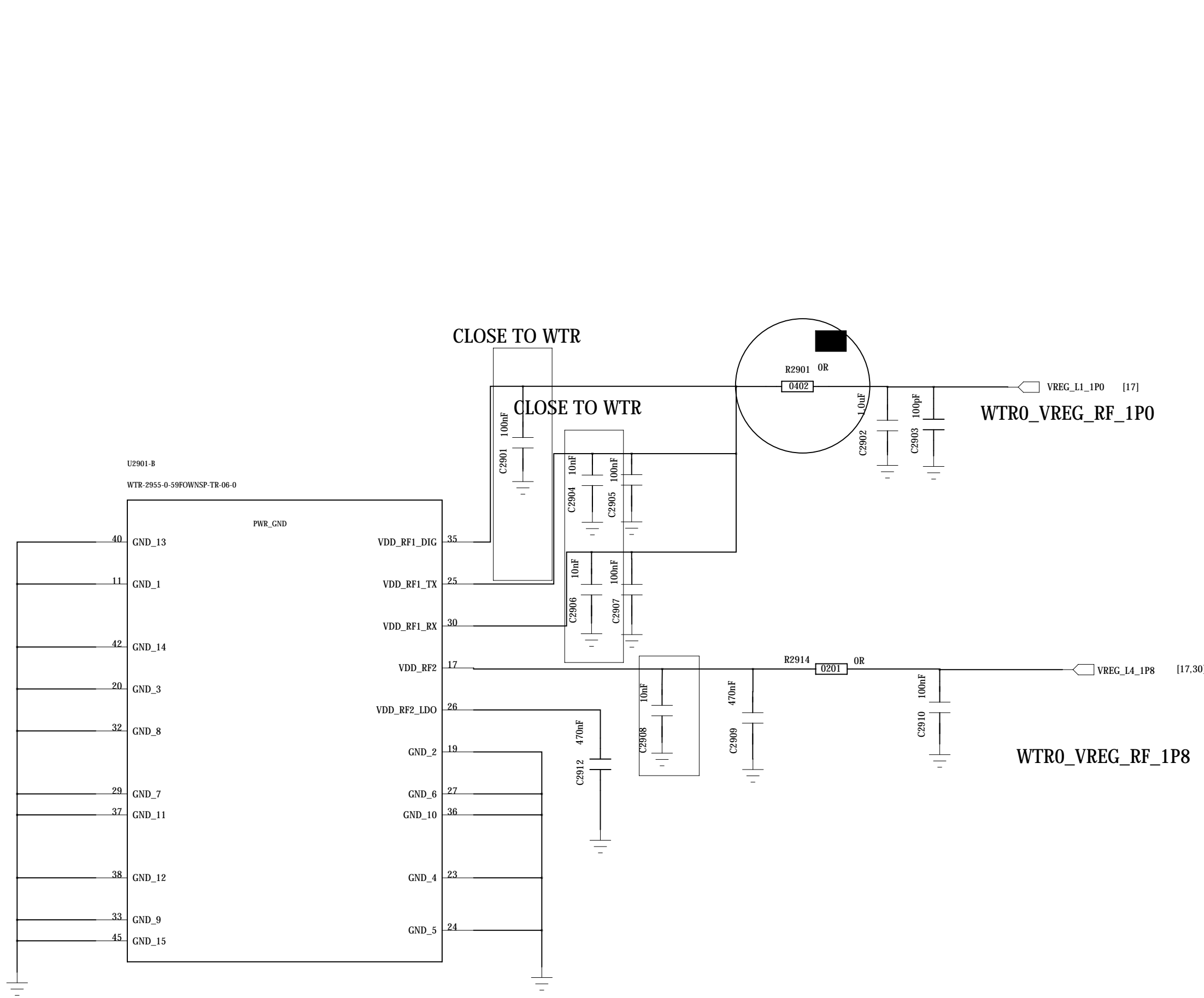


Note:
Battery ID resistor value require 20K~150K.
Add 100K to ground If battery package ID not meet requirement

Force USB boot



REVISION RECORD			
LTB	ECO NO.	APPROVED	DATE



Note:RX ports have DC at the pin, so it need DC block,
please make sure there is no DC short to other voltages and GND

COMPANY: <Company Name>			
TITLE: <Title>			
DRAWN: <Drawn By>	DATED: <Drawn Date>	CODE	
CHECKED: <Checked By>	DATED: <Checked Date>	SIZE	DRAWING NO.
QUALITY CONTROL: <QC By>	DATED: <QC Date>	<Code> A0 <Drawing Number>Revision>	
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 25 31

D

D

C

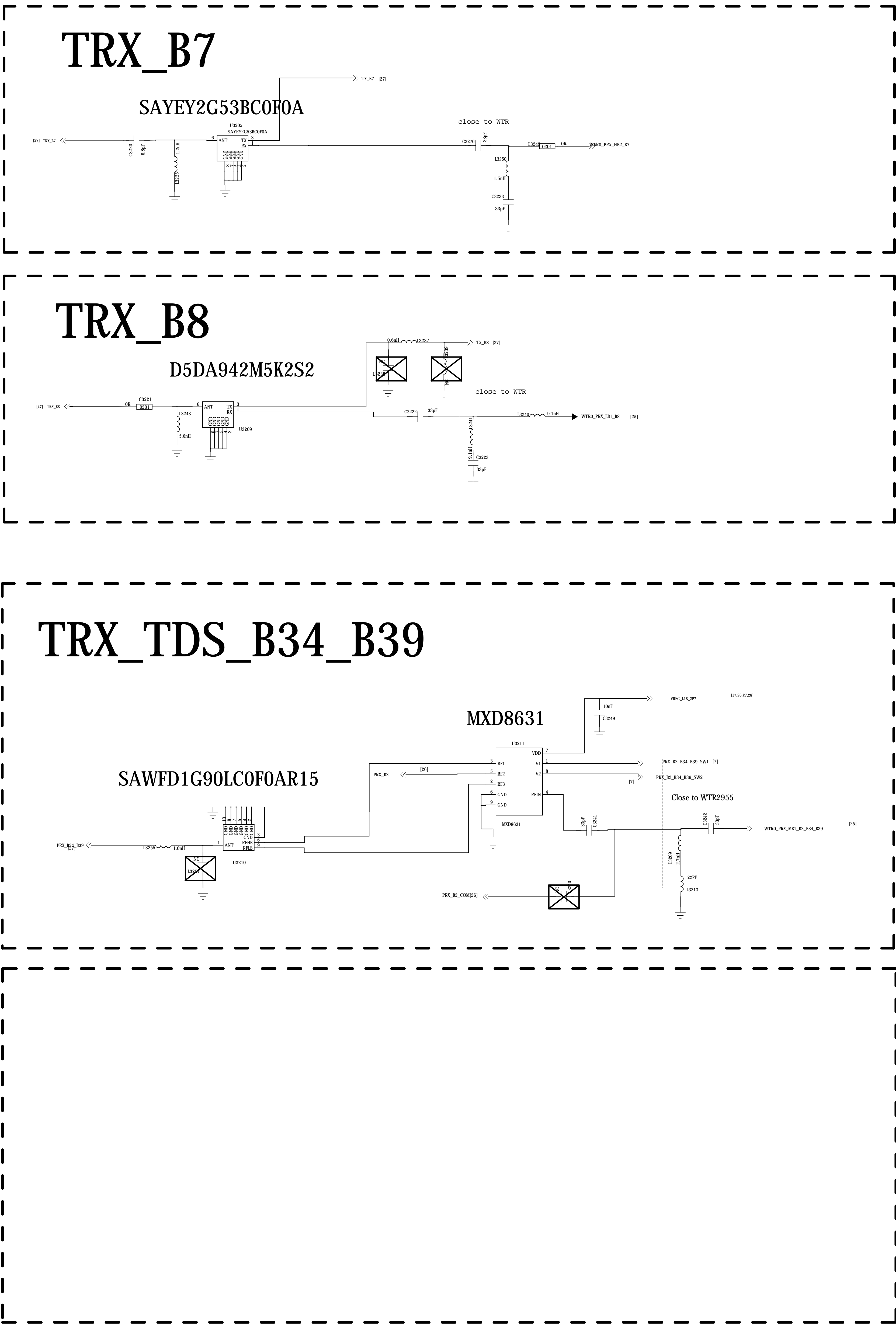
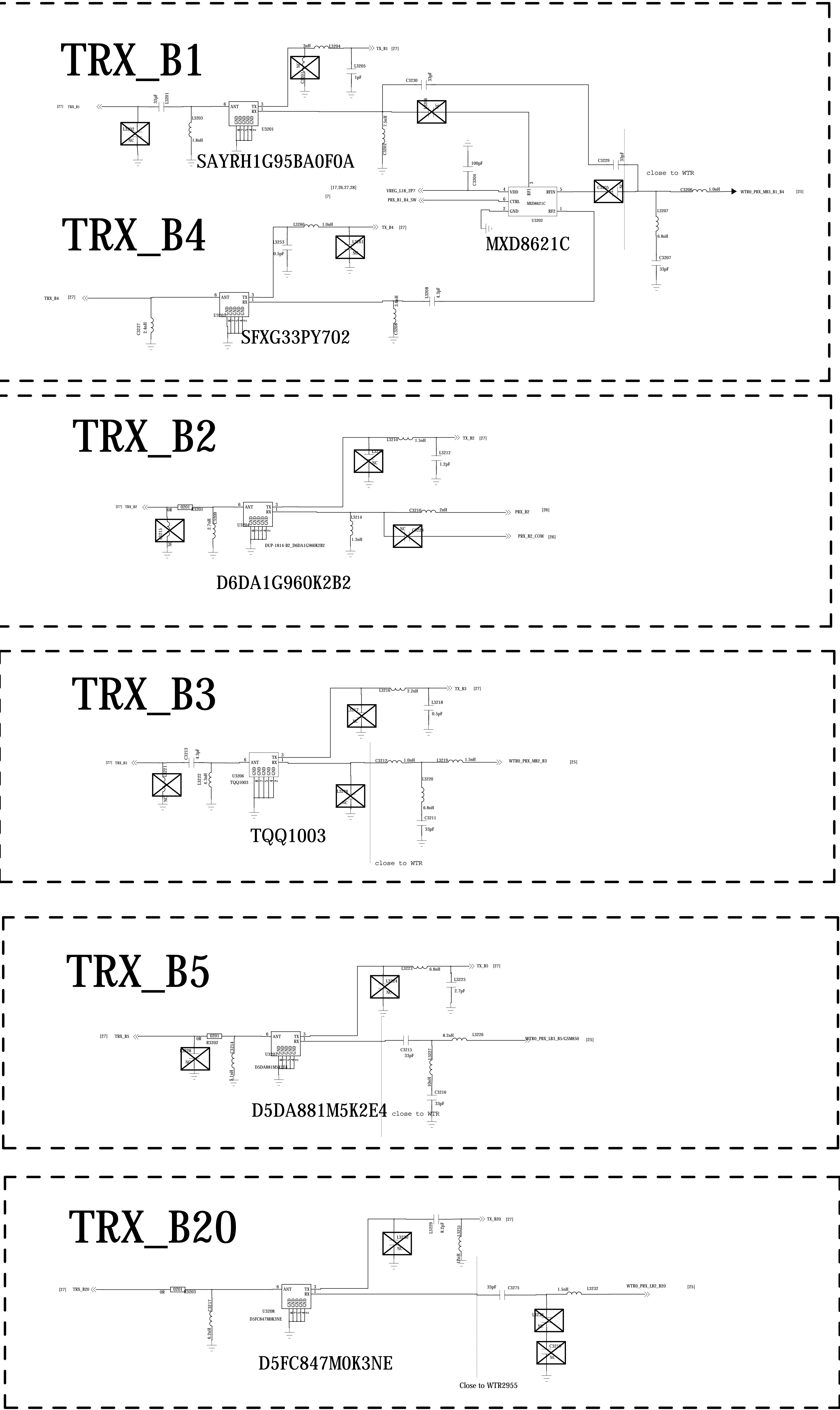
C

B

B

A

A



REVISION RECORD			
LYR	REV. NO.	APPROVED:	DATE:

TXM

X.FL-R-SMT-1(80)

MM8030-2610B

MXD8621C

RFMD5212A

MMPA

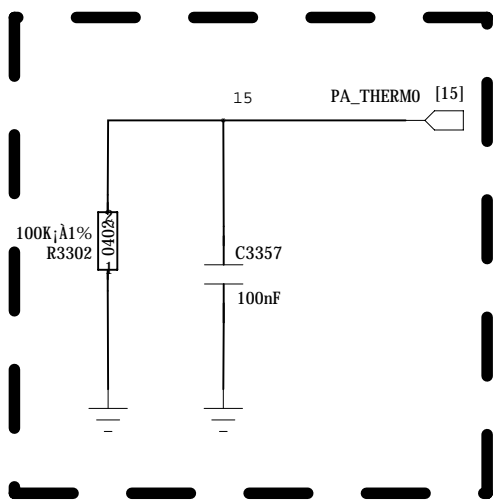
QM23040T

B39262B8870L210

ACX BF1608-L1R9NDB

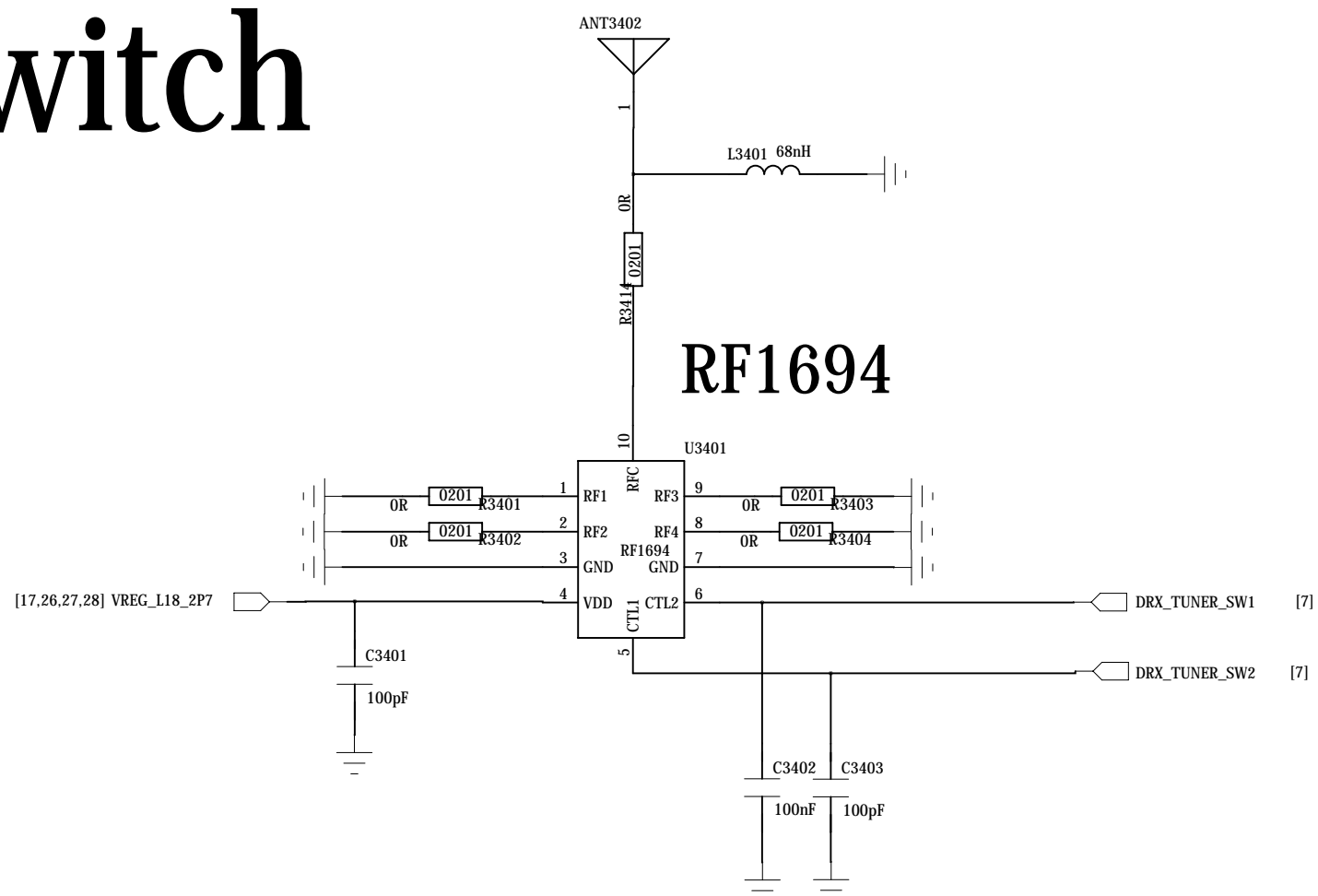
RFMD5428

Near to PA

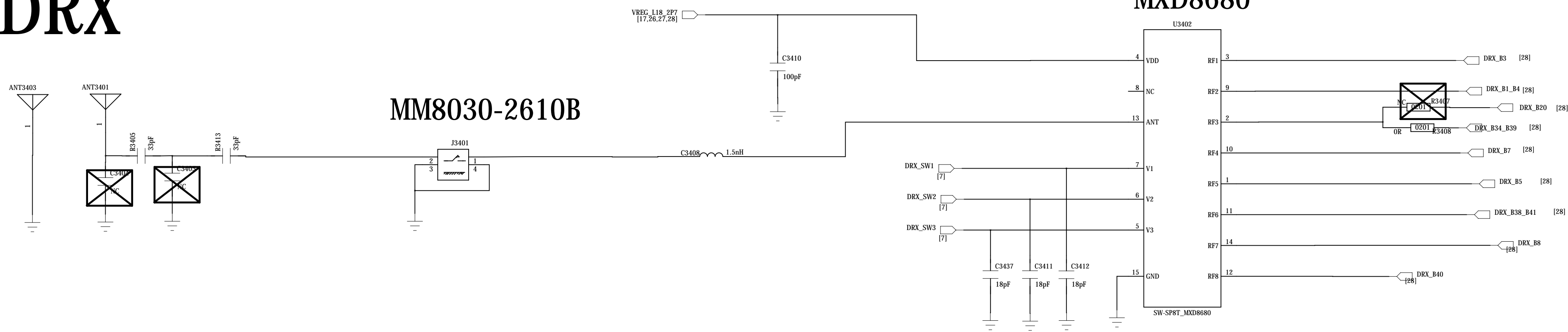


COMPANY: <Company Name>			
TITLE: <Title>			
DRAWN: <Drawn By>	DATED: <Drawn Date>		
CHECKED: <Checked By>	DATED: <Checked Date>	CODE	SIZE
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO.	
RELEASED: <Released By>	DATED: <Release Date>	REV:	
SCALE: <Scale>		SHEET: 27 31	

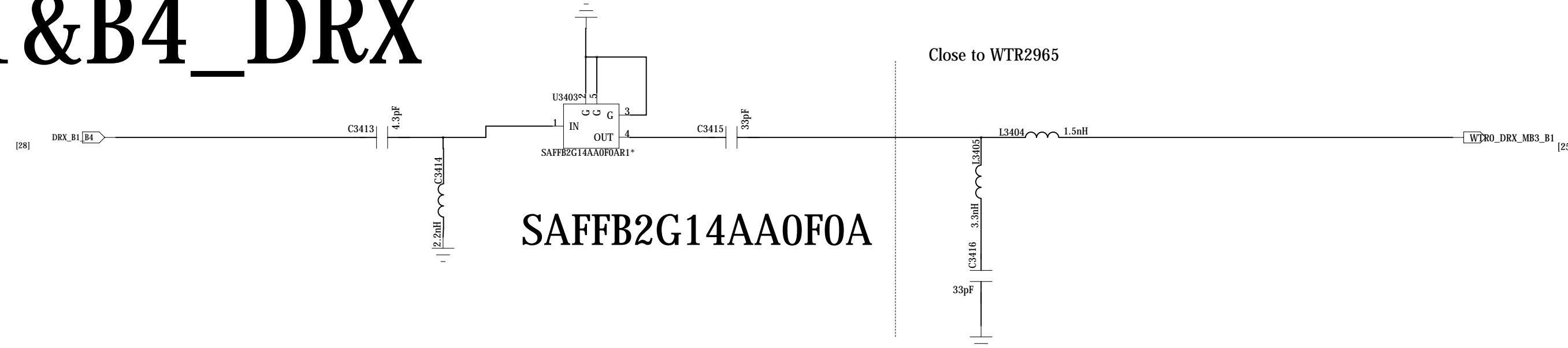
ANT Switch



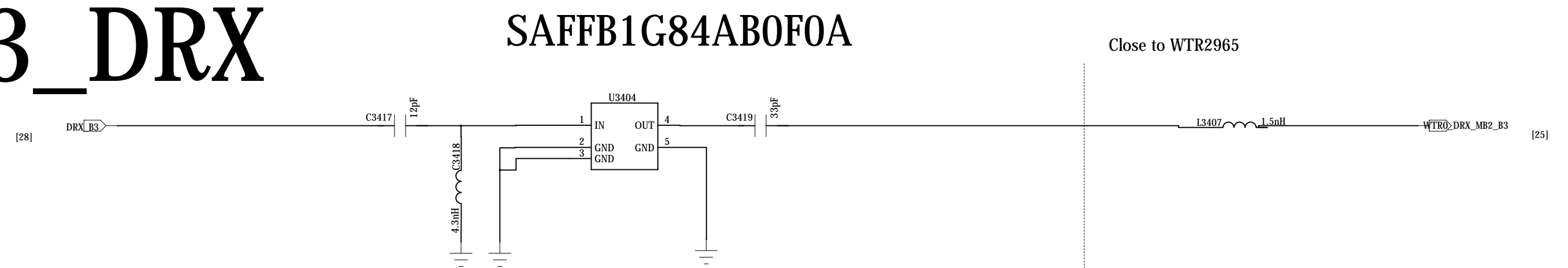
DRX



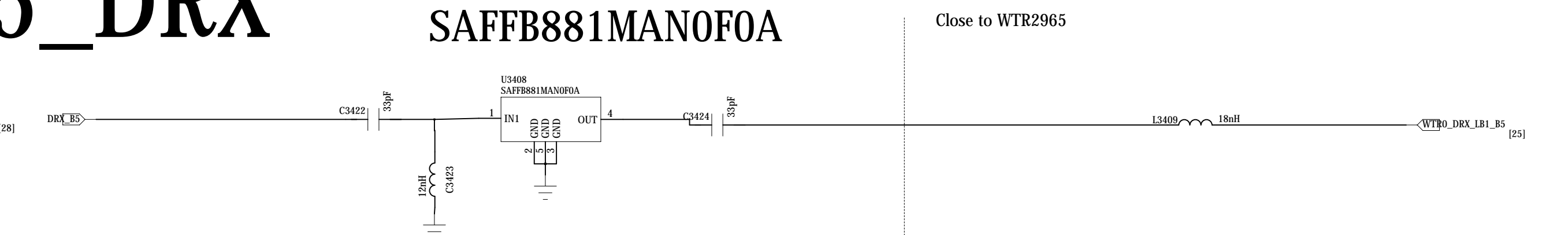
B1&B4_DRX



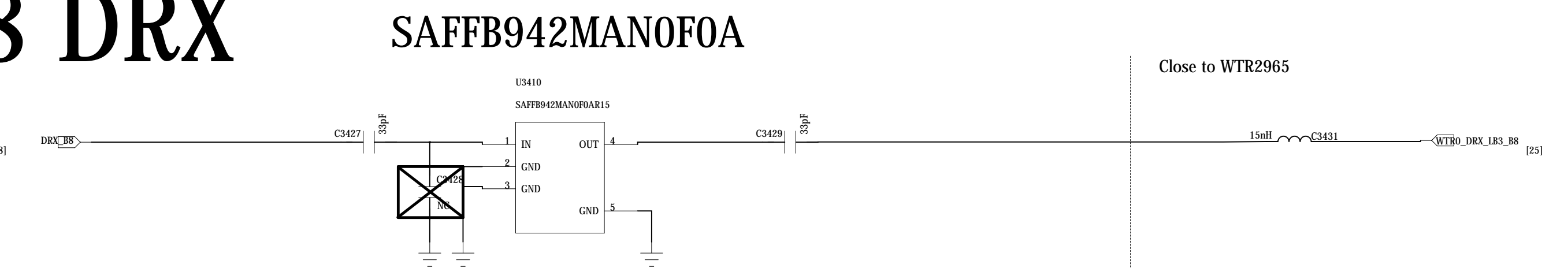
B3_DRX



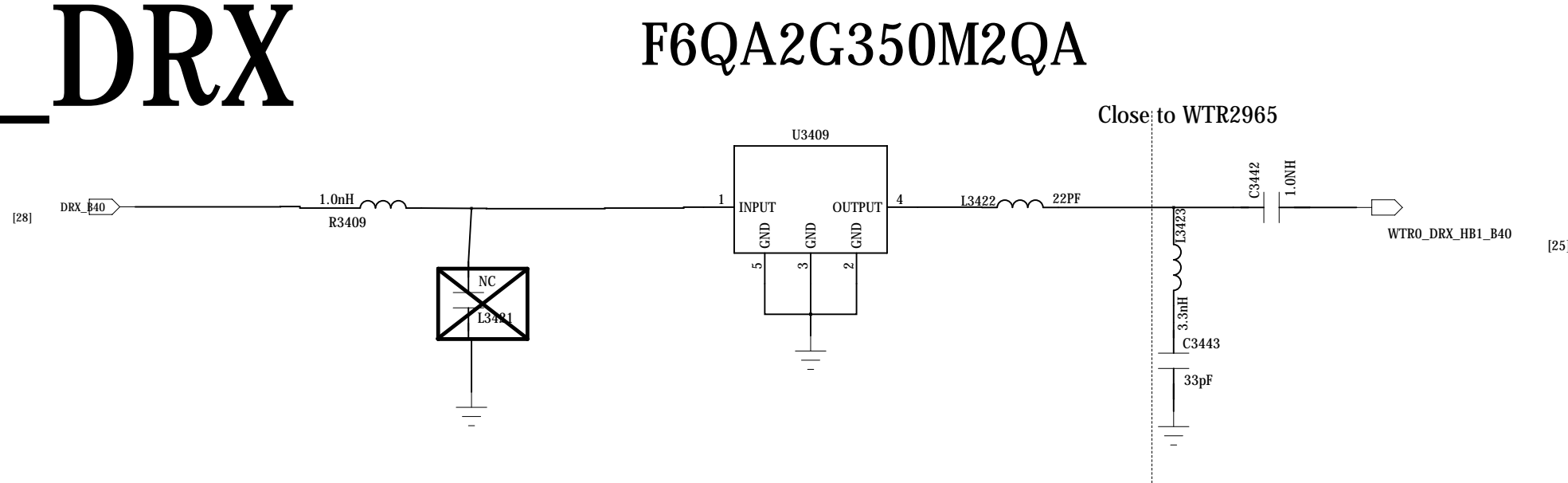
B5_DRX



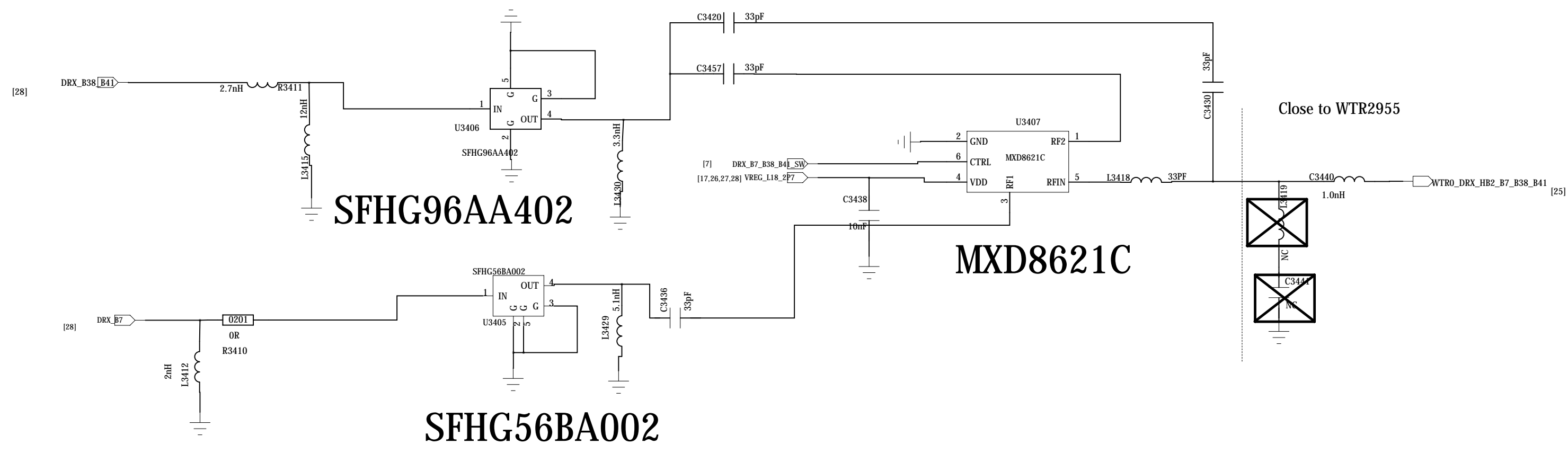
B8 DRX



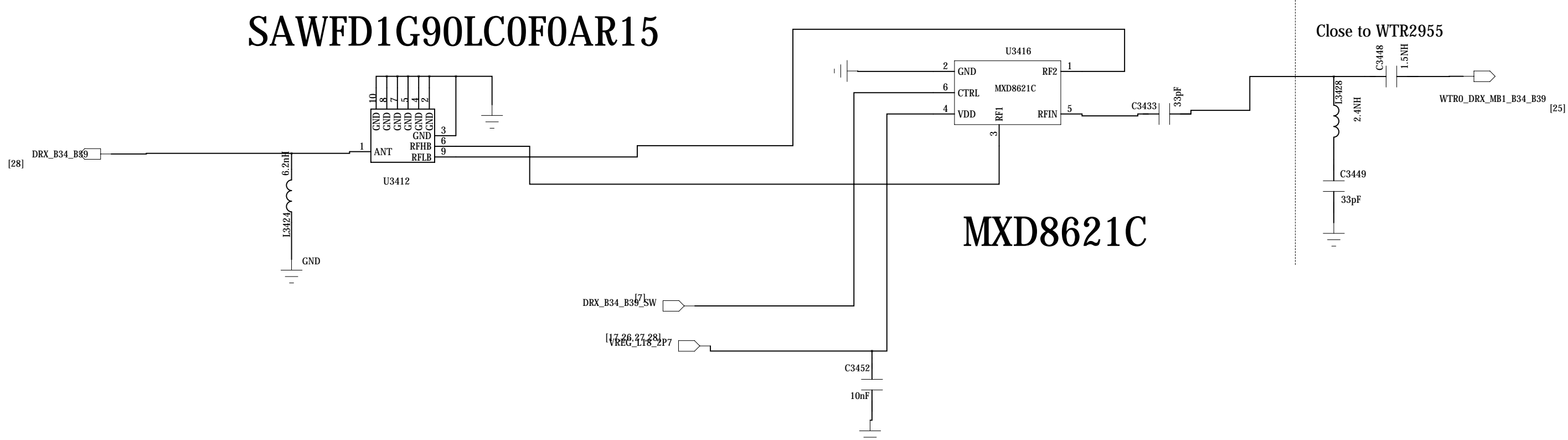
B40_DRX



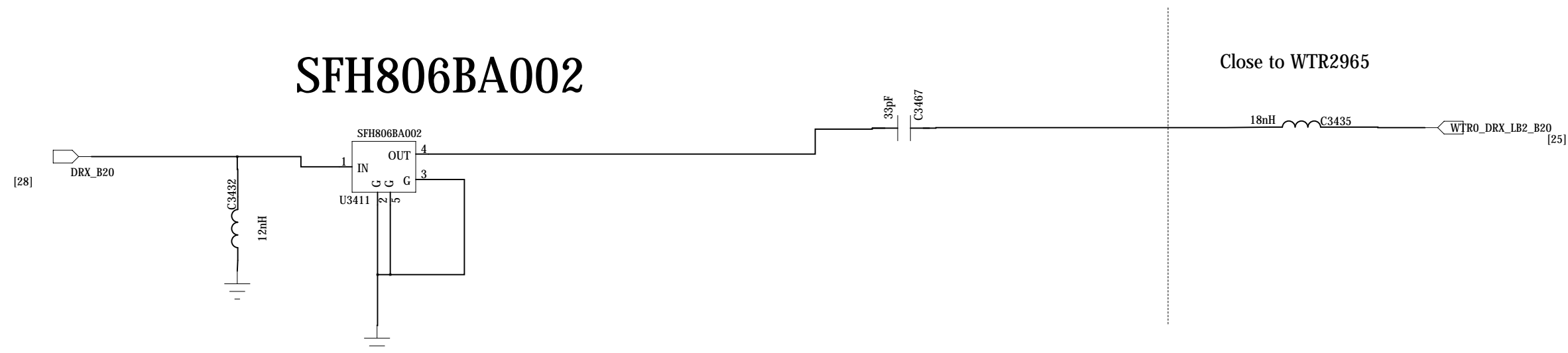
B7_B38_B41_DRX



B34_B39_DRX



B20_DRX



W C N

DRAWN: <u>LiuMengya</u> CHECKED: <u>LIJ</u>		DATED: <u><Drawn Date></u> DATED: <u><Checked Date></u>		COMPANY: <u><Company Name></u> TITLE: <u>24_WCN3680B</u>	
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		<Code>	A0	<Drawing Number>	<Revision>
		SCALE: <u><Scale></u>		SHEET <u>30</u> of <u>31</u>	

Change list

0519

- 1.SIM; ``»»³Éf~D6
- 2.06¼0¶ú»ú²¿·0μçÂ·

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San Diego, CA 92121-1714
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Title		
Sheet		
Size	Name	Rev
Date: _____ Sheet _____ of _____		