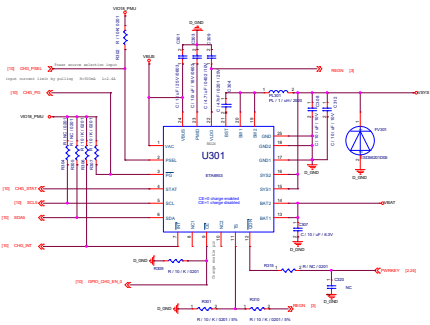


Title <i>Person</i>			
Size C	Document Number Contents		Rev V1.0
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Switching Charger Power Path

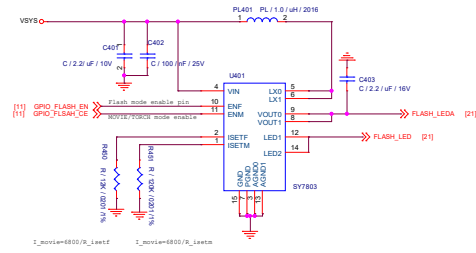
RTA6953: address: 0x68 BQ25601: address: 0x68

10
Don't forget to check the power good sequence. Connect to the pwr0 pin of the
charger (U301) and check the sequence.
Don't forget to check the power good sequence. Connect to the pwr0 pin of the
charger (U301) and check the sequence.
Don't forget to check the power good sequence. Connect to the pwr0 pin of the
charger (U301) and check the sequence.

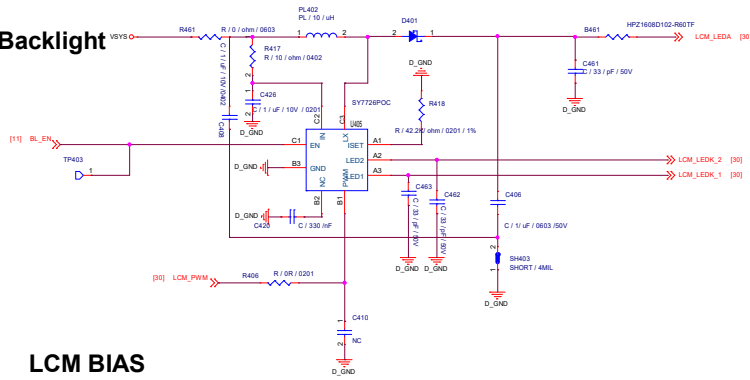


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13	POWER
14	POWER
15	POWER
16	POWER
17	POWER
18	POWER
19	POWER
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99	POWER
100	POWER

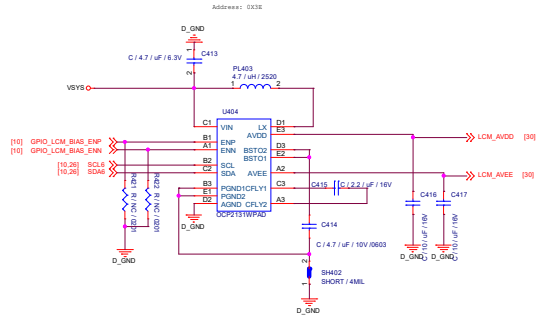
Flash LED Driver



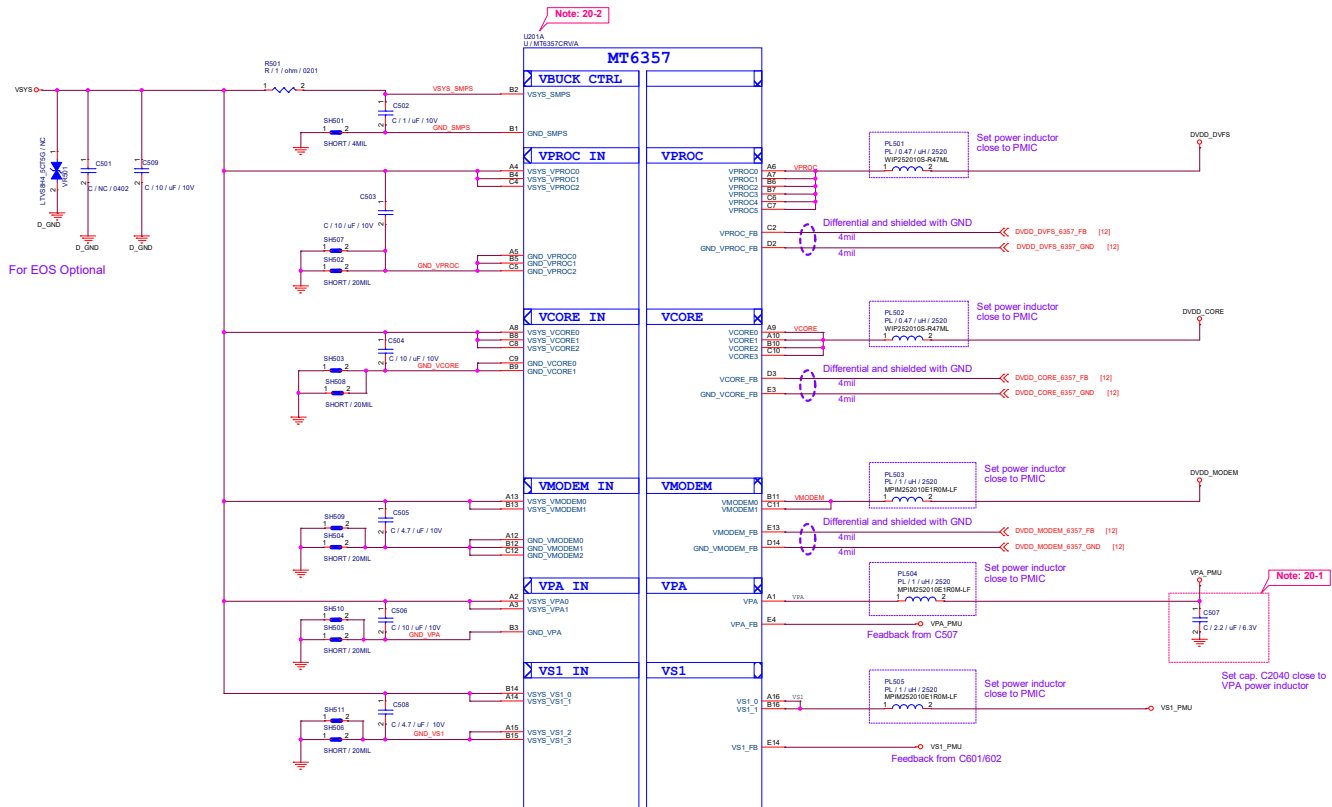
Backlight



LCM BIAS



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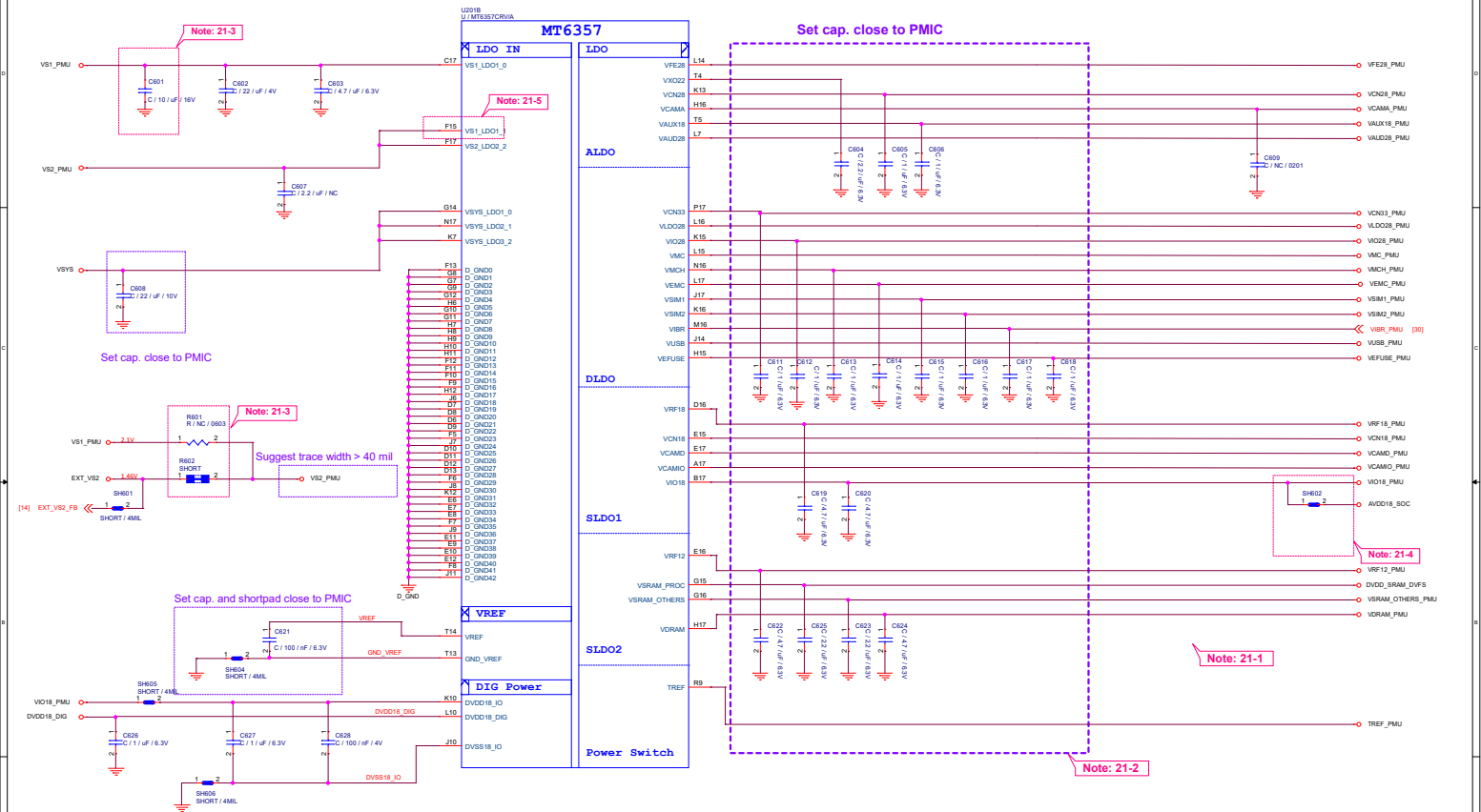
Note 20-1: C507, please choose 0402 size

Note 20-2: PMIC Part number notice for MT6765/62/61 platform

MTK Platform	PMIC
MT6765 / 62	MT6357 CRV
MT6761	MT6357 MRV

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1. "Typical Cap" defined in design notice to LDO Cout. 2. NC cap can move to application, if (PCB L<20nH, PCB R<0.2 ohm) => value and placement of Cap, please refer design notice



Note 21-1: If these power trace can meet LDO layout constraint, these CAP can be NC or removed. Please refer to MT6357 design notice.

Note 21-2: Output cap range please follow MT6357CRV LDO design notice

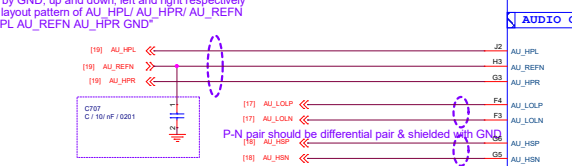
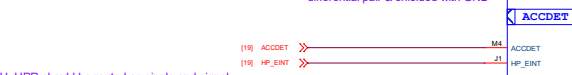
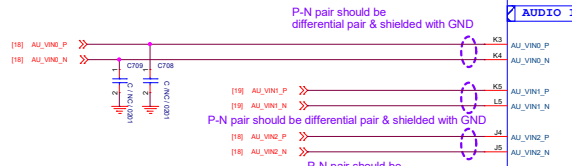
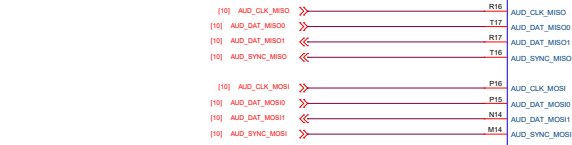
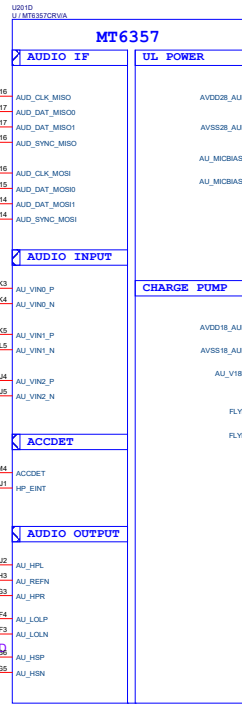
Note 21-3: Ext Buck BOM option

Ext. buck option		
	w/ EXT VS2 Buck	w/o EXT VS2 Buck
C601	10uF	22uF, 0603
R602	0-ohm, 0603	NC
R601	NC	0-ohm, 0603

Note 21-4: Please set SH602 and SH603 close to C620, making star connection among VIO18_PMU, AVDD18_SOC, and EMI_VDD1 near to LDO cap. C620
Please also refer to MT6357 design notice for further detail design information

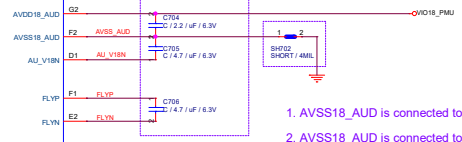
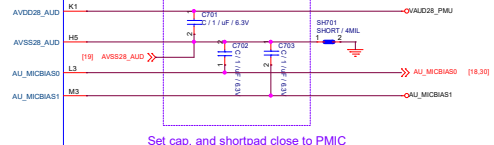
Note 21-5: Please connect VS2_LDO1(F15) to VS1_PMU if voltage applied to VCAMD(E17) >= 1.3 V

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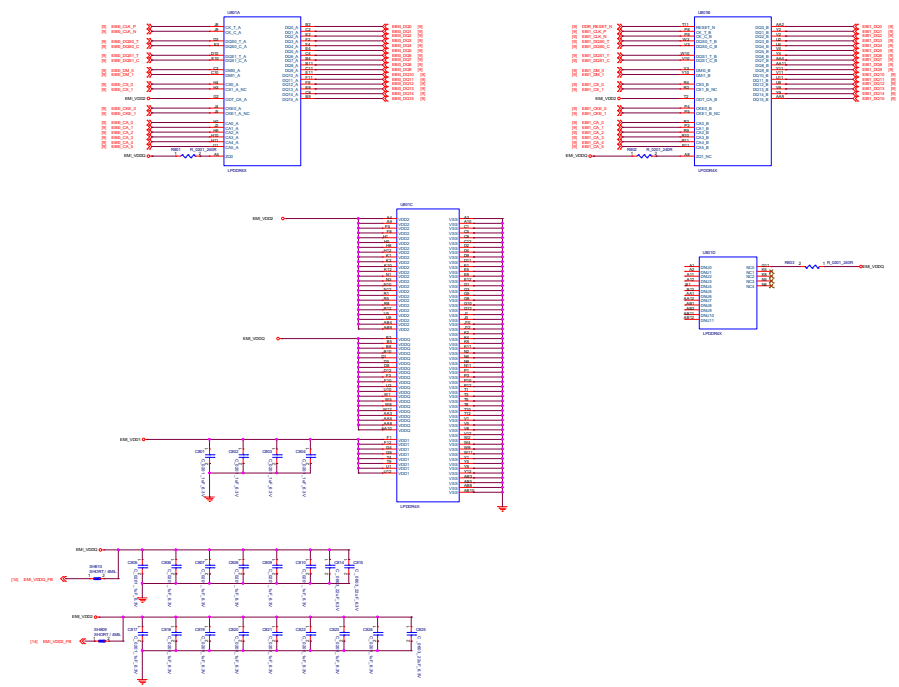
- AU_HPL and AU_HPR should be routed as single end signal and be guarded by GND, up and down, left and right respectively

- The suggested layout pattern of AU_HPL/AU_HPR/AU_REFN is "GND AU_HPL AU_REFN AU_HPR GND"



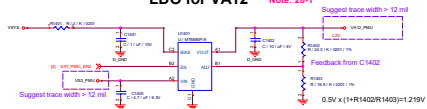
1. AVSS18_AUD is connected to GND in very short trace
2. AVSS18_AUD is connected to de-couple cap of AVDD18_AUD and AU_V18N with 6mil. trace respectively

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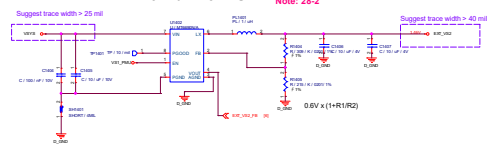
LDO for VA12

Note: 28-1



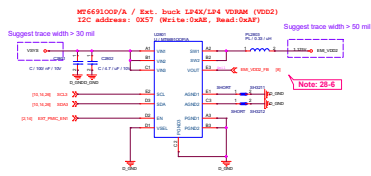
Ext. Bulk for VS2

Note: 28-2



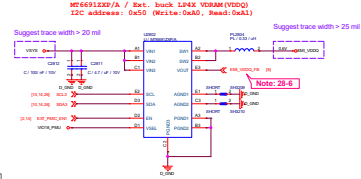
Ext. buck LPDDR4X/LPDDR4 VDRAM

Note: 28-4

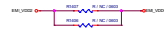


Ext. buck LPDDR4X VDDQ

Note: 28-4

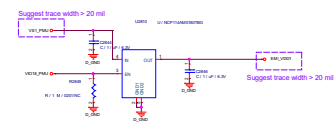


Reserved for LP4 DRAM [VDDQ=1.1V]



LPDDR4X/LPDDR4 VDD1 1.8V LDO

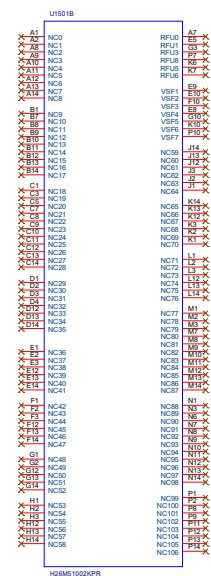
Note: 28-5



Note 28-1: VA12 Layout placement please close to AP

Note 28-2: VS2 Buck Layout placement please close to PMIC M76357, only used for M76762, NC for M76761

Rev	Rev	Rev
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1.2	1.2	1.2
1.3	1.3	1.3
1.4	1.4	1.4
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1.6	1.6	1.6
1.7	1.7	1.7
1.8	1.8	1.8
1.9	1.9	1.9
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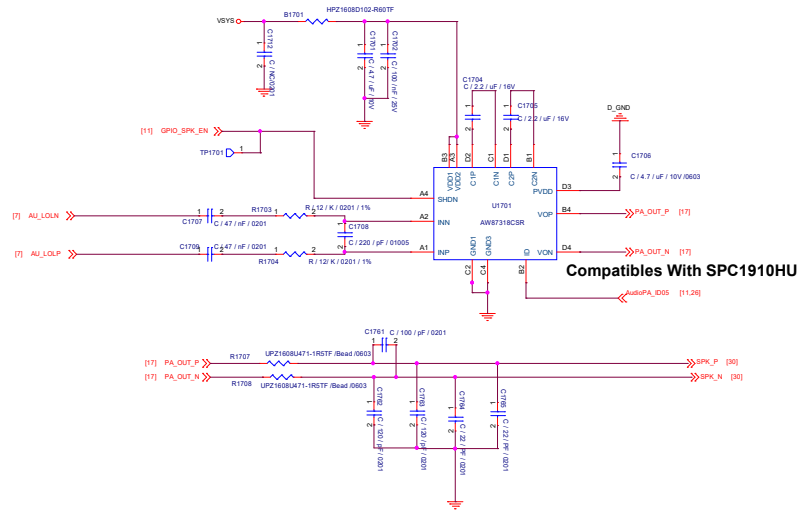


Project	C1517	C1418
MT6765	2.2uF	1uF
MT6762	2.2uF	1uF
MT6761	0.1uF	0.1uF

Project	C1517	C1418
MT6765	2.2uF	1uF
MT6762	2.2uF	1uF
MT6761	0.1uF	0.1uF

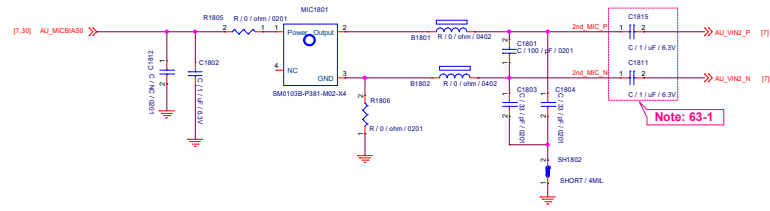
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Date: Wednesday, April 01, 2020	Sheet 16 of 38		

Class K PA

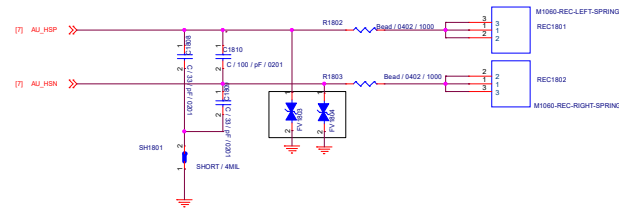
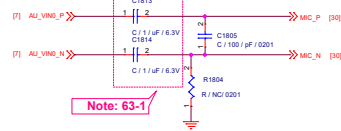


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MIC2



MIC1

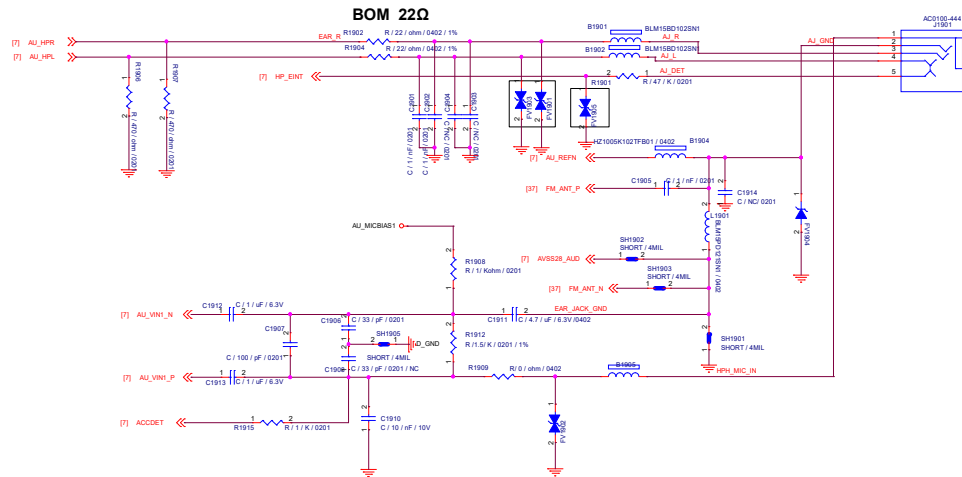


Schematic design notice of "63_PERI_AUDIO_IO" page.

Note 63-1: 1 uF for ACC mode
0 ohm for DCC mode

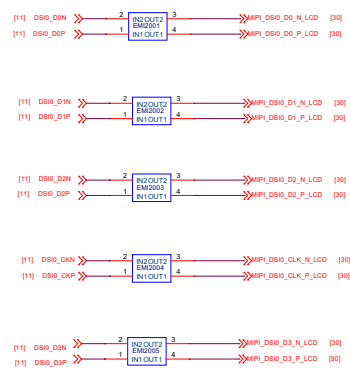
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Doc	Document Number	MC	
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A schematic diagram of a four-bar linkage mechanism. It consists of four links: a ground link (L), a crank link (R), a coupler link (G), and a follower link (M). The links are connected in a closed loop. The ground link is represented by a vertical line on the right. The crank link is a horizontal line on the left. The coupler link is a horizontal line in the middle. The follower link is a horizontal line on the right. The mechanism is labeled L-R-G-M below it.



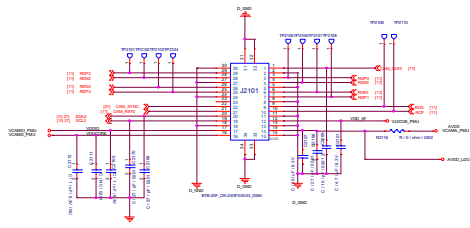
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Main LCM

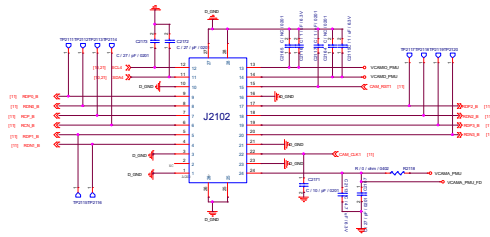


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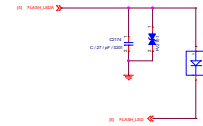
Main Camera



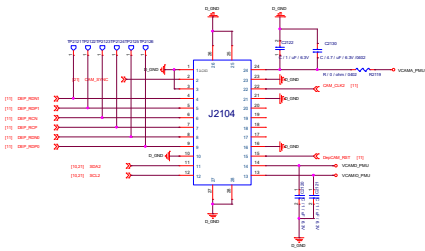
Front Camera



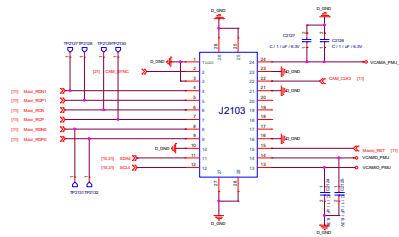
Main Flash LED



Macro Camera

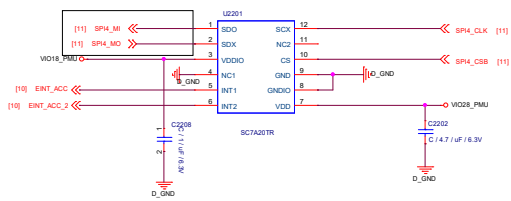


Dep Camera

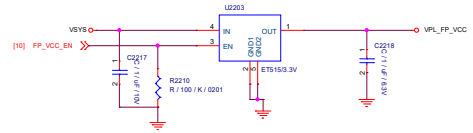
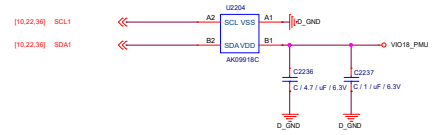
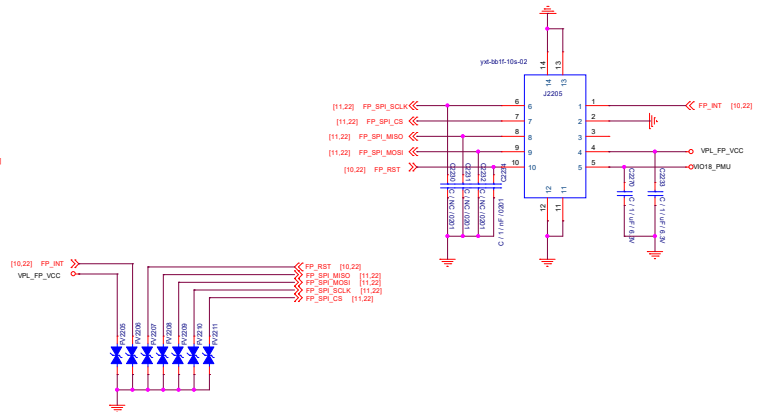
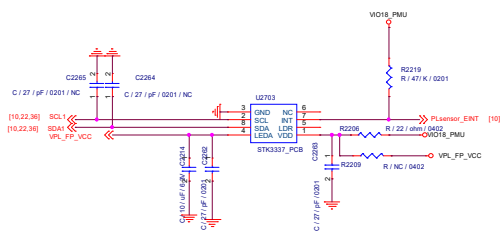


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1	2	3	4

G-Sensor

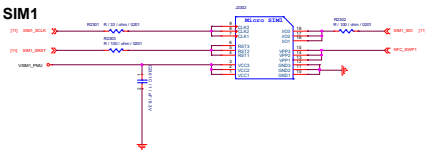


M SENSOR

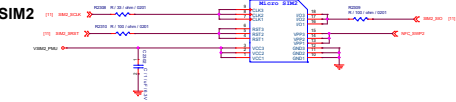
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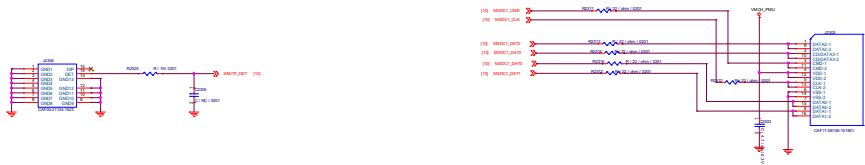
SIM1



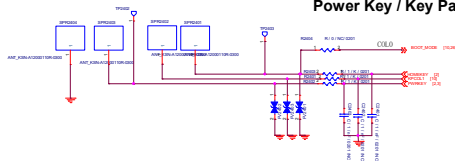
SIM2



SD CARD



Power Key / Key Pad



Title		Assessor	
Area	Estimate Number	History	W.D.
Date	Wednesday, April 01, 2003		Time: 10:07 AM

Name	
Address	
City	
State	
Zip	
Phone	
E-mail	

Timing diagram showing signals IDCKG, USB_DM, USB_DP, and VBUS_IN. The signals are connected to TP3005, TP3004, TP3003, and TP3001 respectively. The diagram shows the timing relationship between these signals, with IDCKG, USB_DM, and USB_DP having a [30] label.

eMMC

- [15] MSDIO_RSTB → TP2600
- [16] MSDIO_CMD → TP2626
- [15] MSDIO_DATA → TP2629
- [16] MSDIO_DSL → TP2631
- [10,14] SCL3 → TP2601
- [10,14] SDA3 → TP2602
- [4,10] SCL6 → TP2603
- [4,10] SDA6 → TP2604

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Note 52-1: NFC host I/F and power info are listed in the above connector, NFC COB reference schematic is in the file named "MTK ST NFC Reference Schematic_20170809"

Note 52-2: When NFC is applied, please keep
1. 0ohm NC between VSIM1_PMU and SIM1_VCC
2. 0ohm NC between VSIM2_PMU and SIM2_VCC

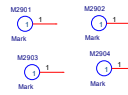
Note 52-3: When NFC is applied, please follow NFC COB reference schematic to draw NFC COB schematic

Title		Accession	
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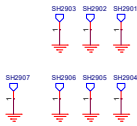
贴片器件，钢网要开



Shielding frame



Marks point

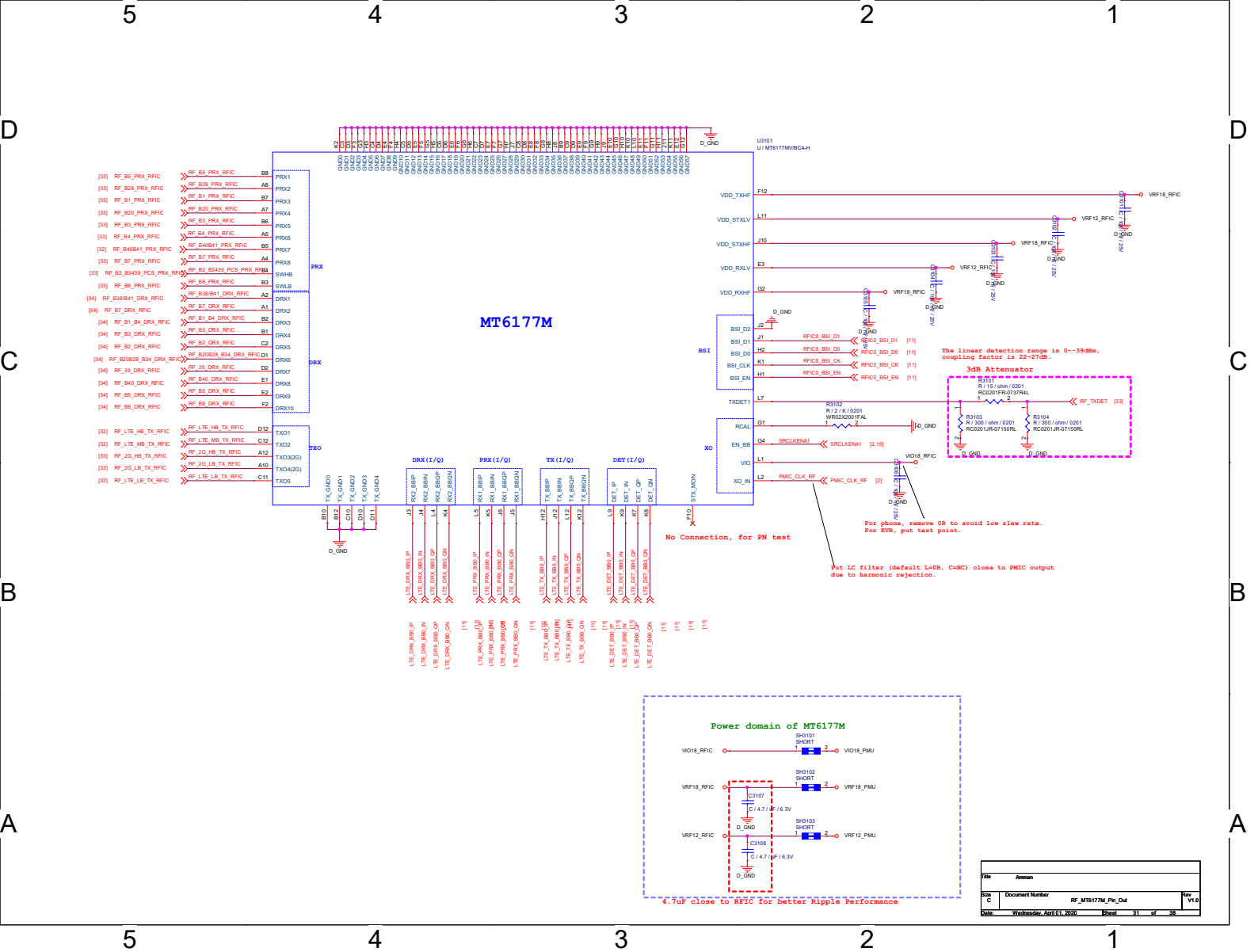


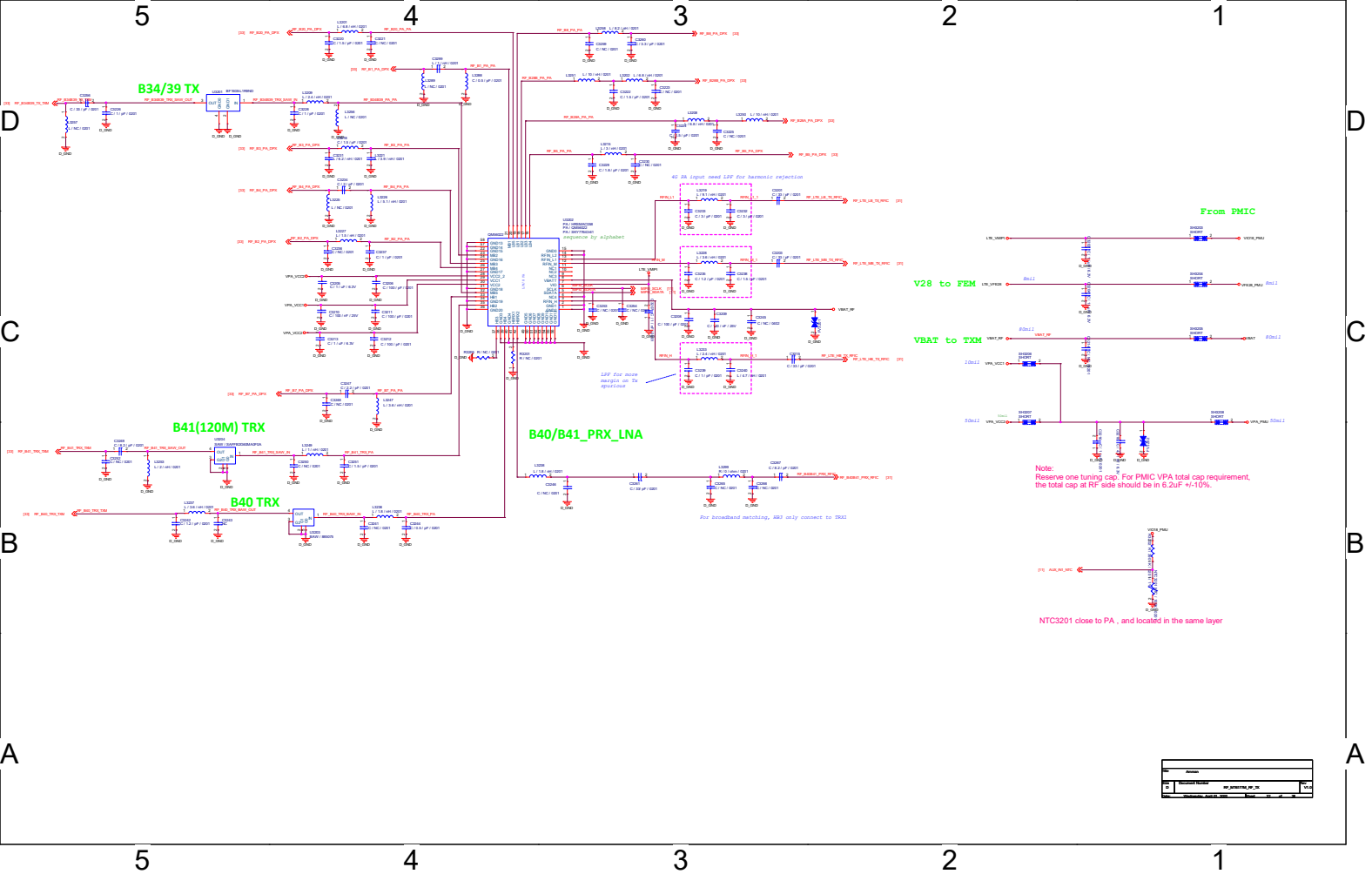
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Size	Document Number				Rev
C	Shielding				V1.0
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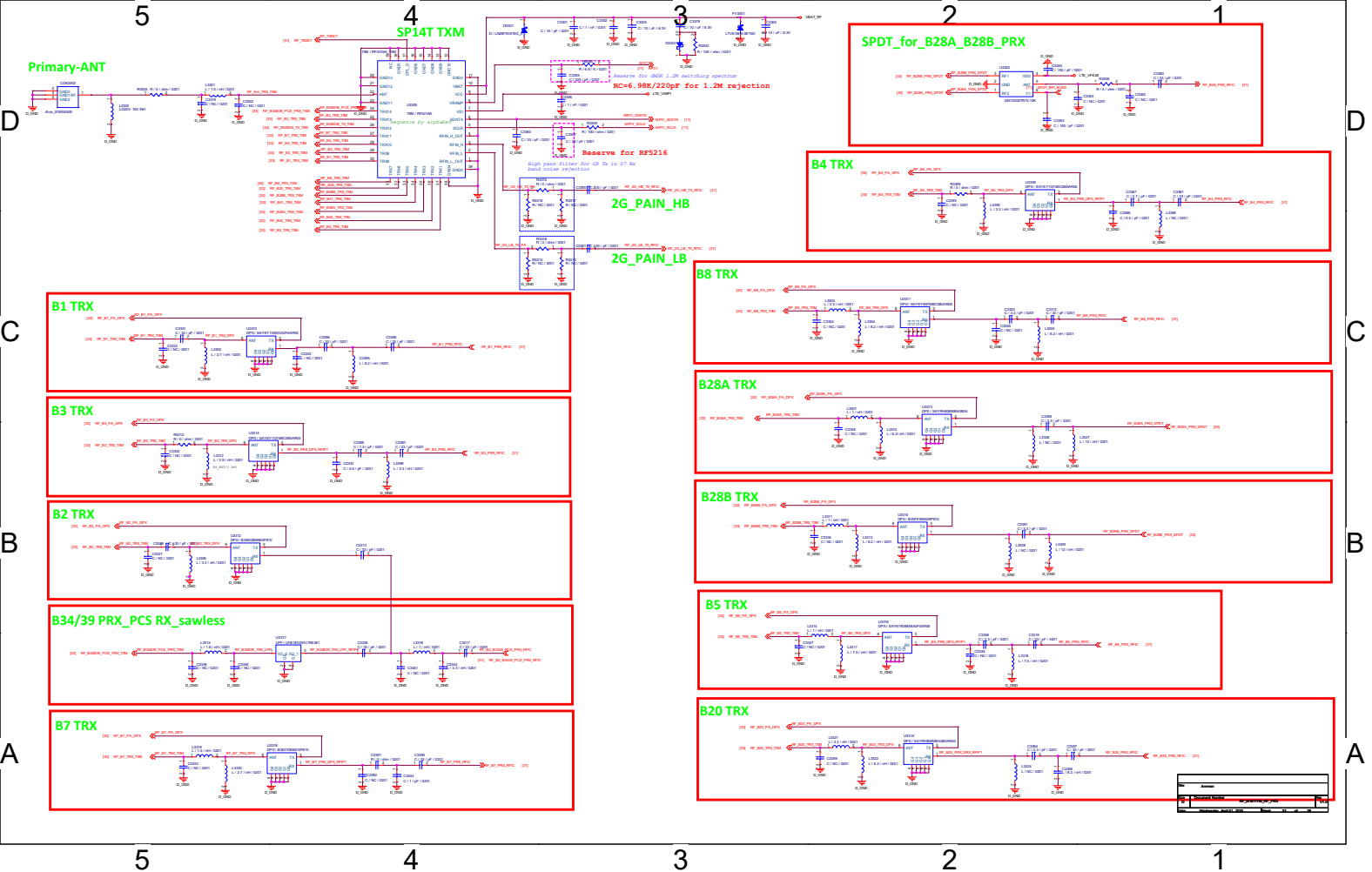


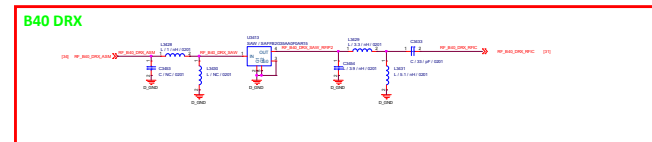
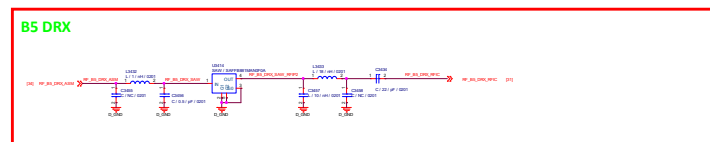
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File Automata	
Size ID	Description / Remarks PSP_MF_WESTING_HIP_0000

